

# MICROFABRICATED THERMOELECTRIC MATERIALS AND DEVICES FOR WASTE HEAT HARVESTING

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# Abstract

Thermoelectric generators offer a unique opportunity to convert thermal gradients directly to electrical power in a reliable, solid-state device containing no moving parts. Devices are scalable to the kilowatt range and higher, and there has been great success implementing generators in niche applications like power supplies for deep space missions using bulk-machined materials. More recently, advances in fabrication technology have enabled the design of materials and devices with micro- and nano-scale features. These advances have opened new working domains for small form-factor generators to harvest near-ambient low-grade “waste” heat and convert it to electrical power in the  $\mu\text{W}$ - $\text{mW}$  domain for use in low power consumption devices such as wireless sensors and wearable electronics. In particular, thin-film fabrication techniques like physical vapor deposition permit patterning of devices with very high thermocouple density resulting in voltages and power densities on the order of 1 V and  $1 \text{ mW}/\text{cm}^2$ , respectively, driven by a temperature differential of only a few degrees.

We begin with a study of fundamental thermal transport in a new class of nanostructured polysilicon thermoelectric materials that exhibit enhanced thermoelectric power factor. Through a combination of measurement techniques, we are able to demonstrate a positive correlation between material thermal conductivity and the size of nanoscale voids present within the material. These trends are validated conceptually using Matthiessen’s rule scaling arguments, and numerically using Monte Carlo ray tracing to quantify the effects of geometric scattering on cross-plane thermal transport due to void and grain boundary contributions. The results of this study suggest the potential for process-dependent control of thermal conductivity in silicon with high power factor. Second, we shift perspective from nanoscale materials

## *ABSTRACT*

to microscale devices and discuss development and navigation of the design optimization space for microfabricated thermoelectric generators. Through conscientious design of factors such as the fill fraction and number of thermocouples, among others, a roadmap is developed for optimization of devices developed for near-ambient thermal energy harvesting. The applicability of the common thermoelectric “figure of merit”  $ZT$  is also called into question when evaluating devices fabricated at the micrometer scale. Third, we outline the fabrication process implemented to fabricate prototype devices using a thin film deposition approach and characterize their performance as electric power generators with an infrared microscopy technique. We demonstrate working generators delivering more than 1 mW actual load power from less than 10 °C temperature difference. Finally, we step back and review solutions for system-level thermomechanical packaging and integration with power conditioning circuitry for the robust, efficient implementation of small form factor thermoelectric generators as power supplies for low power electronics. Acknowledging the rapidly-growing interest in distributed-scale energy harvesters for autonomous sensor networks, wearable electronics, medical devices, and other low power electronics, the goal of this work is to demonstrate the connected nature of physics from the nanometer scale to macroscale systems and routes to optimization in each regime.

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# Chapter 1

## Introduction

This section introduces the processes involved in thermoelectric phenomena, and their relevance to specific functional thermoelectric devices.

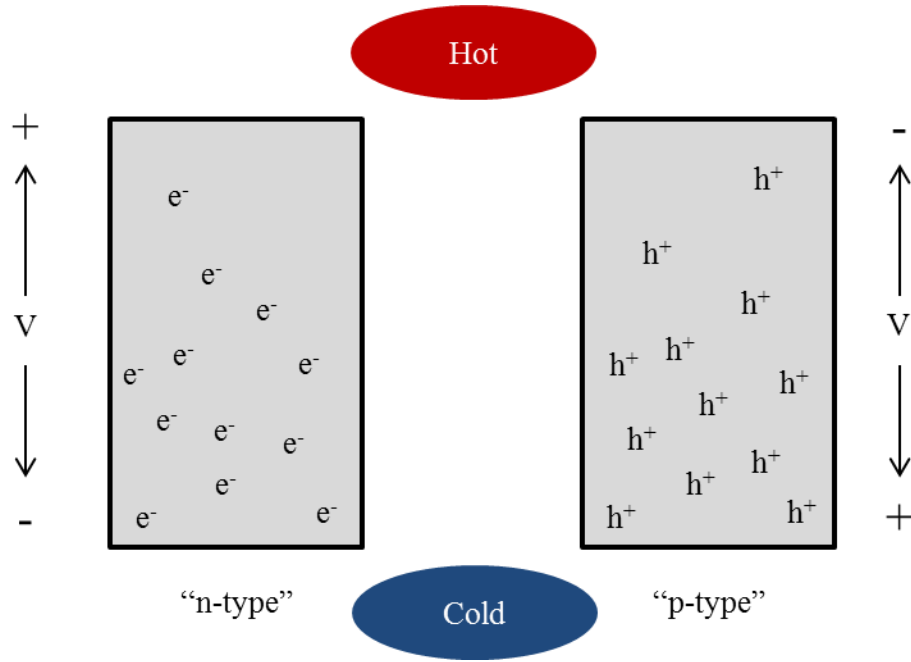
### 1.1 Thermoelectric Phenomena

Thermoelectric phenomena include the Seebeck Effect, the Peltier Effect, and the Thomson Effect. Sometimes collectively referred to as the Thermoelectric Effect, they describe the direct conversion between a thermal gradient and an electric potential (and vice-versa) in materials. Thermoelectric effects are present to some degree in all materials with free electrons or holes, though they are most prominent and useful in a small subset of metals and semiconductors. While thermoelectric metals are widely used in thermocouples for temperature measurement, semiconductors are more common in complex functional devices for thermal management and power generation, and will be the material class of emphasis in this dissertation.

#### 1.1.1 The Seebeck Effect

In the presence of a temperature gradient, carriers such as phonons, free electrons, or free holes will transport thermal energy from the hot end of a material to the cold end. In the case of free electrons and holes, an electric potential will also be established across the material as the population density of charge carriers increases at the cold end. Depending on the majority charge carrier of the material (electrons in n-type semiconductors and holes in p-type semiconductors), either a positive or negative voltage will be present along the thermal gradient as illustrated in Figure 1-1.

## INTRODUCTION



**Figure 1-1.** Illustration of the Seebeck effect in n- and p-type thermoelectric materials.

The Seebeck voltage is the electromotive force reacting to the buildup of charged carriers in the material and defined mathematically as the product of the temperature gradient  $\nabla T$  and the Seebeck coefficient  $S$ :

$$E_{\text{emf}} = -S\nabla T \quad (1.1)$$

This term contributes to the electric current density  $J$ , such that :

$$J = \sigma(-\nabla V + E_{\text{emf}}) \quad (1.2)$$

In the absence of electric current flow through the material (i.e. open-circuit), the Seebeck coefficient can be defined, and measured, as the negative ratio of the local voltage and temperature gradients:

$$S = -\frac{\nabla V}{\nabla T} \quad (1.3)$$

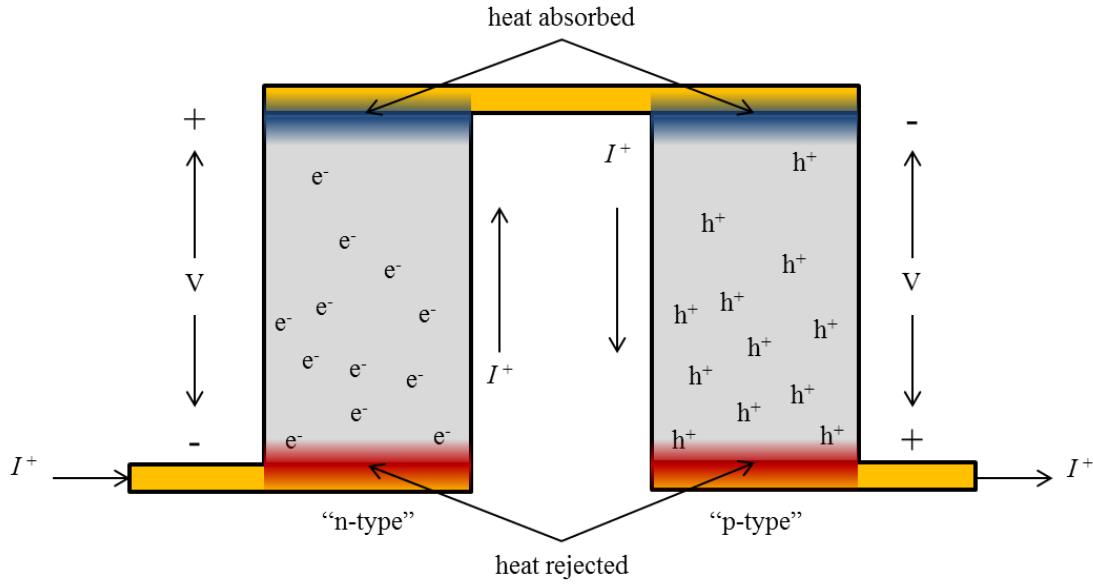
Equation 1.3 is valid for zero current flow through the material and for small temperature gradients, as the Seebeck coefficient is in general a temperature-dependent property.

### 1.1.2 The Peltier Effect

When electrical current is passed through a thermoelectric material, heat is transported by the motion of the charge carriers. When this current passes through an interface between two materials with different Seebeck coefficients, a discontinuity in heat flow driven by the electric current arises, and heat is either absorbed or rejected at the interface. This is referred to as the Peltier heat, and with conventional current flowing from material 1 to material 2, is described mathematically as:

$$\dot{Q}_{\text{Peltier}} = (S_1 T_1 - S_2 T_2) I_{1 \rightarrow 2} \quad (1.4)$$

where  $T_1$  and  $S_1$  are the local temperature and Seebeck coefficient of material 1 at the interface. The effect is illustrated in Figure 1-2 for a single thermocouple of an n-type material ( $S_n < 0$ ), a p-type material ( $S_p > 0$ ), and a metallic interconnect ( $S \sim 0$ ).



**Figure 1-2.** Illustration of the Peltier effect in a thermocouple structure.

With the direction of electric current flowing from n-type to p-type material, the heat rate described in Equation 1.4 is negative at the top of Figure 1-2 ( $\dot{Q} = (S_n - 0)I^+$  and  $\dot{Q} = (0 - S_p)I^+$ ), indicating that heat is absorbed at the junctions. Conversely, the heat rate is positive at the bottom of Figure 1-2 ( $\dot{Q} = (0 - S_n)I^+$  and  $\dot{Q} = (S_p - 0)I^+$ ), indicating that heat is rejected or released at the junctions. In this manner, the thermocouple acts as a heat pump from top to bottom in the figure. Changing the direction of electric current likewise reverses the direction of heat pumping.

### 1.1.3 The Thomson Effect

When a temperature gradient is present which results in variation of the temperature-dependent Seebeck coefficient, electric current passing through the material will cause the release or absorption of a continuous differential amount of heat along the current pathway inside the material. This heat arises from the Thomson effect, which in essence is the Peltier effect inside a single material due to differential changes in the local Seebeck coefficient. In most thermoelectric devices, and

particularly for devices operating with small temperature gradients as typical of the devices concerning this dissertation, the Thomson effect is negligible.

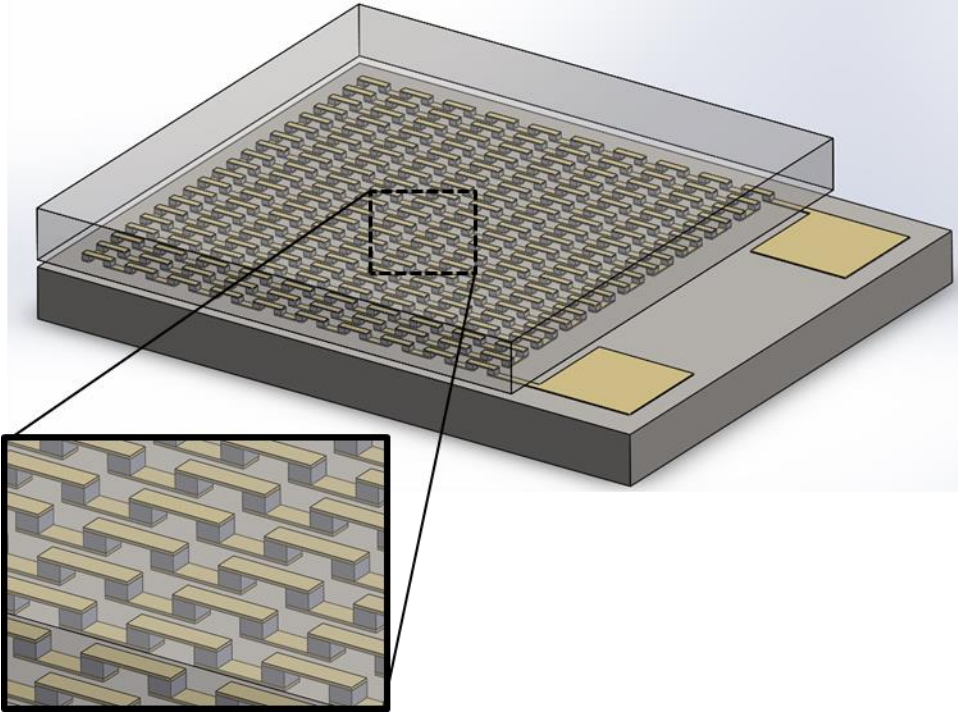
## **1.2 Use of Thermoelectric Phenomena in Functional Devices**

The thermoelectric phenomena described above, most significantly the Seebeck and Peltier effects, lend themselves to convenient use for solid-state thermal management and electric power generation.

### **1.2.1 Thermoelectric Devices for Thermal Management**

Thermoelectric devices enjoy widespread use as thermal management solutions for heating and cooling, with applications including refrigerators [1], vehicle seat temperature controllers [2], coolers for microelectronics [3], and more. While typically demonstrating a lower coefficient of performance than traditional thermodynamic heat pumps and refrigeration cycles, advantages exist in their rapid response time and the fact that they are solid state devices with no moving parts [1]. Thermoelectric devices used in this manner rely fundamentally on the Peltier effect. Traditionally, by arranging a large number of thermocouples thermally in parallel and electrically in series as illustrated in Figure 1-3, a driving current will pump heat from one side of the device to the other via heat absorption or rejection at each material junction according to Equation 1.4.

## INTRODUCTION



**Figure 1-3.** Illustration of vertically-aligned Peltier device with thermoelectric elements arranged thermally in parallel and electrically in series. In this design, current would be supplied using the protruding square contact pads and heat would be pumped up or down through the device depending on current direction.

The magnitude of heat released or absorbed at each junction is proportional to the transmitted electric current, and to a point an increase in electric current drives more heat through the device by the Peltier effect. However, the materials in a Peltier device are not perfect conductors, and resistive Joule heating enters proportional to the square of current as:

$$\dot{Q}_{\text{Joule}} = I^2 R \quad (1.5)$$

This competing term dominates with sufficiently high currents in a Peltier device, resulting in an optimal cooling condition, after which point Joule heating will dominate and release heat throughout the entire device.

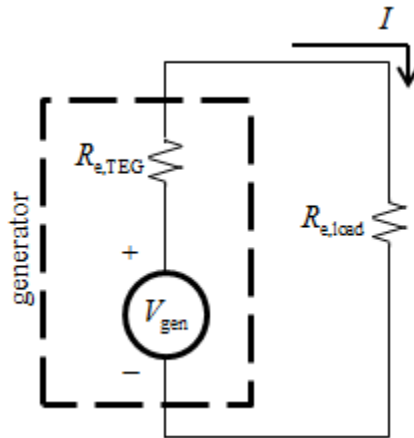


### 1.2.2 Thermoelectric Devices for Electric Power Generation

For electric power generation, thermoelectric devices make use of the Seebeck effect. Like thermal management devices such as Peltier coolers/heaters, thermoelectric generators are most commonly designed to be thermally in parallel and electrically in series. By connecting a large number of thermocouples in this manner, the electric potential produced by the Seebeck effect is multiplied as given in Equation 1.6:

$$V_{\text{gen}} = n_{\text{TC}} S_{\text{net}} \Delta T_{\text{TC}} \quad (1.6)$$

Here  $V_{\text{gen}}$  is the total voltage produced by the Seebeck effect,  $n_{\text{TC}}$  is the number of thermocouples,  $S_{\text{net}} = (S_p - S_n)$  is the net Seebeck coefficient of each thermocouple, and  $\Delta T_{\text{TC}}$  is the temperature gradient across the thermocouple array. When connected to an electrical load, the maximum power output of an ideal generator occurs with a load resistance matching the generator resistance, resulting in half the open-circuit voltage dropped across the load. We can prove this by considering the electric circuit diagram of a thermoelectric generator, given in Figure 1-4.



**Figure 1-4.** Electrical circuit model for a thermoelectric generator connected to a load.

## INTRODUCTION

The electric power delivered to the load is defined as:

$$P_{\text{load}} = \frac{V_{\text{load}}^2}{R_{\text{e,load}}} \quad (1.7)$$

The voltage  $V_{\text{load}}$  is calculated using a voltage divider expression:

$$V_{\text{load}} = V_{\text{gen}} \frac{R_{\text{e,load}}}{R_{\text{e,load}} + R_{\text{e,TEG}}} \quad (1.8)$$

Combining Equations 1.7 and 1.8 and taking the derivative with respect to the load voltage yields:

$$\frac{dP_{\text{load}}}{dR_{\text{e,load}}} = \frac{V_{\text{gen}}^2 (R_{\text{e,TEG}} - R_{\text{e,load}})}{(R_{\text{e,TEG}} + R_{\text{e,load}})^3} \quad (1.9)$$

For all other terms held constant, a local maximum exists when load resistance  $R_{\text{e,load}}$  is equal to generator resistance  $R_{\text{e,TEG}}$ , and the maximum load power of an ideal generator is calculated as:

$$P_{\text{max,ideal}} = \frac{V_{\text{load}}^2}{R_{\text{e,load}}} = \frac{V_{\text{gen}}^2}{4R_{\text{e,load}}} = \frac{n_{\text{TC}}^2 S_{\text{net}}^2}{4R_{\text{e,load}}} \Delta T_{\text{TC}}^2 \quad (1.10)$$

This derivation neglects contributions from Peltier heating and cooling and other losses, hence the “ideal generator” designation. When connected in a circuit, electric current flows through the generator, which results in Peltier heating and cooling at the thermoelement junctions and a coupling of the electrical and thermal systems. Due to the orientation of established electric potentials in the n- and p-type materials from the Seebeck effect (see Figure 1-1), heat will always be absorbed at the hot side and rejected at the cold side of the generator via the Peltier effect. This results in a

reduction of  $\Delta T_{TC}$  and is an unavoidable loss when operating the thermoelectric device as a power generator.

### 1.2.3 Generator Efficiency and the Thermoelectric Figure of Merit

It is impossible to review the scientific literature on thermoelectric materials and devices without encountering the so-called dimensionless thermoelectric figure-of-merit “ $ZT$ ”. This quantity combines three physical parameters of primary interest in the study and application of thermoelectric phenomena: Seebeck coefficient  $S$ , electrical conductivity  $\sigma$  or resistivity  $\rho$ , and thermal conductivity  $k$ :

$$ZT = \frac{S^2 \sigma}{k} T = \frac{S^2}{\rho k} T \quad (1.11)$$

Within  $ZT$  is another relevant quantity, referred to as the “power factor”, defined as:

$$PF = S^2 \sigma = \frac{S^2}{\rho} \quad (1.12)$$

While the figure of merit  $ZT$  is dimensionless, power factor is commonly reported in units of  $\text{mW m}^{-1} \text{K}^{-2}$ . The maximum thermal efficiency of a thermoelectric generator can be derived [4] in terms of the figure of merit for junction temperature difference  $T_h - T_c$  and average material temperature  $\bar{T}$  as:

$$\eta_{th,max} = \left(1 - \frac{T_c}{T_h}\right) \left( \frac{\sqrt{1 + Z\bar{T}} - 1}{\sqrt{1 + Z\bar{T}} + T_c / T_h} \right) \quad (1.13)$$

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The terms of Equation 1.13 present two key concepts. First, that a thermoelectric generator is a heat engine and therefore limited by the Carnot efficiency (first term). Second, that the maximum thermal efficiency possible for a thermoelectric generator is limited by the figure of merit, and converges to the Carnot efficiency as  $Z\bar{T} \rightarrow \infty$ . While there is no theoretical limit on the figure of merit, values approaching 1 are commonly considered to be characteristic of viable materials for thermoelectric applications.

$ZT$  in itself will receive limited treatment in this dissertation for reasons to be made more clear in the device analysis presented in Chapter 3. However, its form provides a valuable presentation of the desired qualities of a thermoelectric material. The Seebeck coefficient should be high, so as to produce a large voltage in response to a temperature gradient. The electrical conductivity should also be high, so as to improve electron transport and limit losses from electrical resistance. Conversely, the thermal conductivity should be low, such that a large temperature gradient is maintained across the material for a given heat flow.

### 1.2.4 Thermal Conductivity

A brief discussion of thermal conductivity in the context of  $ZT$  is warranted here, as its relationship to the other parameters motivate much of the efforts toward material optimization in the thermoelectrics literature. In a solid material, heat is transported by electrons and phonons which contribute individually to the material's overall thermal conductivity:

$$k = k_{\text{electron}} + k_{\text{phonon}} \quad (1.14)$$

Thermal transport at room temperature in poor electrical conductors (e.g. insulators and semiconductors) is typically dominated by the phonon contribution,

while transport in good electrical conductors (e.g. metals) is typically dominated by the electron contribution. While phonons themselves (differentiating from phonon drag effects which may contribute to the electric field by “pushing” electrons under certain conditions) are carriers only of thermal energy, electrons carry both thermal energy and electric charge. The Wiedemann-Franz-Lorenz law is an empirical correlation describing the relationship between the electronic contribution to thermal conductivity and the electrical conductivity in a material with mobile carriers (free holes or electrons):

$$\frac{k_{\text{electron}}}{\sigma} = L_0 T \cong \frac{\pi^2 k_B^2}{3q^2} T \quad (1.15)$$

Here,  $k_B$  is the Boltzmann constant,  $q$  is the electron charge, and  $L_0$  is known as the Lorenz number. Equation 1.15 is typically applicable at high temperatures (~room temperature and above) and at very low temperatures (~a few Kelvin), although the Lorenz number can vary between materials about its generalized value of  $2.45 \times 10^{-8} \text{ W } \Omega \text{ K}^{-2}$ . In the context of  $ZT$  and the idea of engineering thermoelectric materials with reduced thermal conductivity for improved the figure of merit, it is clearly desirable to reduce thermal conductivity by limiting only the phonon contribution if possible. This concept of limiting the phonon, or “lattice”, contribution to thermal conductivity while preserving electron transport is known in the literature as the “phonon-glass electron-crystal” approach [5]. While this concept illustrates the ideal configuration of phonon and electron transport in a thermoelectric material, the co-optimization of electrical and thermal conductivity remains a significant challenge and very active area of thermoelectrics research.

## 1.3 Organization and Scope of Work

Chapter 1 introduces the physics of thermoelectric phenomena and outlines the leverage of such effects for the design of functional thermoelectric devices. The

## INTRODUCTION

thermoelectric figure of merit  $ZT$  is introduced, as well as generator power and efficiency.

Chapter 2 discusses the use of the time domain thermoreflectance measurement technique for the thermal characterization of high thermoelectric power factor polysilicon thin films containing nanovoids. We show a positive correlation between measured thermal conductivity and mean void diameter. Matthiessen's rule scaling arguments and Monte Carlo scattering simulations are used to corroborate the dependence of thermal conductivity on void size.

Chapter 3 transitions from nanoscale thin film materials to microfabricated thermoelectric generators for waste heat harvesting. Reduced order models are developed to enable rapid parametric optimization, and validated with finite element models. Key parameters for device optimization are discussed in the context of a general methodology for optimizing microgenerators for power output. The appropriateness of  $ZT$  as a performance metric in the design of thermoelectric microgenerators is questioned and discussed.

Chapter 4 begins with a review and discussion of common experimental characterization techniques for thermoelectric devices. Next, results from the performance characterization of microfabricated prototype generators using a four-point electrical probe method as well as infrared microscopy are discussed.

Chapter 5 introduces the topics of thermomechanical packaging and power management system integration for microfabricated thermoelectric generators. Concluding remarks offer suggestions for the direction of future work.

# Chapter 2

## Enhanced Phonon Scattering by Nanovoids in High Thermoelectric Power Factor Polysilicon

This section presents experimental and numerical studies of thermal transport in nanostructured thin film polysilicon exhibiting high thermoelectric power factor.

### 2.1 Silicon as Thermoelectric Material

The pursuit of high-performance thermoelectric devices for both thermal management and thermal energy harvesting has been largely focused on increasing the dimensionless thermoelectric figure of merit  $ZT$ . The structure of  $ZT$  places a difficult physical constraint on this performance metric, as a high  $ZT$  simultaneously requires a high electrical conductivity and a low thermal conductivity. Since limitation of the electron contribution to thermal conductivity also penalizes the electrical conductivity, it is ideal to restrict thermal energy carrier scattering to phonons as much as possible.

Several materials have seen widespread use in thermoelectrics applications due to their inherently high  $ZT$  values near specific temperatures, for example SiGe near 1000 K ( $ZT \sim 0.8-1.2$ ) and  $\text{Bi}_2\text{Te}_3$  near room temperature ( $ZT \sim 1$ ) [6]. The use of silicon as a thermoelectric material offers several benefits, including a wealth of processing knowledge within the semiconductor industry, elemental abundance, low toxicity, and lower cost when compared to other materials which have seen widespread adoption in thermoelectric generators and Peltier coolers [7]. Bulk silicon has been regarded as a generally poor thermoelectric material due to its high thermal

conductivity ( $k \sim 140 \text{ W m}^{-1} \text{ K}^{-1}$ ) [8], which significantly reduces the figure of merit. However, precise nanostructuring has shown some success in reducing the thermal conductivity while preserving a desirable electrical conductivity because of the relative phonon and electron mean free paths in silicon. This is evident in recent results for silicon nanowires, which are engineered with dimensions that cause phonon energy carriers to scatter while minimizing additional scattering of electrons [9,10]. Silicon nanowires have been reported in the literature with thermal conductivities on the order of  $1 \text{ W m}^{-1} \text{ K}^{-1}$ , with  $ZT$  approaching 1 [9]. However, reliability of silicon nanowires in devices remains an issue, with specific challenges in maintaining electrical contact across the tips of bundles of nanowires [11]. Altering the phonon contribution to thermal conductivity is also possible by modifying the internal structure, where crystal grains and defects introduce scattering sites. Porous silicon structures are of particular interest as efficient phonon scatterers, and simulations [12] and measurements [13,14] have been reported in the literature for nanoscale to macroscale pores. Implantation of helium ions followed by thermal annealing is known to produce cavities or voids within silicon [15–18], including highly boron-doped polycrystalline silicon for which an anomalous increase in Seebeck coefficient and electrical conductivity has been observed due to a two-phase silicon-boride precipitate near the grain boundaries [19–21].

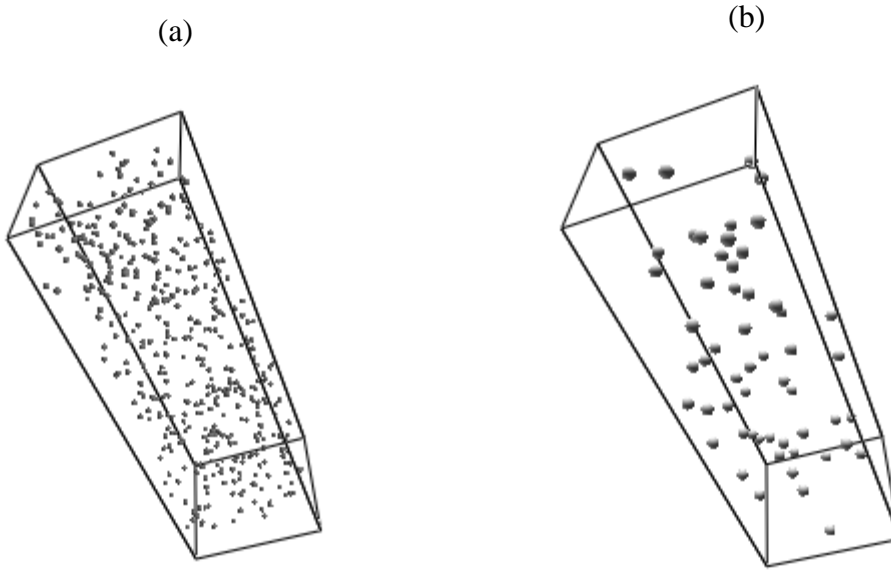
### **2.1.1 Nanovoids as Phonon Scatterers**

Phonons, or carriers of thermal energy transmitted through a material by vibration of atoms in the lattice, are the dominant thermal energy carrier in silicon at room temperature. Like other energy carriers, phonons transmit heat most effectively when they can travel a long distance uninterrupted. In a population of phonons, the average distance a carrier travels before a scattering event which disrupts this transport is called the mean free path,  $\lambda$ . This quantity can be related to the carrier's contribution to thermal conductivity through the simplified relation:



$$k = \frac{1}{3} C v \Lambda \quad (2.1)$$

where  $C$  is the carrier heat capacity in units of  $\text{J m}^{-3} \text{K}^{-1}$ ,  $v$  is the carrier velocity in units of  $\text{m s}^{-1}$ , and  $\Lambda$  is the carrier mean free path in units of  $\text{m}$ . The form of thermal conductivity given in Equation 2.1 represents an approximation that neglects the frequency dependence of the individual parameters with a so-called “gray” approximation. More exact calculations of thermal conductivity involve integration over a range of phonon frequencies using phonon dispersion models and accounting for frequency-dependent heat capacity and carrier scattering times. In a doped polycrystalline material, phonons will commonly scatter on dopant impurity atoms, grain boundaries, and other phonons. If defects or voids are introduced into the material, they will also impede phonon transport through scattering, reducing the mean free path  $\Lambda$  and subsequently the thermal conductivity  $k$  through the relation given by Equation 2.1. The films used in this study are highly-doped polycrystalline silicon films with the addition of nanoscale voids. Processing conditions have been shown to impact the size of the voids while retaining the same total volume fraction. These voids act as additional scattering sites which reduce the effective phonon mean free path. Figure 2-1 provides illustrations of single columnar silicon grains containing voids of different sizes, 2 nm diameter in (a) and 4 nm diameter in (b), but the same total volume fraction.



**Figure 2-1.** Perspective illustration of columnar grains containing randomly-arranged voids at a 0.5% volume fraction. In (a) the voids are each 2 nm in diameter with higher number density, while in (b) they are 4 nm in diameter with lower number density.

The impact of this relationship between void size and number density and thermal conductivity in the film is the focus of this chapter.

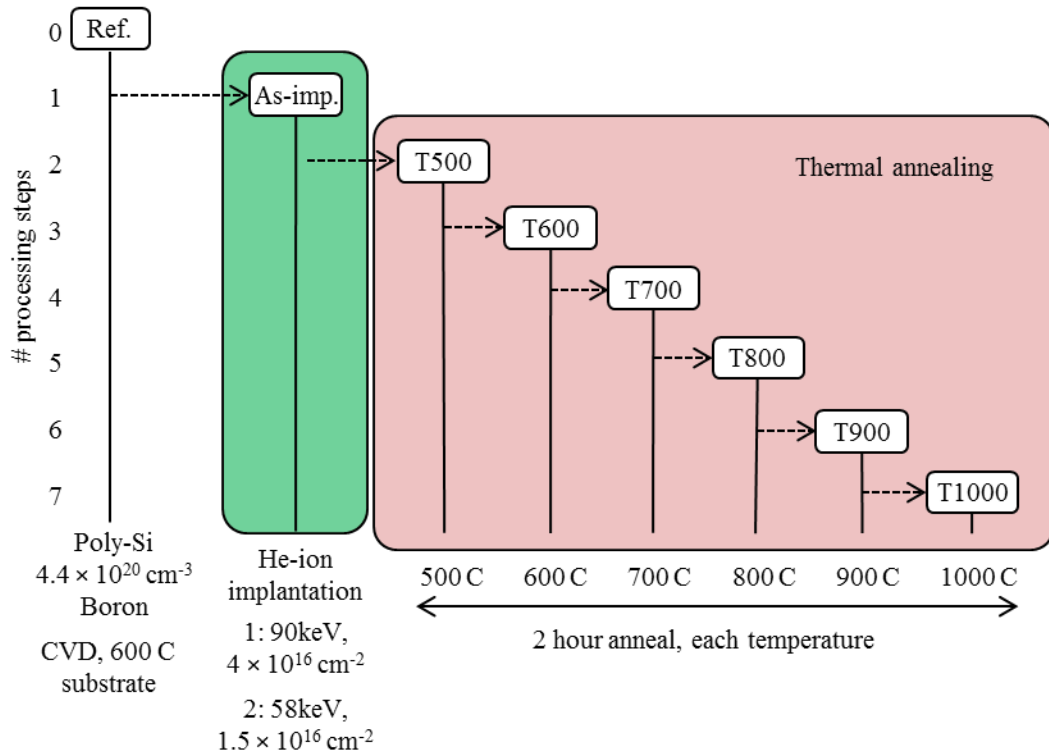
## **2.2 Polysilicon Sample Fabrication and Thermal Conductivity Characterization**

This section details the fabrication process for the polysilicon films, and the use of TDTR for measurement of the films' cross-plane thermal conductivities.

### **2.2.1 Thin Film Deposition and Nanovoid Formation**

Thin films of polycrystalline silicon were deposited to a thickness of 450 nm on a Si substrate with 88 nm thermal SiO<sub>2</sub> dielectric barrier using chemical vapor deposition (CVD) at 600 °C . The films were boron-doped by ion implantation at 60

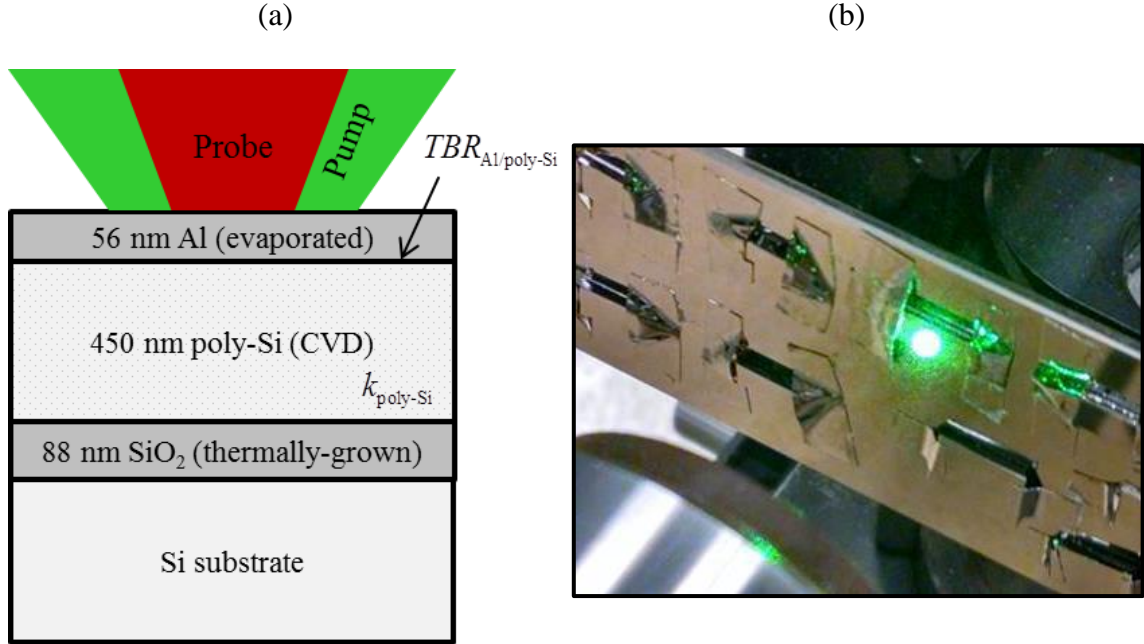
keV and  $2.0 \times 10^{16} \text{ cm}^{-2}$  to a nominal concentration of  $4.4 \times 10^{20} \text{ cm}^{-3}$ , followed by 30 s damage recovery at 1050 °C. Grains were found by TEM to be columnar, with dimensions of  $\sim 150 \text{ nm}$  in the cross-plane and  $\sim 50\text{-}80 \text{ nm}$  in the in-plane directions. A set of samples was implanted with He using a two-step implantation process at 90 keV with a fluence of  $4 \times 10^{16} \text{ cm}^{-2}$ , and 58 keV with a fluence of  $1.5 \times 10^{16} \text{ cm}^{-2}$ , through a  $\sim 250 \text{ nm}$  thick sacrificial aluminum layer. The aluminum layer was then removed with an HCl etch, and the film was subjected to a sequence of thermal annealing processes in an argon-heavy atmosphere. The first sample was annealed for 2 hours at 500 °C, the second for 2 hours at 500 °C followed by 2 hours at 600 °C, and so on until the sixth annealed sample was processed at a high temperature of 1000 °C for a total of 6 annealing stages after helium implantation [17]. Samples undergoing thermal annealing are referenced by ‘T’ followed by the highest anneal temperature (e.g. T500 for 500 °C max anneal). The process flow for the set of samples analyzed in this study is illustrated in Figure 2-2.



**Figure 2-2.** Illustration of process flow for each sample in the present study.

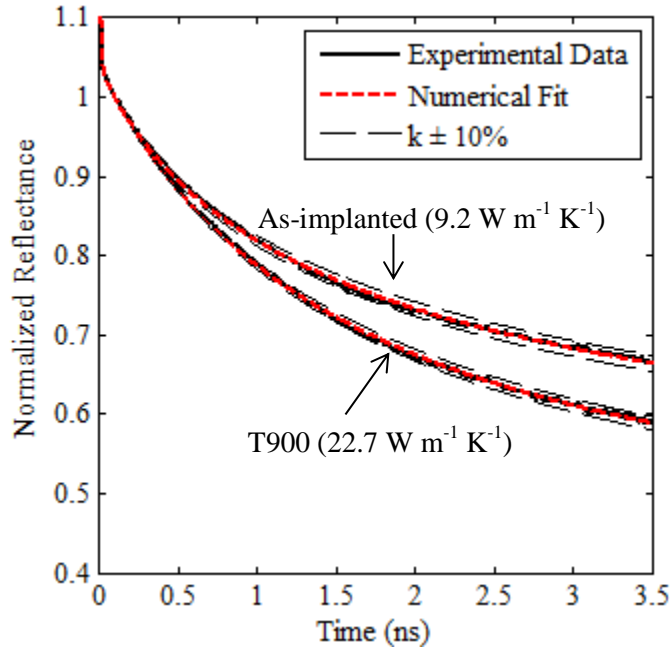
### **2.2.2 TDTR Measurement Theory**

Time domain thermoreflectance (TDTR), an optical pump-probe method, was used to measure the cross-plane thermal conductivity of the thin film polysilicon samples. TDTR is a well-established technique, which is used to measure thermal conductivity of thin films and bulk materials [22]. An aluminum transducer layer is deposited on top of all polysilicon films simultaneously by electron-beam evaporation. The thickness of the transducer layer is determined using a Tencor Alpha-Step 500 Surface Profiler to be 56 nm. Our TDTR setup uses a ~9 ps pulse-width, 82 MHz repetition rate laser source, split into pump ( $\lambda = 532$  nm) and probe ( $\lambda = 1064$  nm) components. The pump beam is amplitude modulated at a frequency of 1 MHz, and heats up the sample through absorption within the Al transducer layer. The time delayed probe beam (maximum delay time of 3.5 ns) measures the temporal rate of decay of temperature at the surface of the sample by interrogating the reflectivity of the Al layer. In these measurements, the pump and probe beams are focused down to  $1/e^2$  spot diameters of ~10 and 6  $\mu\text{m}$  [22]. The total optical power incident onto the sample is limited to ~10 mW, resulting in a steady state temperature rise of  $< 2$  K. The amplitude of the temperature decay normalized at +100 ps is fit to a three-dimensional thermal model using a non-linear least squares routine to simultaneously extract the cross-plane thermal conductivity of polysilicon, and the Al/poly-Si thermal boundary resistance (TBR). For the 56 nm aluminum transducer layer we assume a heat capacity of  $2.44 \text{ MJ m}^{-3} \text{ K}^{-1}$  and a thermal conductivity of  $100 \text{ W m}^{-1} \text{ K}^{-1}$ . For the poly-Si and Si substrate layers we assume a heat capacity of  $1.66 \text{ MJ m}^{-3} \text{ K}^{-1}$ , and a substrate thermal conductivity of  $148 \text{ W m}^{-1} \text{ K}^{-1}$ . For the buried  $\text{SiO}_2$  layer we assume a heat capacity of  $1.62 \text{ MJ m}^{-3} \text{ K}^{-1}$ , a thermal conductivity of  $1.38 \text{ W m}^{-1} \text{ K}^{-1}$ , and a TBR of  $5 \text{ m}^2 \text{ K GW}^{-1}$  at the poly-Si/ $\text{SiO}_2$  and  $\text{SiO}_2$ /Si interfaces, on the order of TBR values extracted by Kädin *et al.* [23]. An illustration of the sample stack and photo of laser incident on the sample surface is given in Figure 2-3.



**Figure 2-3.** (a) Schematic of TDTR measurement showing the sample stack, and (b) photograph of laser striking sample surface.

Figure 2-4 shows data and best fits for two samples that have the lowest and highest conductivities of the poly-Si samples, illustrating the general trend of faster decay in the normalized surface reflectance for higher conductivity material. This is due to the faster diffusion of heat from the surface down into the material(s) underneath the transducer layer. As validation, a witness sample consisting of 50 nm thick thermally-grown SiO<sub>2</sub> on silicon substrate was coated in the same aluminum evaporation step. Measurements yielded a thermal conductivity of  $1.33 \text{ W m}^{-1} \text{ K}^{-1}$  at room temperature in good agreement with literature [24].



**Figure 2-4.** Experimental data and numerical fits for As-implanted and T900 samples.

On the polysilicon samples, measurements were taken at three spots per sample, in order to probe the level of film inhomogeneity. For 6 of 8 measured samples, the spatial variation in conductivity is less than 3%, while 2 samples in the set (T600 and T1000) showed a maximum spatial variation of 11%. Error bars are calculated by combining in quadrature  $\pm 5\%$  uncertainty in aluminum transducer thickness and standard deviation from 3 spot measurements per sample. The Al/poly-Si TBR for all our samples falls within the range 7-9 m<sup>2</sup> K GW<sup>-1</sup>, except for T1000 where TBR  $\sim$  12 m<sup>2</sup> K GW<sup>-1</sup>. No systematic variation of TBR with final annealing temperature was observed.

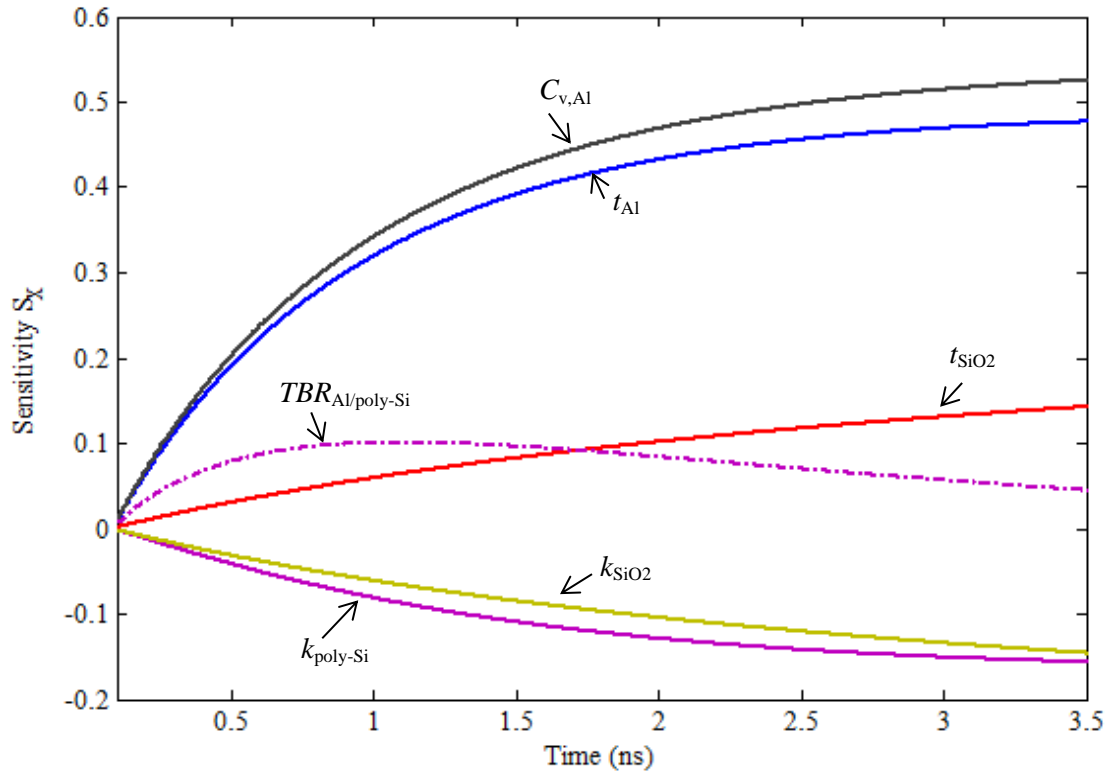
### 2.2.3 Sensitivity Analysis

The sensitivity of the TDTR technique to different properties of the materials in the layered structure is quantified using the differential change in the measured

normalized reflectance caused by a differential perturbation in a specific property  $X$  about a nominal value. A normalized sensitivity coefficient  $S_X$  for parameter  $X$  can then be defined as:

$$S_X = \frac{\partial \ln(R)}{\partial \ln(X)} \quad (2.2)$$

where the measured signal  $R$  is the amplitude of the in- and out-of-phase voltage signals from the RF lock-in amplifier. When all other parameters remain fixed,  $S_X$  indicates the relative sensitivity of the measured signal to a thermophysical parameter  $X$ . A plot of sensitivity to various parameters in the multilayered samples is provided in Figure 2-5.



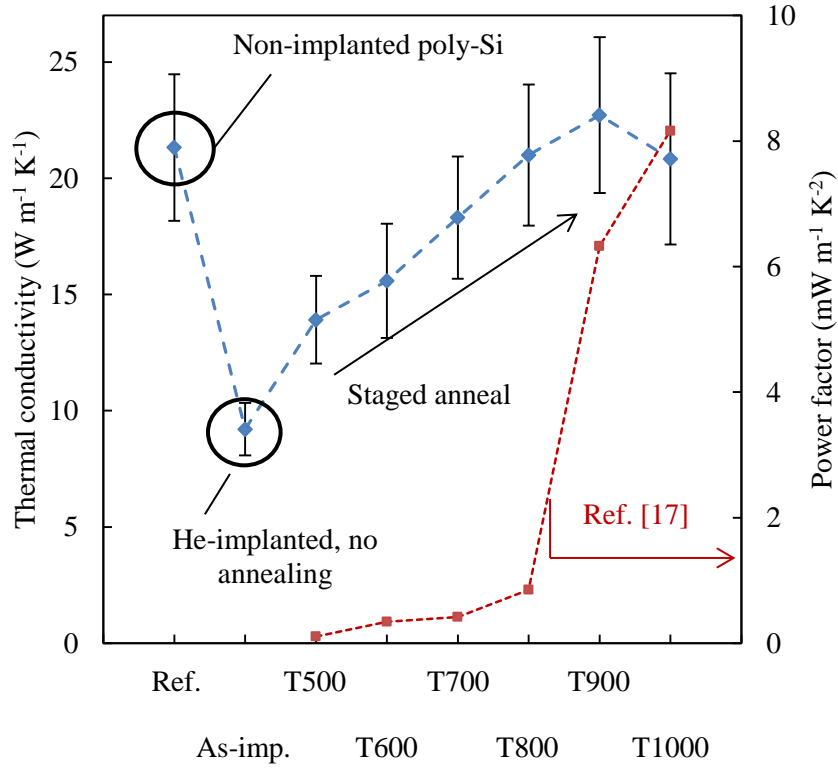
**Figure 2-5.** Plot of the normalized reflectance sensitivity over the measurement timescale for the various parameters in the multilayered silicon samples of this study for a pump beam amplitude modulation of 1 MHz.

The magnitude of the sensitivity parameter never exceeded 0.04 for the TBR at the SiO<sub>2</sub>/Si or poly-Si/SiO<sub>2</sub> interfaces, the specific heats of the poly-Si, SiO<sub>2</sub>, or Si layers, the aluminum thermal conductivity, or the thickness of the poly-Si and they have been omitted from Figure 2-5 for clarity. The sensitivity parameter plot indicates good sensitivity to the fitting parameters  $TBR_{\text{Al/poly-Si}}$  and  $k_{\text{poly-Si}}$ . These are comparable to the sensitivity to the thickness and thermal conductivity of the SiO<sub>2</sub> layer, but these should be well-known for thermally-grown oxide films. The reflectance signal is highly-sensitive to the aluminum transducer layer thickness and specific heat. The specific heat is assumed to be well-known for evaporated aluminum, but the sensitivity to the thickness is accounted for with an assumed  $\pm 5\%$  variability that contributes to the experimental error bars as discussed in the previous section.

#### **2.2.4 Thermal Conductivity of Polysilicon Thin Films**

The evolution of thermal conductivity as a function of processing condition in Figure 2-6 shows that the films initially exhibit a significant 57% reduction in thermal conductivity after helium ion implantation (35% after the first thermal annealing step), but that the value returns to the level of the untreated sample after the high annealing temperature step reaches approximately 800 °C. A previous study of the Seebeck coefficient and electrical conductivity of identically-prepared films demonstrated a significant jump in thermoelectric power factor [17], but unfortunately not until the thermal conductivity was observed to have returned to non-implanted levels in this study. It was considered that the reduction in thermal conductivity could be due at least in part to grain growth through the annealing process. Plan-view SEM images were prepared and the average grain intercept method applied to confirm no significant variation in lateral grain size through the annealing process. Previous cross-section TEM imaging on similar samples also indicated no grain growth through the conditions used in this study [20], in agreement with previous studies showing the capability of boron to pin grain boundaries [25].





**Figure 2-6.** Plot of measured thermal conductivity (this work) and power factor [17] across the measured sample set.

Increases in electrical conductivity due to dopant reactivation (indicated by an initial rise in boron impurity concentration from Hall measurements) during thermal recovery from helium implantation will also contribute to an increased electron thermal conductivity, which is calculated in Table 2-1 as  $k_{e,\text{in-plane,WFL}}$  using the Wiedemann-Franz-Lorenz relation. While in-plane grains are known to be smaller than cross-plane grains in these samples which indicates higher electron thermal conductivity in the cross-plane direction, expected anisotropy ratios ( $\sim 2\text{-}3$ ) still suggest less than 5% contribution to total thermal conductivity from electron transport.

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**Table 2-1.** Experimental doping and transport data as a function of maximum annealing temperature.

Sample Label	$T_{a,max}$ [°C]	$B_{Si}$ [cm <sup>-3</sup> ]	$\rho_{in-plane}$ [Ω-m]	$k_{e,in-plane,WFL}$ [W m <sup>-1</sup> K <sup>-1</sup> ]	$d_{void,avg}$ [nm]	$k_{poly-Si}$ [W m <sup>-1</sup> K <sup>-1</sup> ]
nHeI <sup>a</sup>	N/A	-	-	-	N/A	21.3 ± 3.1
As-imp. <sup>b</sup>	N/A	-	-	-	-	9.2 ± 1.1
T500	500	3.26x10 <sup>19</sup> <sup>c</sup>	2.18x10 <sup>-4</sup> <sup>d</sup>	0.03	4.3 ± 1.4	13.9 ± 1.9
T600	600	5.76x10 <sup>19</sup> <sup>c</sup>	8.46x10 <sup>-5</sup> <sup>d</sup>	0.09	6.3 ± 1.8	15.6 ± 2.5
T700	700	9.10x10 <sup>19</sup> <sup>c</sup>	4.59x10 <sup>-5</sup> <sup>d</sup>	0.16	8.1 ± 2.9	18.3 ± 2.6
T800	800	1.01x10 <sup>20</sup> <sup>c</sup>	3.78x10 <sup>-5</sup> <sup>d</sup>	0.19	14.8 ± 4.8	21.0 ± 3.0
T900	900	8.13x10 <sup>19</sup> <sup>c</sup>	2.81x10 <sup>-5</sup> <sup>d</sup>	0.26	-	22.7 ± 3.3
T1000	1000	9.04x10 <sup>19</sup> <sup>c</sup>	2.38x10 <sup>-5</sup> <sup>d</sup>	0.31	29.2 ± 5.9	20.8 ± 3.7

<sup>a</sup> non-Helium-implanted.

<sup>b</sup> He-implanted with no subsequent annealing processes.

<sup>c</sup> Identically-doped films annealed at 30 minutes per step, Ref. [17]

<sup>d</sup> Ref. [17]

## 2.3 Dependence of Thermal Conductivity on Void Size

A positive correlation is observed between void size within the films and measured thermal conductivity. Wide-angle and shallow-angle X-ray scattering (WAXS/SAXS) data were obtained, except for the as-implanted and T900 samples, to quantitatively evaluate the mean diameter and size distribution of nanovoids through the range of film processing conditions. This technique has been previously utilized to characterize nano- and micro-scale void and defect structures in polysilicon [26,27]. This section discusses physical scaling arguments and numerical simulations validating the trends in the observed experimental data.

### 2.3.1 Matthiessen's Rule Scaling Argument

Previous work [18] showed that the processing steps used to produce these samples result in coalescence of many, smaller voids to fewer, larger voids as anneal

temperatures are increased. The trend in thermal conductivity to increase as the void distribution evolves to one with fewer, larger scattering sites with constant total volume is qualitatively consistent with Matthiessen's rule considering phonon-boundary, phonon-phonon, and phonon-void scattering, and assuming a fixed, circular scattering cross-section using mean void diameter  $D$ . Matthiessen's rule assumes that the individual scattering mechanisms are independent.

$$\frac{1}{\Lambda} = \frac{1}{\Lambda_{p-b}} + \frac{1}{\Lambda_{p-p}} + \frac{1}{\Lambda_{p-v}} = \frac{1}{\Lambda_{p-b}} + \frac{1}{\Lambda_{p-p}} + \frac{n\pi D^2}{4} \quad (2.3)$$

For constant total void volume fraction  $F$ , with number density  $n$  and single void volume  $V$ ,  $nV = F$ , the expression for mean phonon mean free path becomes:

$$\Lambda = \frac{1}{\frac{1}{\Lambda_{p-b}} + \frac{1}{\Lambda_{p-p}} + \frac{3F}{2D}} \quad (2.4)$$

The phonon mean free path will increase with void diameter assuming constant total void volume fraction  $F$  (assumed approximately 0.5% from previous studies [17]), constant phonon-boundary scattering mean free path  $\Lambda_{p-b}$ , and constant phonon-phonon scattering mean free path  $\Lambda_{p-p}$ , resulting in an increased thermal conductivity.

### 2.3.3 Monte Carlo Modeling of Void Contribution to Phonon Scattering

We developed a Monte Carlo ray tracing model to numerically study the dependence of thermal conductivity on a changing distribution of volumetric scattering sites by stochastically calculating the geometric scattering contribution from phonon-boundary and phonon-void interactions. Following the methodology described by Hori *et al.* [28], phonons are initialized at a random position on a starting plane (e.g. one end of a grain or nanowire) with random  $\varphi$  angle (rotation angle about the

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normal vector of the launch plane). Sets of phonons are released at increments of  $1^\circ$  for  $0.5^\circ \leq \theta \leq 89.5^\circ$ , where  $\theta$  is the angle of inclination from the launch plane. The launch vector is described mathematically by:

$$\vec{r} = \sin(\theta_{\text{launch}}) (\cos(\varphi_{\text{launch}}) \hat{t}_1 + \sin(\varphi_{\text{launch}}) \hat{t}_2) + \cos(\theta_{\text{launch}}) \hat{n}_{\text{surface}} \quad (2.5)$$

where  $\hat{n}_{\text{surface}}$  is the unit vector normal to the launch plane in the direction of launch (into the grain/nanowire), and  $\hat{t}_1$  and  $\hat{t}_2$  are unit vectors orthogonal to  $\hat{n}_{\text{surface}}$ . If the phonon's path crosses a grain boundary, the phonon is assumed to scatter diffusely at the point of intersection. The launch angles  $\theta$  and  $\varphi$  are computed using random numbers  $0 \leq R_1, R_2 \leq 1$  as:

$$\theta_{\text{launch}} = \frac{1}{2} \arccos(1 - 2R_1) \quad (2.6)$$

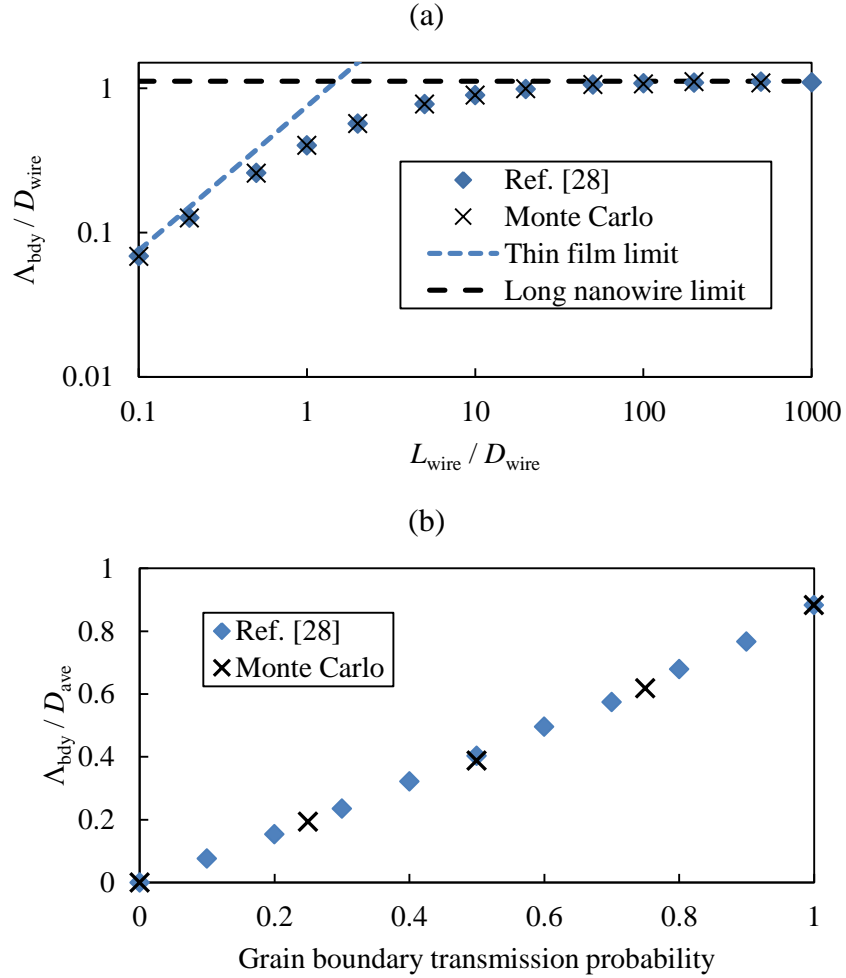
$$\varphi_{\text{launch}} = 2\pi R_2 \quad (2.7)$$

This process continues until the phonon intersects with the transmission plane (opposite end of the grain/nanowire) and is counted as fully transmitted, or until it intersects with the launch plane and is counted as fully reflected. For each incremental launch  $\theta$ , the fraction of launched phonons reaching the transmission plane becomes a transmission probability  $\tau_{12}$ . After the ray tracing operations conclude for all initial  $\theta$  values the mean free path due to boundary scattering can be defined as:

$$\Lambda_{\text{bdy}} = \frac{3}{2} L \int_0^{\pi/2} \tau_{12}(\theta) \cos(\theta) \sin(\theta) d\theta \quad (2.8)$$

where  $L$  is the distance from the launch plane to the transmission plane. Since the initial  $\theta$  values are discrete in increments of  $1^\circ$  from  $0.5^\circ$  to  $89.5^\circ$ , the integral in Equation 2.8 is computed using the trapezoid rule. The developed Monte Carlo code is

validated in and between the limits of thin film ( $D_{\text{wire}} \gg L_{\text{wire}}$ ) and long nanowire ( $D_{\text{wire}} \ll L_{\text{wire}}$ ) with Ref. [28], where  $D_{\text{wire}}$  is the side length of the geometry with square base through which the phonon is traversing. Results are shown in Figure 2-7a. The limiting cases include the analytical solution  $\Lambda_{\text{bdy}} = 1.12D_{\text{wire}}$  for a square nanowire of infinite length and  $\Lambda_{\text{bdy}} = 3L/4$  for cross-plane transport through a thin film having perfectly-absorbing contacts.



**Figure 2-7.** Validation of Monte Carlo code with Ref. [28] showing (a) limiting cases of thin film and long nanowire in single crystal simulations and (b) scaling of mean free path to characteristic grain size with grain boundary transmission coefficient in a polycrystal.

*ENHANCED PHONON SCATTERING BY NANOVOIDS IN HIGH  
THERMOELECTRIC POWER FACTOR POLYSILICON*

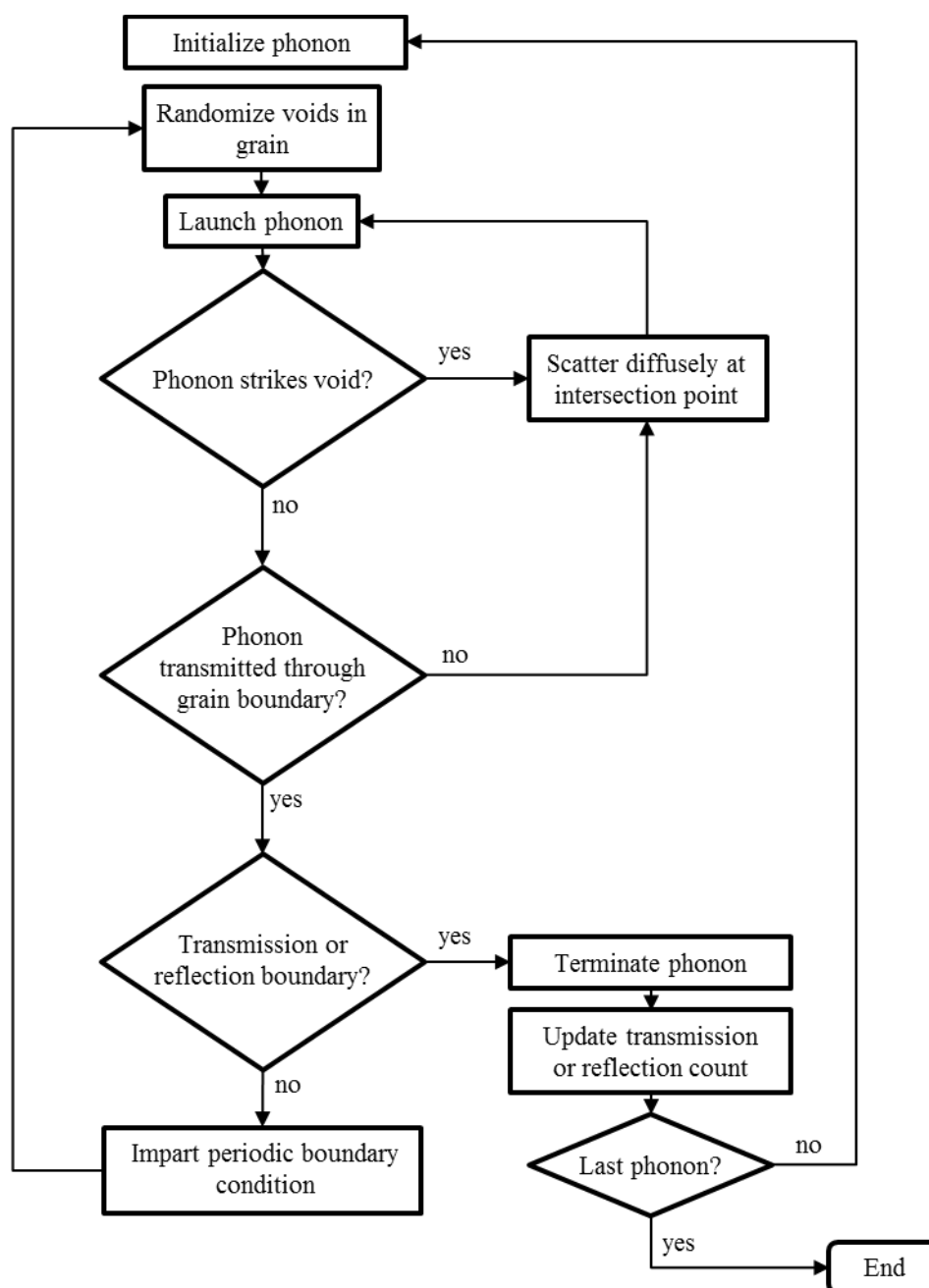
Extending the methodology to a polycrystal, a transmission coefficient  $t$  is assigned to stochastically determine transmission or reflection after intersection with a grain boundary. Hori *et al.* [28] evaluated the mean free path due to boundary scattering for a 200-layer polycrystal as a function of the grain boundary transmission coefficient. Polycrystal simulation functionality was added to the current code and results for a 200-layer polycrystal of 50 nm x 50 nm x 50 nm cubic grains validated against results from the reference article, shown in Figure 2-7b.

Transport through a polycrystalline structure 450 nm in thickness is modelled as three layers of 150 nm-thick grains with lateral dimensions 50 x 50 nm or 80 x 80 nm, using a gray approximation transmission coefficient at the grain boundaries and perfectly-absorbing film contacts. The grain boundary transmission coefficient is estimated using the form of an empirical model with  $\gamma = 2.4$  representing a low-resistance sintered silicon interface [28], assuming a maximum phonon frequency of  $\omega_{\max} \sim 15$  THz and a characteristic phonon frequency of  $\omega_{\text{gray}} \sim 2.5$  THz corresponding approximately to 50% accumulation of bulk thermal conductivity in room-temperature silicon (estimated from Refs. [29,30]):

$$t_{\text{gray}} = \frac{1}{\gamma \omega_{\text{gray}} / \omega_{\max} + 1} \quad (2.9)$$

Voids are re-oriented randomly each time a simulated phonon passes into a new grain, to reduce position bias and more accurately simulate a random distribution of voids at the polycrystal level. The phonon's path is checked for intersection with every spherical void in the current grain. Occasionally the path will intersect multiple voids. In this case, the calculated intersection point which is the minimum distance from the ray's starting location is determined to be the physical intersection point and the phonon is diffusely scattered from that location on the void. Simulations were repeated three times to calculate mean and standard deviation (which was within the height of the markers). A flow chart illustrates the ray tracing procedure in Figure 2-8. This

sequence is repeated for each set of discrete initial launch  $\theta$  angles ( $0.5^\circ$  to  $89.5^\circ$  in  $1^\circ$  increments for a total of 90 sequences each initializing 5000 phonon rays).



**Figure 2-8.** Monte Carlo simulation flow chart, run for initial launch  $\theta$  angles from  $0.5^\circ$  to  $89.5^\circ$  in  $1^\circ$  increments.

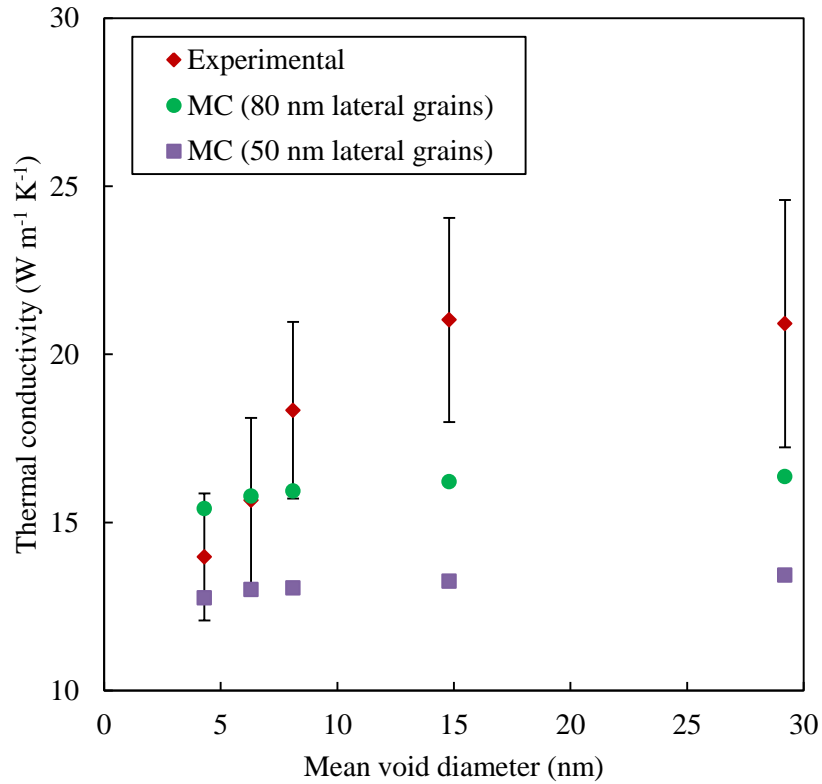
*ENHANCED PHONON SCATTERING BY NANOVoids IN HIGH  
THERMOELECTRIC POWER FACTOR POLYSILICON*

Once the geometric scattering mean free path (now including grain boundary scattering and void scattering) is determined from the ray tracing procedure and Equation 2.8, thermal conductivity is calculated using Matthiessen's rule using model data for comparably-doped bulk silicon [31] ( $\sim 38.6 \text{ W m}^{-1} \text{ K}^{-1}$  at  $4.4 \times 10^{20} \text{ cm}^{-3}$  boron concentration) to determine an intrinsic room temperature phonon-phonon scattering mean free path. The phonon dispersion model properties ( $C_v = 0.93 \times 10^6 \text{ J m}^{-3} \text{ K}^{-1}$  and  $v = 1804 \text{ m s}^{-1}$ ) from Chen [32] are used to account for the fact that optical phonons contribute negligibly to heat conduction near room temperature, resulting in an intrinsic mean free path estimate of  $\Lambda_{p-p} = 69 \text{ nm}$ , which is combined with the total phonon-grain boundary and phonon-void scattering contribution from Monte Carlo using Matthiessen's rule to calculate thermal conductivity:

$$k = \frac{1}{3} C_v v \left( \frac{1}{\Lambda_{p-p}} + \frac{1}{\Lambda_{GB+voids}} \right)^{-1} \quad (2.10)$$

We note that data for sample T900 are not presented, as WAXS/SAXS scattering data for void size were not obtained.



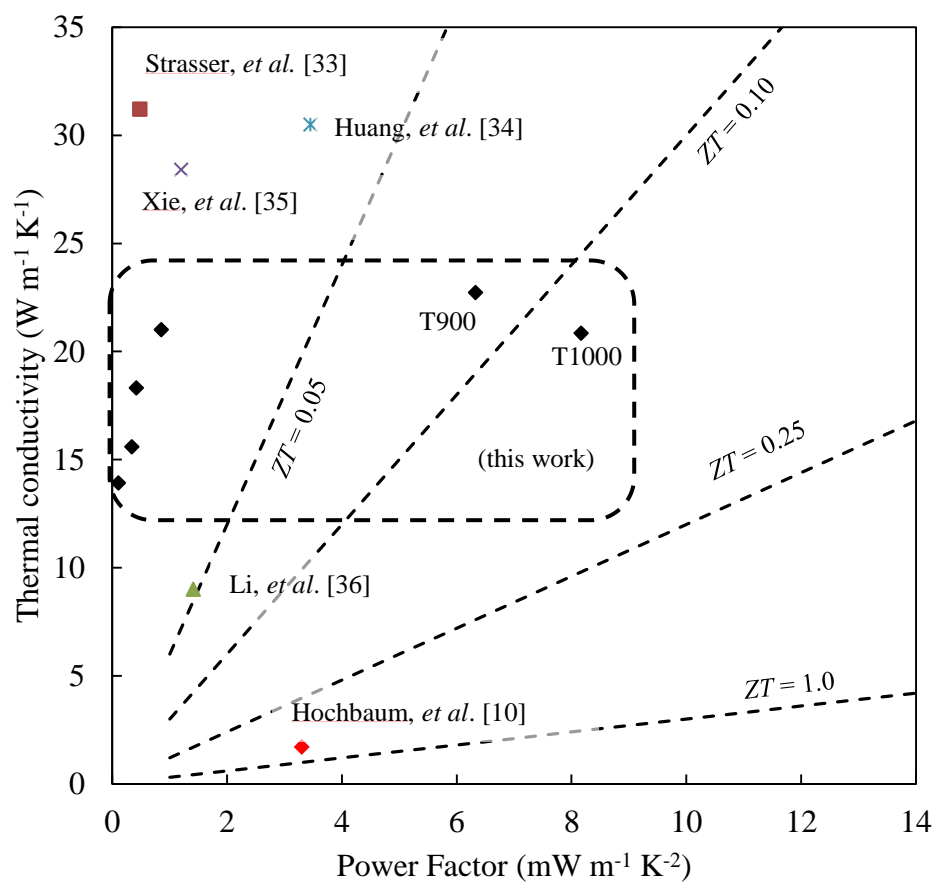


**Figure 2-9.** Comparison of measured thermal conductivity to Matthiessen’s rule and Monte Carlo (MC) models.

Experimental and numerical thermal conductivity data for films undergoing the thermal annealing sequence are plotted in Figure 2-9. A monotonic rise in thermal conductivity as the void distribution trends toward fewer, larger voids in the grain volume is observed in both the numerical and experimental data, although with clearly different slopes. Additional mechanisms thought to contribute to the thermal transport and steeper slope observed in the experimental data include defect evolution at the grain boundaries and precipitation of volumetric boron impurities, though direct data to quantify these contributions were not available. The impact of void morphology on simulated conductivity data, while still present, is less significant under the assumption of smaller lateral grain dimensions (50 nm vs. 80 nm), when grain boundary scattering dominates.

## **2.4 Implications for Thermoelectric Performance and Comparison to Literature**

In Figure 2-10 we compare the results of the present study with reported silicon-based nano-featured thermoelectric materials in the thermal conductivity vs. power factor space. It is not appropriate to extract a true material  $ZT$  from the films of this study considering in-plane power factor and cross-plane thermal conductivity measurements. However, we can estimate a lower bound for in-plane  $ZT$  as the smaller lateral grain size can be reasonably expected to further reduce in-plane thermal transport. Iso- $ZT$  lines for 0.05, 0.10, 0.25, and 1.0 at 300 K are plotted for reference. The films we report sit in a gap region of thermal conductivity between typical thin-film silicon materials [33–35] and high-performance nanowires [10,36] due to a combination of high doping, defects/voids, and modest grain size. Samples T900 and T1000 in particular show strong performance compared to thin film silicon in the thermoelectric literature. Despite no longer benefiting significantly from phonon-void scattering contributions, the jump in thermoelectric power factor and lower thermal conductivity due to high doping levels and small grain structure enhance their position in the  $ZT$  space.



**Figure 2-10.** Comparison of present study experimental results and nano-featured silicon thermoelectric materials from the literature.

## **Chapter 3**

# **Design and Optimization of Microfabricated Thermoelectric Generators**

This section discusses key parameters for the optimization of thermoelectric generators, with special attention given to devices fabricated at the micro-scale. Portions of the information presented in this chapter can also be found in Ref. [37].

### **3.1 Microfabricated Thermoelectric Generators**

Microfabricated thermoelectric generators ( $\mu$ TEGs) are used to produce electrical power for devices, such as wireless sensors, requiring micro-Watts to milli-Watts of power per device. These generators scavenge thermal energy from waste heat sources that have temperature differences or spatial dimensions that are too small for conventional thermodynamic heat engines to effectively utilize. In this domain, only a small fraction of available thermal energy needs to be extracted from the thermal reservoir to achieve a target power output, often without concern for thermal efficiency. In the limit where the heat capacities of heat source and sink are very large, the temperatures of the source and sink are not appreciably perturbed by the small amount of heat drawn through the  $\mu$ TEG system, which is dependent on device configuration (*i.e.* the geometry, interfaces, boundary conditions, etc.). This fixed temperature assumption is an ideality that benefits from the relatively high thermal resistance of a  $\mu$ TEG, compared to larger devices for which local temperature perturbations may be a more present concern [38]. Under a fixed temperature assumption, optimization for either maximum thermal efficiency or maximum power

output will lead to two different devices [39,40]. Since many microfabricated devices, sensors, and actuators have well-defined power and footprint requirements, this work defines and optimizes performance based on electrical power generated by the device rather than thermal efficiency and presents a comprehensive design methodology for microfabricated waste heat scavenging devices.

### 3.1.1 Applications and State-of-Art

The field of  $\mu$ TEGs emerged in the early/mid-1990s, reducing feature sizes to mm and  $\mu$ m following decades of successful use of high-temperature, bulk-scale devices for applications such as spacecraft power generation [41]. Microfabricated devices offer an advantage over traditional bulk-processed devices by allowing for streamlined assembly in semiconductor process lines and direct on-chip integration. One of the first discussions of the use of thermoelectric generators for the recovery of “low-grade” waste heat examined mm-scale devices exposed to temperature sources up to 240 °C [42]. In 1997, Fleurial *et al.* [43] suggested the use of thin-film fabrication methods for “micropower sources” to accommodate the advance in miniaturized systems, particularly for space applications. In the same year, Stordeur and Stark [44] reported on the successful fabrication and testing of a  $\mu$ TEG, produced by thin-film sputtering in a planar pattern followed by dicing and vertical assembly. Fleurial *et al.* [45,46] achieved thicker ( $\sim$ 10-50  $\mu$ m) thermoelectric films deposited by electrodeposition for low-power, high-voltage harvesting of small temperature gradients. In 2004, Böttner *et al.* [47] discussed a novel sandwich-type wafer assembly with interlocking substrates prepared by co-sputtering. Strasser *et al.* [33] prepared and analyzed a CMOS-compatible generator design based on Si and SiGe semiconductors in a design where heat flows laterally in the device. Electrodeposition of bismuth-telluride and nickel-copper devices using polymer molds was reported by Glatz *et al.* [48] to extend the regime of thin film thermoelectric leg lengths, which is a limiting factor in microfabricated devices.

### **3.1.2 Challenges in Microgenerator Design**

While significant progress has been made in fabrication and preliminary demonstration of  $\mu$ TEGs, there has been little attention on the challenge of optimizing these devices for power output. While optimizing  $ZT$  at the materials level has been the focus of much of the thermoelectrics community, these reports may not be complete as the  $\mu$ TEG community strives to improve power generation per unit footprint area for practical applications, a particularly important metric for small thermoelectric modules converting waste heat to electricity. The use of the metric  $ZT$  as an indicator of the quality of thermoelectric generators [41,49–51] may not be appropriate for  $\mu$ TEGs. This quantity encapsulates the operating temperature and three primary material properties contributing to the thermoelectric rate equations into a dimensionless parameter, the so-called thermoelectric figure-of-merit:

$$ZT = \frac{S^2}{\rho k} \left( \frac{T_h + T_c}{2} \right) \quad (3.1)$$

In Equation 3.1,  $S$  is the Seebeck coefficient (units of  $\mu\text{V K}^{-1}$ ),  $\rho$  is the electrical resistivity ( $\Omega \text{ m}$ ),  $k$  is the thermal conductivity ( $\text{W m}^{-1} \text{ K}^{-1}$ ), and  $T_h$  and  $T_c$  are the hot and cold temperatures across the thermoelectric. In reality, an “incompleteness of  $ZT$ ” exists where a single value of  $ZT$  does not uniquely predict power output or provide an absolute roadmap to device optimization due to the many combinations of  $S$ ,  $k$ , and  $\sigma$  that yield a single  $ZT$  value.

The impact of filler material, which surrounds the active thermoelectric material (see Figure 3-1) and may exist as a byproduct of manufacturing or intentionally for mechanical stability, is often overlooked despite observed effects on performance [36]. External thermal resistances (*i.e.* the pathways to heat sources/sinks) play a significant role in the performance of  $\mu$ TEGs, and some attention has been given to these effects [52–54]. However, without the inclusion of realistic filler material effects

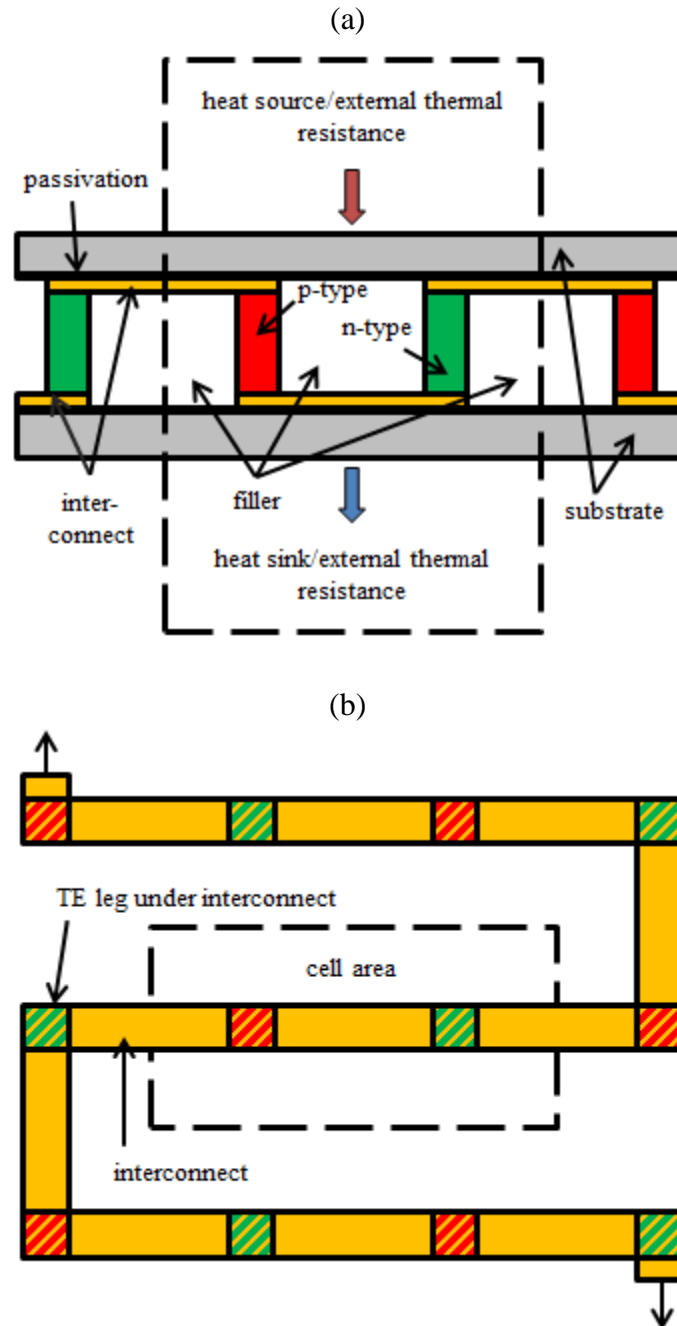
and device design considerations, these analyses are incomplete. Additional factors become important in the realization of a practical generator device, including adjustment of device fill fraction to compensate for fabrication limitations to thermoelectric element length and appropriate selection of number of junctions when accounting for the electrical resistance of interconnects.

The following section presents a comprehensive design methodology for  $\mu$ TEG devices, particularly those harvesting energy from small temperature differences, paying close attention to several parameters that are commonly neglected in the existing literature, such as the effects of fill fraction in combination with different filler materials, limitations and workarounds when restricted to short leg lengths, the impact of the number of thermocouples, and the different contributions of the parameters in the figure of merit  $ZT$  to device performance. Further, a robust closed-form model for the power output of a  $\mu$ TEG is derived, which includes the Peltier effect, external thermal resistances, parasitic resistive losses, fill fraction/filler material, and accounts for variable electric loading.

### 3.2 Numerical Modeling

The analysis presented in this paper considers a thermoelectric generator with heat flowing through the individual thermoelectric elements in parallel and electric current flowing in a serpentine series pattern. Simulations use a thermocouple unit cell that can be repeated to scale up to a full device. The unit cell area and relevant segments of the generator for simulation are illustrated in Figure 3-1.

*DESIGN AND OPTIMIZATION OF MICROFABRICATED THERMOELECTRIC GENERATORS*



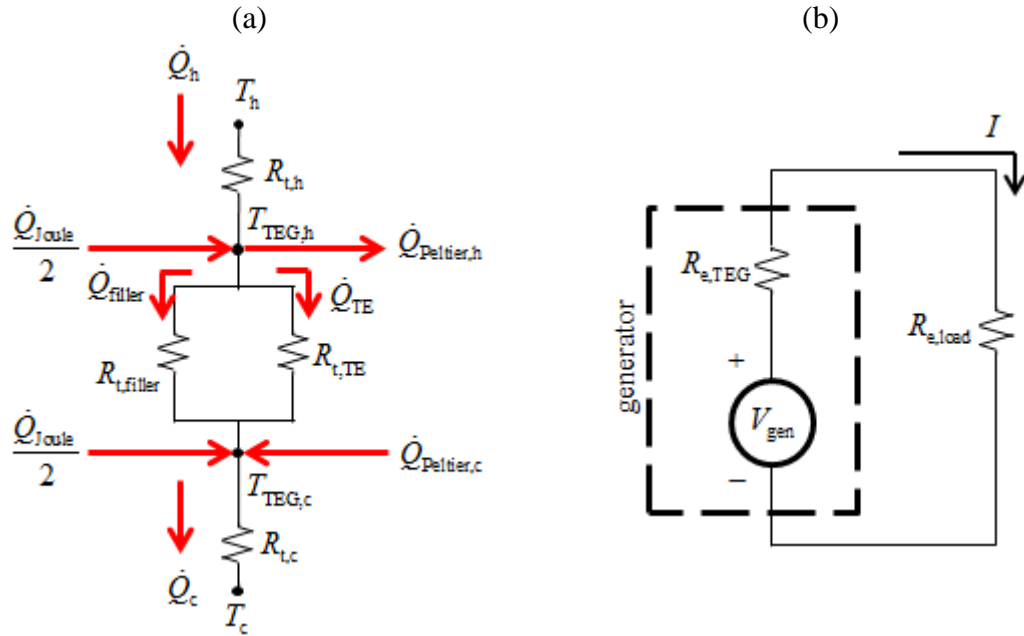
**Figure 3-1.** Diagram of vertically-aligned thermoelectric generator, showing (a) side and (b) top views.

The illustration in Figure 3-1 shows both a side view with heat flowing from one substrate to the other and a top-down view with heat flowing into/out of the page.



### 3.2.1 Reduced-Order Model

A one-dimensional heat transfer model with parallel heat flows is assumed for the vertical structure shown in Figure 3-1, and the thermal and electrical resistance networks are provided in Figure 3-2. For simplicity, we assume that the thin passivation layers and high thermal conductivity metal interconnects in series with relatively long and low-conductivity thermoelectric legs do not contribute significantly to the overall thermal resistance. This assumption is confirmed with 3D finite element analysis.



**Figure 3-2.** (a) One-dimensional thermal and (b) electrical resistance networks used to model thermoelectric generators.

The model accounts for thermal conduction through external thermal resistances  $R_{t,h}$  and  $R_{t,c}$  (e.g. heat sinks/exchangers), substrate resistances, and parallel conduction through the active thermoelectric material and filler material. This model also includes the effects of Joule and Peltier heating. Joule heating ( $\dot{Q}_{Joule}$ ) is volumetric and well-modeled by introducing half of the total heat at each of the hot and cold junctions of

## DESIGN AND OPTIMIZATION OF MICROFABRICATED THERMOELECTRIC GENERATORS

the device [55]. The transfer of heat from the hot junction to the cold junction by the Peltier effect is captured by a removal of heat at the hot end and an addition of heat at the cold end and degrades the performance of thermoelectric devices operating as electric generators. Thomson heat is neglected due to the small temperature gradients encountered in micro-harvesting applications. A nodal energy balance at the hot junction including heat flow from the source ( $\dot{Q}_h$ ), heat flow through the thermoelectric material ( $\dot{Q}_{TE}$ ), heat flow through the filler material ( $\dot{Q}_{filler}$ ), heat removed at the hot junction due to the Peltier effect ( $\dot{Q}_{Peltier,h}$ ), and heat added at the cold junction due to Joule heating ( $\dot{Q}_{Joule}$ ) is given by

$$0 = -\dot{Q}_h + \dot{Q}_{TE} + \dot{Q}_{filler} + \dot{Q}_{Peltier,h} - \frac{\dot{Q}_{Joule}}{2} \quad (3.2a)$$

where:

$$\dot{Q}_h = \frac{T_h - T_{TEG,h}}{R_{t,h}} \quad (3.2b)$$

$$\dot{Q}_{TE} = \frac{T_{TEG,h} - T_{TEG,c}}{R_{t,TE}} \quad (3.2c)$$

$$\dot{Q}_{filler} = \frac{T_{TEG,h} - T_{TEG,c}}{R_{t,filler}} \quad (3.2d)$$

$$\dot{Q}_{Peltier,h} = n_{TC} S_{net} T_{TEG,h} I \quad (3.2e)$$

$$\dot{Q}_{Joule} = I^2 R_{e,TEG} \quad (3.2f)$$

The temperatures of the hot and cold junctions are given by  $T_{TEG,h}$  and  $T_{TEG,c}$ , respectively. The number of thermocouple junctions is expressed by  $n_{TC}$ , and  $S_{net}$  is the net Seebeck coefficient (defined as  $S_{net} = S_p - S_n$ ). The electrical current through and electrical resistance of the generator are  $I$  and  $R_{e,TEG}$ , respectively. The parallel thermal resistances of the thermoelectric material and filler material are given by:

$$R_{t,TE} = \frac{l_{TE}}{k_{TE} A_{total} FF} \quad (3.2g)$$

$$R_{t,filler} = \frac{l_{TE}}{k_{filler} A_{total} (1-FF)} \quad (3.2h)$$

where  $l_{TE}$  is the length (or height) of the each thermoelectric leg,  $k_{TE}$  and  $k_{filler}$  are the respective thermal conductivities of the thermoelectric and filler material,  $FF$  is the filling fraction of active thermoelectric material, and  $A_{total}$  is the device footprint area.

Similarly, we construct an energy balance at the cold junction:

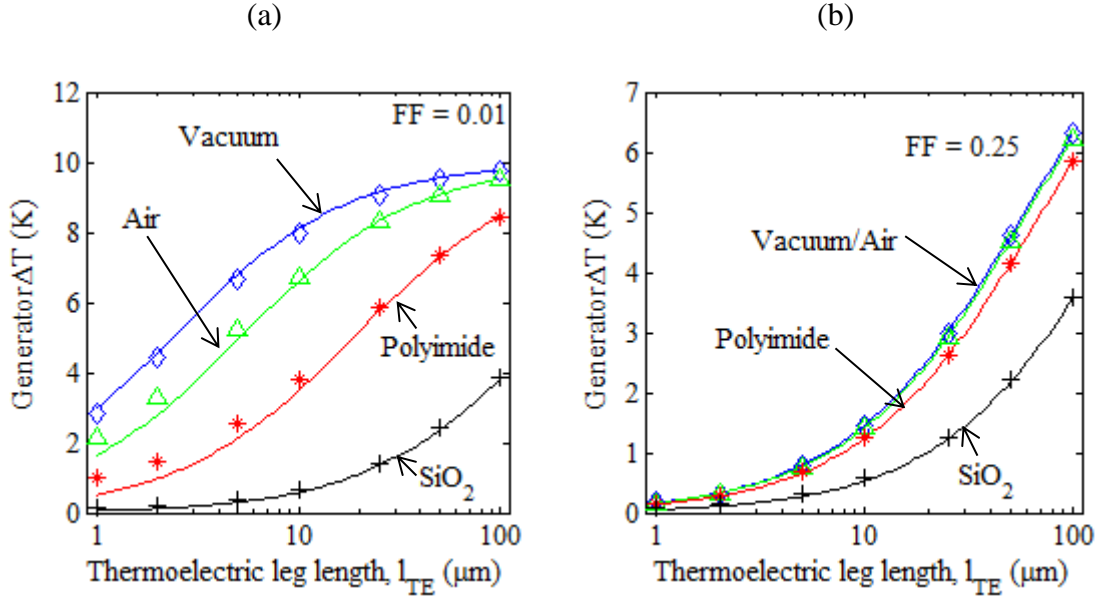
$$0 = \dot{Q}_c - \dot{Q}_{TE} - \dot{Q}_{filler} - \dot{Q}_{Peltier,c} - \frac{\dot{Q}_{Joule}}{2} \quad (3.3a)$$

where:

$$\dot{Q}_c = \frac{T_{TEG,c} - T_c}{R_{t,c}} \quad (3.3b)$$

$$\dot{Q}_{Peltier,c} = n_{TC} S_{net} T_{TEG,c} I \quad (3.3c)$$

The validity of the 1D thermal model (excluding Joule and Peltier contributions) is checked with a 3D finite element simulation in COMSOL Multiphysics. The 3D simulation includes two 100 nm  $Si_3N_4$  passivation layers (implemented first as narrow domain elements and then using the Thin Layer resistance feature with negligible discrepancy) and 1  $\mu m$  tall Au interconnects matched flush to the sides of the thermoelectric legs. The average temperature of the two thermoelectric (TE) legs is calculated at the hot and cold junctions, and the temperature difference is compared to that calculated using the 1D heat transfer approximation. The results are compared in Figure 3-3 for  $FF = 0.01$  and  $0.25$ , and 4 different filler materials (vacuum, air, polyimide, and  $SiO_2$ ).



**Figure 3-3.** Comparison of generator temperature difference calculated by the 1D (lines) and 3D (markers) heat transfer models for (a)  $FF = 0.01$  and (b)  $FF = 0.25$  with different filler materials.

The 1D thermal model neglecting the passivation layers and interconnects shows good agreement with the 3D finite element model. The 1D model begins to deviate from the 3D model for low fill fractions and thermoelectric leg lengths on the order of the interconnect height.

The electric circuit equations are coupled to the thermal model through the junction temperatures  $T_{TEG,h}$  and  $T_{TEG,c}$ , which determine the generated Seebeck voltage  $V_{gen}$ :

$$V_{gen} = n_{TC} S_{net} (T_{TEG,h} - T_{TEG,c}) \quad (3.4)$$

The voltage drops across the generator resistance  $R_{e,TEG}$ , which includes contact and interconnect (IC) resistances, and the connected load resistance  $R_{e,load}$  are then found using voltage divider expressions (see Figure 3-2b):

### CHAPTER 3

$$V_{\text{TEG}} = \frac{R_{\text{e,TEG}}}{R_{\text{e,TEG}} + R_{\text{e,load}}} V_{\text{gen}} \quad (3.5)$$

$$V_{\text{load}} = \frac{R_{\text{e,load}}}{R_{\text{e,TEG}} + R_{\text{e,load}}} V_{\text{gen}} \quad (3.6)$$

The electric current  $I$  is calculated as the generated Seebeck voltage divided by the electrical resistance of the total pathway through generator and load:

$$I = \frac{V_{\text{gen}}}{R_{\text{e,TEG}} + R_{\text{e,load}}} \quad (3.7)$$

The electric power delivered to the load is then calculated using the voltage across the load resistance given by Equation 3.6 to write:

$$P_{\text{load}} = \frac{V_{\text{load}}^2}{R_{\text{e,load}}} = \frac{R_{\text{e,load}} n_{\text{TC}}^2 S_{\text{net}}^2 (T_{\text{TEG,h}} - T_{\text{TEG,c}})^2}{(R_{\text{e,TEG}} + R_{\text{e,load}})^2} \quad (3.8)$$

The electric power and the voltage and current produced by the generator are of primary interest, and the coupled system of Equations 3.2-3.8 requires an iterative solution to obtain the temperatures on the hot and cold active regions of the generator,  $T_{\text{TEG,h}}$  and  $T_{\text{TEG,c}}$ , respectively. The fraction of temperature drop across the thermoelectric versus the total available temperature difference from the reservoirs is less than unity for nonzero external thermal resistances and can be quantified as a temperature efficiency that is useful for device analysis:

$$\eta_{\text{T}} = \frac{T_{\text{TEG,h}} - T_{\text{TEG,c}}}{T_{\text{h}} - T_{\text{c}}} \quad (3.9)$$

### 3.2.2 Closed-Form Temperature Solution

The coupled system described by Equations 3.2-3.8 requires an iterative numerical approach to converge to a solution. However, simplifications can be used to obtain a closed-form solution. One first-order approach [52,56] neglects both the Peltier and Joule heating contributions and calculates the relevant temperature difference from a ratio of thermal resistances analogous to a voltage divider:

$$(T_{\text{TEG,h}} - T_{\text{TEG,c}})_{\text{1st-order}} = \frac{\left( \frac{1}{R_{\text{t,TE}}} + \frac{1}{R_{\text{t,filler}}} \right)^{-1}}{R_{\text{t,h}} + \left( \frac{1}{R_{\text{t,TE}}} + \frac{1}{R_{\text{t,filler}}} \right)^{-1} + R_{\text{t,c}}} (T_{\text{h}} - T_{\text{c}}) \quad (3.10)$$

The resulting relation requires no numerical iteration, but leads to a non-negligible error, on the order of 10%, primarily due to absence of the Peltier heats. We obtain a more accurate closed-form expression by retaining a form of the Peltier heating term. In the domain of small temperature differences the conversion efficiency is very small due to the theoretical limits of heat engine thermal efficiency. This allows us to neglect the effect of Joule heating in Equations 3.2 and 3.3, which is negligible compared to the total heat flow in the device (~3% for a Carnot engine operating between 20 and 30 C). If Equations 3.2 and 3.3 are then added and combined with Equations 3.4 and 3.7, the following equation is produced:

$$\begin{aligned} \frac{T_{\text{h}} - T_{\text{TEG,h}}}{R_{\text{t,h}}} + \frac{T_{\text{TEG,c}} - T_{\text{c}}}{R_{\text{t,c}}} &= 2 \frac{T_{\text{TEG,h}} - T_{\text{TEG,c}}}{R_{\text{t,TEG}}} + 2 \frac{T_{\text{TEG,h}} - T_{\text{TEG,c}}}{R_{\text{t,filler}}} + \dots \\ \frac{n_{\text{TC}}^2 S_{\text{net}}^2 (T_{\text{TEG,h}} - T_{\text{TEG,c}})}{R_{\text{e,load}} + R_{\text{e,TEG}}} (T_{\text{TEG,h}} + T_{\text{TEG,c}}) & \end{aligned} \quad (3.11)$$

For small temperature difference near room temperature, such as seen by microscale generators in waste heat recovery applications, it can be assumed with

reasonable accuracy that  $(T_{\text{TEG,h}} + T_{\text{TEG,c}}) \approx (T_h + T_c)$ , which approximates the Peltier heat contribution in terms of the known reservoir temperatures. These temperatures are assumed constant due to the small amount of heat extracted by a  $\mu\text{TEG}$  compared to the heat capacity of a hot wall or pipe, for example. In a final step, it is assumed that the external thermal resistances  $R_{\text{t,h}}$  and  $R_{\text{t,c}}$  are expressible as an average  $R_{\text{t,ext,avg}}$ . With these steps, a closed-form solution for the temperature difference across the active region of the generator is derived:

$$(T_{\text{TEG,h}} - T_{\text{TEG,c}})_{\text{closed}} = \frac{T_h - T_c}{1 + R_{\text{t,ext,avg}} \left[ \frac{2}{R_{\text{t,TEG}}} + \frac{2}{R_{\text{t,filler}}} + \frac{n^2 S_{\text{net}}^2}{R_{\text{e,load}} + R_{\text{e,TEG}}} (T_h + T_c) \right]} \quad (3.12)$$

The temperature difference calculated in Equation 3.12 can then be used directly in Equation 3.8 to determine electric power delivered to a resistive load. Two limiting cases for Equation 3.12 can be considered to verify physical intuition. First, as  $R_{\text{t,ext,avg}} \rightarrow 0 \text{ K W}^{-1}$ , the case of no thermal resistance between the generator junctions and the thermal reservoirs, the temperature efficiency  $\eta_T \rightarrow 1$ , and the junction temperature difference  $(T_{\text{TEG,h}} - T_{\text{TEG,c}})$  simplifies to the reservoir temperature difference  $(T_h - T_c)$ . Second, as  $R_{\text{t,ext,avg}} \rightarrow \infty \text{ K W}^{-1}$ , the case of external thermal resistances much greater than the generator and filler thermal resistance, the temperature efficiency  $\eta_T \rightarrow 0$  and the junction temperature difference  $(T_{\text{TEG,h}} - T_{\text{TEG,c}})$  approaches 0 K because effectively all of the available temperature difference is dropped across the external resistances.

The closed-form model, Equation 3.12, can be compared quantitatively with the iterative, Equations 3.2-3.3, and 1<sup>st</sup> order, Equation 3.10, models by considering a device with nominal thermophysical properties of thermoelectric material comparable to bismuth telluride compounds, given in Table 3-1. Thermoelectric legs for the model are square in cross-section (side length 15  $\mu\text{m}$ ) with a fill fraction of  $FF = 0.01$ . The fill fraction of vertically-aligned thermoelectric devices is defined to be the fraction of  $A_{\text{total}}$  occupied by active thermoelectric material. For electrical resistance calculations, interconnects are modeled as gold with width equal to the width of the adjacent

# DESIGN AND OPTIMIZATION OF MICROFABRICATED THERMOELECTRIC GENERATORS

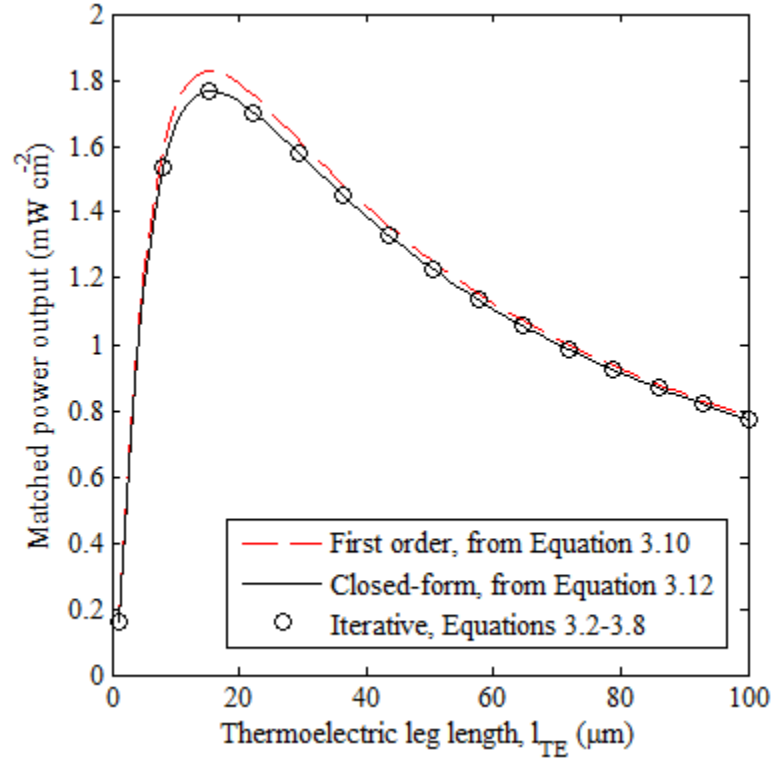
thermoelectric leg, and thickness of 1  $\mu\text{m}$ . Filler material is air with thermal conductivity of  $0.024 \text{ W m}^{-1} \text{ K}^{-1}$  and negligible convective thermal transport inside the module.

**Table 3-1.** Input thermoelectric material parameters for one possible device configuration.

	$S (\mu\text{V K}^{-1})$	$\rho (\Omega \text{ m})$	$k (\text{W m}^{-1} \text{ K}^{-1})$	$ZT @ 300\text{K}$
p-type ( $\sim\text{Sb}_2\text{Te}_3$ )	200	$1 \times 10^{-5}$	2.0	0.6
n-type ( $\sim\text{Bi}_2\text{Te}_3$ )	-200	$1 \times 10^{-5}$	2.0	0.6

The values for  $R_{t,h}$  and  $R_{t,c}$  include thermal resistance through a 525  $\mu\text{m}$ -thick monosilicon substrate as well as an external thermal resistance (*i.e.* heat exchanger) between the substrate and thermal reservoir. The nominal values for these external thermal resistances are  $1 \times 10^{-5} \text{ m}^2 \text{ K W}^{-1}$  to represent conduction from a solid hot-side heat reservoir (*e.g.* hot water pipe) and  $1 \times 10^{-4} \text{ m}^2 \text{ K W}^{-1}$  to represent fin-assisted natural convection to a cold-side reservoir (*e.g.* static air) at ambient conditions. These values are characteristic of a solid bond contact with spreading into a metal surface for the hot side and small commercially-available machined-aluminum fin arrays (approximately  $10 \text{ K W}^{-1}$  total thermal resistance), made area-specific using a nominal thermoelectric device footprint of  $10 \text{ mm}^2$ . The results from the 1D iterative, closed-form, and first order approaches are compared in Figure 3-4, using matched electrical loading conditions, where the load electrical resistance in Figure 3-2b is equal to the internal electrical resistance of the thermoelectric generator.





**Figure 3-4.** Comparison of iterative 1D model (black squares calculated using Equations 3.2-3.8), simplified first-order model (dashed red line calculated using Equations 3.10 and 3.8), and the proposed closed-form model (solid black line calculated using Equations 3.12 and 3.8).

The proposed closed-form solution shows excellent agreement with the iterative model and a noticeable improvement over the 1st order model, particularly near maximum power conditions, where these devices are intended to operate.

### 3.3 Device Design Considerations

Nominal parameters used to produce simulation data are given in Table 3-2. We note that in the domain of microscale generators, electrical contact resistance in the series electrical pathway is significant and included, while thermal contact resistances in the parallel heat pathway are not and ignored.

**Table 3-2.** Nominal system and material values used for parametric simulations.

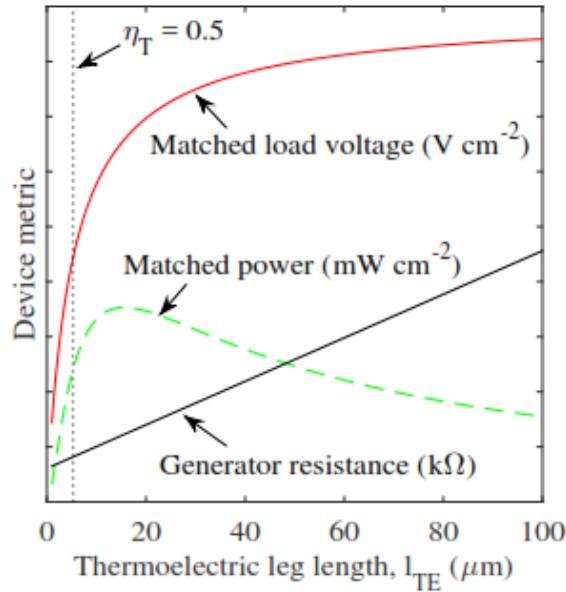
Parameter	Nominal Value
Net Seebeck coefficient, $S_{\text{net}}$	400 $\mu\text{V K}^{-1}$
Thermoelectric material thermal conductivity, $k_{\text{TE}}$	2 $\text{W m}^{-1} \text{K}^{-1}$
Thermoelectric material electrical resistivity, $\rho_{\text{TE}}$	$1.0 \times 10^{-5} \Omega \text{m}$
Semiconductor/metal electrical contact resistance, $\rho_{\text{contact}}$	$5.0 \times 10^{-11} \Omega \text{m}^2$ [48,57]
Cold reservoir temperature, $T_{\text{c}}$	293.15 K
Hot reservoir temperature, $T_{\text{h}}$	303.15 K
Total device area, $A_{\text{total}}$	$1 \times 10^{-5} \text{m}^2$
Individual leg cross-sectional area, $A_{\text{leg}}$	$2.25 \times 10^{-10} \text{m}^2$
Au interconnect thickness, $t_{\text{IC}}$	1 $\mu\text{m}$
Area-specific thermal resistance to heat source, $R''_{\text{t,h}}$	$1 \times 10^{-5} \text{m}^2 \text{K W}^{-1}$
Area-specific thermal resistance to heat sink, $R''_{\text{t,c}}$	$1 \times 10^{-4} \text{m}^2 \text{K W}^{-1}$
Silicon substrate thickness	525 $\mu\text{m}$
$\text{Si}_3\text{N}_4$ passivation thickness	100 nm

Proper design of a thermoelectric generator for maximum power output relies on optimization of thermal resistance versus electrical resistance. To maximize electrical power from the generator, the thermal resistance of the active thermoelectric layer should be comparable to that of any inactive layers such as substrates and heat sinks. Increasing the ratio  $R_{\text{t,TEG}} / (R_{\text{t,ext,h}} + R_{\text{t,ext,c}})$  leads to a higher temperature efficiency, initially increasing the power through the  $(T_{\text{TEG,h}} - T_{\text{TEG,c}})$  term in Equation 3.8. However, the means of increasing this thermal resistance geometrically (*i.e.* by increasing leg length or decreasing leg cross-section) also increase the electrical resistance, which increases  $R_{\text{e,TEG}}$ . With all other parameters remaining constant,

power output is maximized for a specific value of leg length or a specific value of fill fraction.

### 3.3.1 Thermoelectric Element Length

Changing the length of each thermoelectric element is a straightforward way to adjust the thermal and electrical resistance. Under fixed reservoir temperature conditions, an increase in leg length at first rapidly increases the temperature drop across the thermoelectric layer before the rate of change slows and asymptotically approaches the reservoir temperature difference ( $\eta_T \rightarrow 1$ ). In contrast, the electrical resistance continues to increase linearly with increasing leg length. These competing effects lead to a maximum, where we find an initial rise in power output due to rapidly increasing thermal resistance for short leg lengths followed by a decrease in power output due to the continuing increase in electrical resistance with diminishing benefits in thermal resistance.

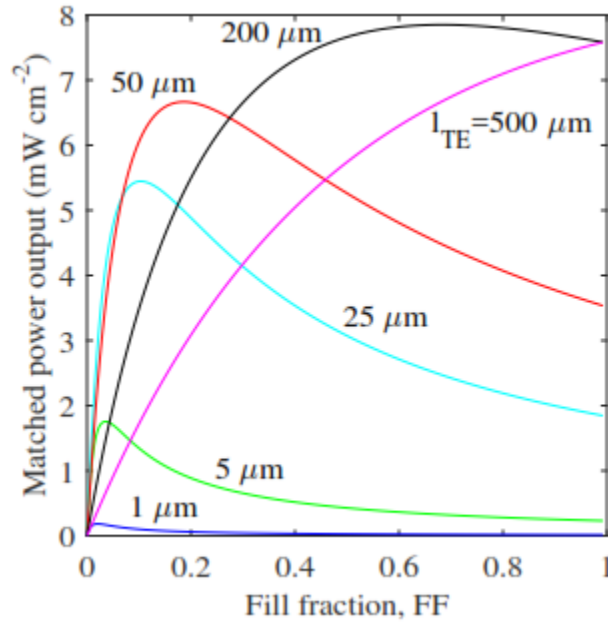


**Figure 3-5.** Plot of matched load voltage, load power, and device electrical resistance trends vs. thermoelectric leg length.

The competing temperature and electrical resistance effects are shown in Figure 3-5. In an ideal system, the maximum matched power is reached when half of the available reservoir temperature difference occurs across the thermoelectric layer ( $\eta_T = 0.5$ ). However, when parasitic losses such as interconnect electrical resistance are included as they are here, the target fractional temperature difference  $\eta_T$  changes, and the maximum power condition does in fact occur at a longer leg length than the  $\eta_T = 0.5$  condition resulting in  $\eta_{T,\max \text{ power}} > 0.5$ . This observation is discussed in a later section of this work.

### **3.3.2 Fill Fraction**

The fabrication method imposes limits on maximum attainable leg length, particularly in the domain of microdevices constructed using bottom-up processes like sputtering or electrodeposition. This poses a constraint on the maximum thermal resistance that can be attained by simply extending the thermoelectric element. The fill fraction can be used to compensate for this limitation. While a very high fill fraction may seem desirable for efficient use of device real estate, it will be shown here that it is not desirable for power output except for very long elements. In fact, when element lengths are limited to  $\sim 1\text{-}10 \mu\text{m}$  as is common with current thin film technology, optimal fill fractions are very low ( $< 10\%$ ).



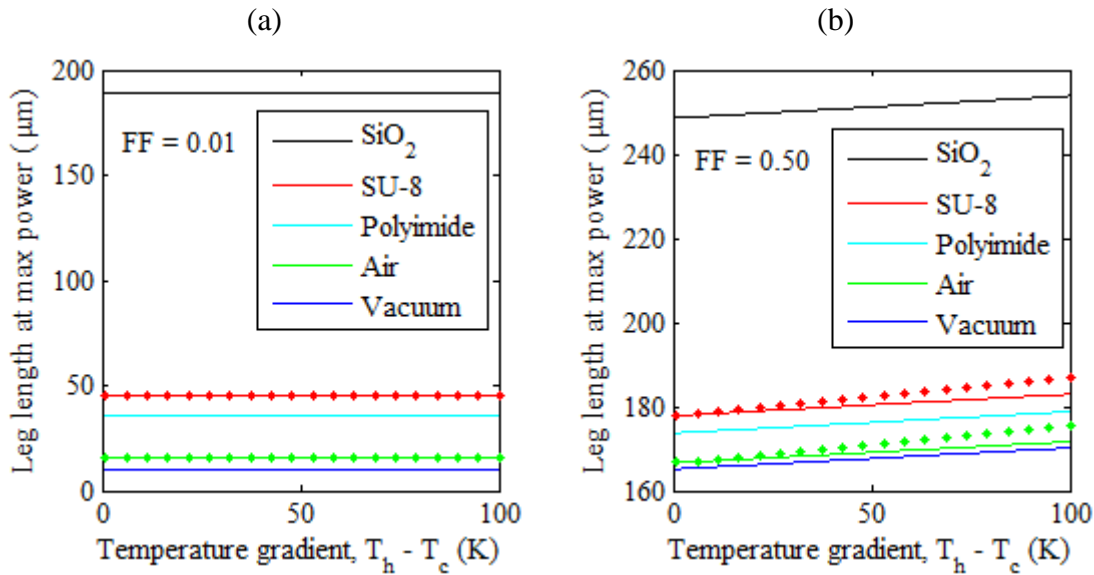
**Figure 3-6.** Matched power per-unit-area vs. fill fraction for different thermoelectric element lengths, using the results of the closed-form solution from Equation 3.12.

The impact of thermoelectric leg length and device fill fraction (varied by changing  $n_{TC}$  with constant element cross section) on power output is illustrated in Figure 3-6. The data show that a maximum power output exists at some fill fraction for a fixed leg length, and that for very short leg lengths, this optimum fill fraction approaches zero. At very long leg lengths, the maximum would appear to occur for  $FF > 1$ , which is non-physical. The thermal resistance due to the thermoelectric under these conditions is too large to reach the maximum power condition with any fill fraction. This motivates the thin-film fabrication approach, as optimal leg lengths for achievable fill fractions may be much shorter than what is possible with bulk machining processes. As seen in Figure 3-6, the maximum attainable power output occurs when higher  $FF$  is used in combination with longer leg length, as long as their combined effect on thermal resistance remains optimal. It is important to note here that the maximum power output for each leg length would be identical, though still occurring for different fill fractions, if electrical losses due to the interconnects and thermal shunting due to the filler material were neglected. It will be shown that

## DESIGN AND OPTIMIZATION OF MICROFABRICATED THERMOELECTRIC GENERATORS

increasing fill fraction by increasing the number of thermocouples reduces the parasitic effect of non-ideal interconnects.

Fill fraction also has an effect on the sensitivity of the optimal leg length to the reservoir temperature gradient. Increasing the fill fraction leads to a longer optimal leg length, as shown in Figure 3-6, and at this leg length, a larger electric power generation. The resulting larger Peltier heats diminish the steady state junction temperature difference, and a longer leg length must be reached to compensate. This effect is shown for two fill fractions, 0.01 and 0.50, in Figure 3-7. The plots also show an increasing error with increased temperature gradient at higher fill fractions due to the approximation made for the Peltier heat contribution in the closed-form equation, but results in only a 2.3% difference in calculated optimal leg length for air filler, 50% fill fraction, and 100 K available reservoir temperature difference.

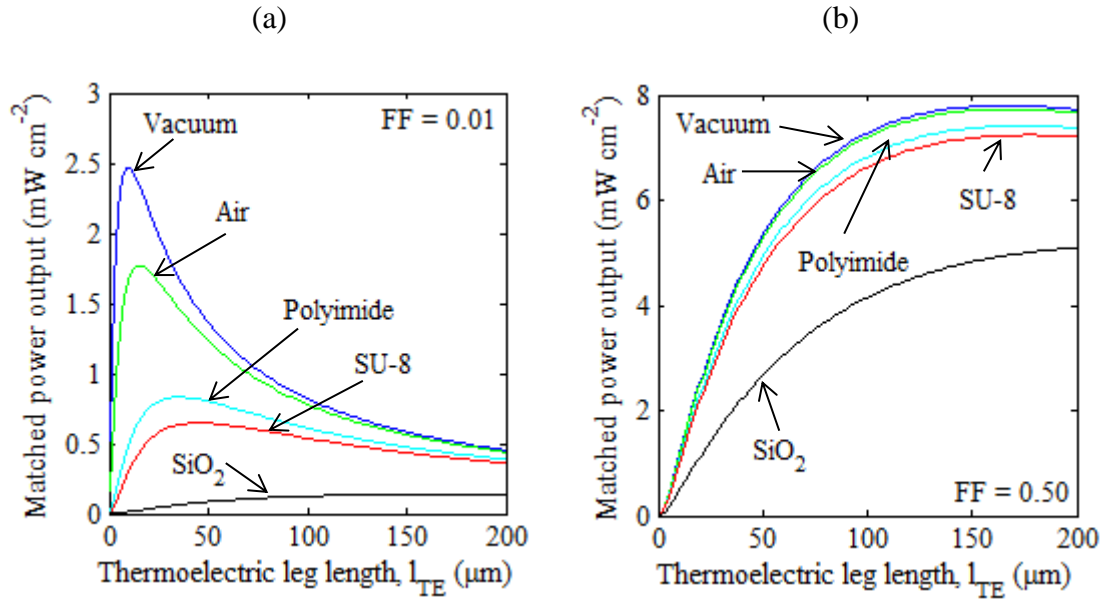


**Figure 3-7.** Dependence of optimal leg length on reservoir temperature gradient for fill fractions of (a) 0.01 and (b) 0.50. Solid lines utilized the derived closed-form model, while dotted lines calculated using the full iterative 1D model are given for accuracy comparison.

If the Peltier heat contribution is removed from the equations, the optimal leg length is independent of temperature difference at any fill fraction. For significant temperature differences across the thermoelectric material, temperature-dependent properties will become important and further impact this relationship.

### 3.3.3 Filler Material

When optimization leads to a very low fill fraction, the thermal properties of the filler material become critically important as the relatively large cross-sectional area may create a significant thermal shunt and reduce the temperature drop across the thermoelectric elements. The ideal filler material should have low thermal conductivity, considered here with a limiting case of vacuum ( $k=0.0001 \text{ W m}^{-1} \text{ K}$  from first-order kinetic theory calculations for air at 1 Pa, 300 K, and a mean free path size-limiting dimension of  $\sim 100 \text{ }\mu\text{m}$ ). In a real device this is not always a practical option as preservation of vacuum conditions means carefully sealing a  $\mu\text{m}$ -scale structure and adding a competing thermal shunt through the seal. Air ( $k=0.024 \text{ W m}^{-1} \text{ K}^{-1}$ ) is a simple option, but oxidation can be a concern and it does not provide structural support during fabrication or operation. Polymers with low thermal conductivity such as polyimide ( $k=0.14 \text{ W m}^{-1} \text{ K}^{-1}$ ) and SU-8 ( $k=0.208 \text{ W m}^{-1} \text{ K}^{-1}$ ) [48,56] have been used in an attempt to add structural integrity while minimizing thermal shunting, as opposed to the use of  $\text{SiO}_2$  ( $k=1.38 \text{ W m}^{-1} \text{ K}^{-1}$ ) [36] which has a thermal conductivity comparable to bismuth telluride thermoelectric material.



**Figure 3-8.** Plot of matched power vs. leg length for (a)  $FF = 0.01$  and (b)  $FF = 0.50$  assuming different filler materials.

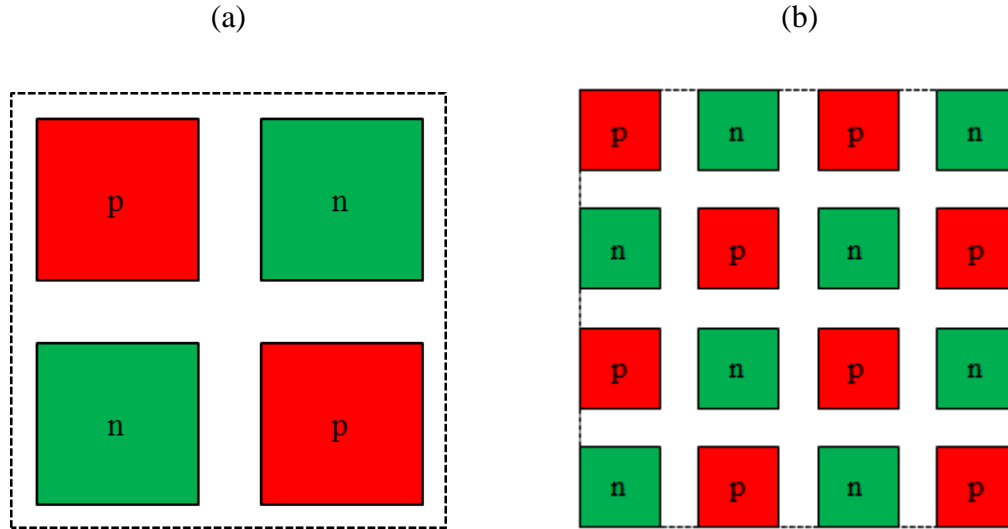
Matched power per unit area vs. thermoelectric leg length is shown in Figure 3-8a and b for  $FF = 0.01$  and  $FF = 0.50$ , respectively, and a variety of candidate filler materials. Each curve shows the same general trend: maximum matched power decreases and occurs at longer leg lengths with increasing filler thermal conductivity. With a more prominent thermal shunt (or large thermal gradients combined with moderate-to-high fill fractions), a longer leg length must be attained to reach the optimal temperature drop across the thermoelectric. This increased leg length increases electrical resistance and decreases power output. When the fill fraction is increased, two primary effects are seen. First, the impact of the specific filler material becomes less significant, and in fact, vacuum and air show nearly identical power curves at 0.50 fill fraction. This is simply due to the fact that there is less filler material, and its presence becomes negligible as  $FF \rightarrow 1$ . Second, higher maximum matched powers are reached, but at longer leg lengths. The reason that different maximum power outputs are reached is due to the reduction in parasitic losses, both



thermal losses from a smaller thermal shunt and electrical losses from the interconnects. For low fill fractions, the thermal resistance is very high and the fraction of reservoir temperature difference dropped across the thermoelectric is large at short leg lengths. Hence, the electrical resistance due to the legs is relatively small, and parasitic losses through the interconnects contribute significantly. When fill fraction increases, the thermal resistance decreases, and a longer leg length must be reached to force the optimal temperature drop. The presence of a filler material with nonzero thermal conductivity will reduce the parallel thermal resistance.

### 3.3.4 Number of Thermocouples

Another design consideration is the selection of the number of thermocouples. The fill fraction is non-unique in that the total area occupied by thermoelectric material depends on both the number of legs and the cross-sectional area of each leg. Therefore multiple combinations of thermocouple number density and individual leg cross-section will result in the same fill fraction, as illustrated in Figure 3-9.



**Figure 3-9.** Configuration with (a)  $n_{TC} = 2$  and (b)  $n_{TC} = 8$  each resulting in the same fill fraction, with different numbers of thermocouples and leg cross-section.

# DESIGN AND OPTIMIZATION OF MICROFABRICATED THERMOELECTRIC GENERATORS

Under ideal conditions (*i.e.* no parasitic thermal or electrical losses), matched power output will be identical for any combination of thermocouple count and leg cross-section which results in the same fill fraction for the same total area. Beginning with the definition of fill fraction as the ratio of thermoelectric material cross sectional area to total footprint:

$$FF = \frac{2n_{TC}A_{leg}}{A_{total}} \rightarrow A_{leg} = \frac{A_{total}FF}{2n_{TC}} \quad (3.13a)$$

Under matched loading conditions, the voltages dropped across the generator and the load resistance are equivalent:

$$V_{matched} = \frac{n_{TC}S_{net}(T_{TEG,h} - T_{TEG,c})}{2} \quad (3.14b)$$

The electrical resistance of the series of thermoelectric elements not accounting for parasitic interconnect or contact resistance, and therefore the load for matched loading conditions, can be related to the fill fraction  $FF$ :

$$R_e = 2n_{TC}\rho_{TE} \frac{l_{TE}}{A_{leg}} = 4n_{TC}^2 \frac{\rho_{TE}l_{TE}}{A_{total}FF} \quad (3.14c)$$

We then calculate the power delivered to the load using Equations 3.14b and c:

$$P_{matched} = \frac{V_{matched}^2}{R_e} = \frac{A_{total}S_{net}^2FF(T_{TEG,h} - T_{TEG,c})^2}{16\rho_{TE}l_{TE}} \quad (3.14d)$$

With fill fraction constant, the thermal resistance is unchanged. The Peltier and Joule heating terms are the only remaining parameters in the heat balance which could affect the matched power calculation. The electrical current in terms of the number of thermocouples  $n_{TC}$  is:

$$I = \frac{V_{matched}}{R_e} = \frac{A_{total}S_{net}FF(T_{TEG,h} - T_{TEG,c})}{8n_{TC}\rho_{TE}l_{TE}} \quad (3.14a)$$

The Peltier heating contributions at the hot and cold junctions are dependent on fill fraction  $FF$ , but independent of the number of thermocouples  $n_{TC}$ :

$$\dot{Q}_{\text{Peltier,h}} = -n_{TC} S_{\text{net}} I T_{\text{TEG,h}} = \frac{-T_{\text{TEG,h}} A_{\text{total}} S_{\text{net}}^2 FF (T_{\text{TEG,h}} - T_{\text{TEG,c}})}{8\rho_{\text{TE}} l_{\text{TE}}} \quad (3.15b)$$

$$\dot{Q}_{\text{Peltier,c}} = \frac{T_{\text{TEG,c}} A_{\text{total}} S_{\text{net}}^2 FF (T_{\text{TEG,h}} - T_{\text{TEG,c}})}{8\rho_{\text{TE}} l_{\text{TE}}} \quad (3.15c)$$

Under matched electrical loading, the power delivered to the load is equivalent to the power dissipated in the generator by Joule heating.

For matched load conditions and constant total area, the heat balance equations will not change for any combination of thermocouple number and leg cross-section that gives the same fill fraction. In the absence of parasitic losses, this property can be used to design the generator for a desired voltage output or electrical resistance. Increasing the number of thermocouples should be the preferred approach to reach a target load voltage when expected source/sink temperatures are known, as voltage boost circuits may result in significant electrical conversion penalties.

$$n_{TC} = \frac{V_{\text{gen,desired}}}{S_{\text{net}} (T_{\text{TEG,h}} - T_{\text{TEG,c}})} \quad (3.15)$$

If parasitic losses are considered, particularly due to electrical resistance over the interconnect length between each thermoelectric element and contact resistance at the semiconductor-metal junctions, the power output may vary with different combinations of element area and number of thermocouples. The electrical resistance along total length of all interconnects within the device is derived geometrically as:

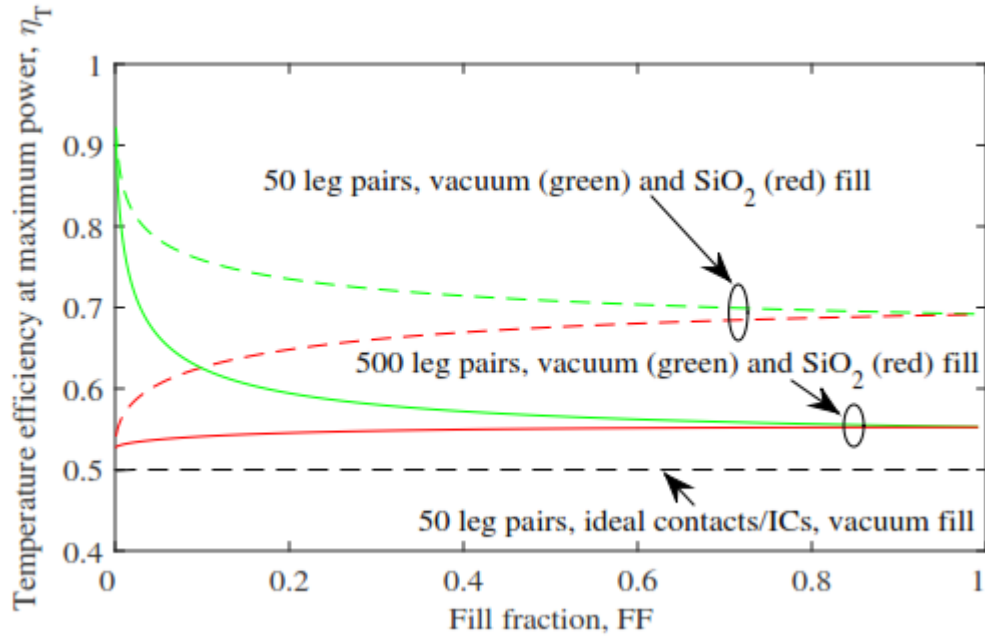
$$R_{\text{e,total,IC}} = 2n_{TC} \rho_{\text{IC}} \frac{\sqrt{\frac{A_{\text{TE}}}{FF}} + \sqrt{A_{\text{TE}}}}{t_{\text{IC}} \sqrt{A_{\text{TE}}}} \quad (3.16a)$$

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Utilizing the generator electrical resistance from Equation 3.14c and calculating the ratio of parasitic to generator electrical resistance:

$$\begin{aligned} \frac{R_{e,\text{total,IC}} + R_{e,\text{total,contact}}}{R_{e,\text{total,TE}}} &= \frac{\rho_{\text{IC}} \frac{\sqrt{\frac{1}{FF}} + 1}{t_{\text{IC}}} + 2 \frac{\rho_{\text{contact}}}{A_{\text{leg}}}}{\rho_{\text{TE}} \frac{l_{\text{TE}}}{A_{\text{leg}}}} \\ &= \frac{A_{\text{total}} FF \rho_{\text{IC}} \left( \sqrt{\frac{1}{FF}} + 1 \right)}{2 n_{\text{TC}} \rho_{\text{TE}} t_{\text{IC}} l_{\text{TE}}} + 2 \frac{\rho_{\text{contact}}}{\rho_{\text{TE}} l_{\text{TE}}} \end{aligned} \quad (3.17b)$$

Equation 3.17b shows that when keeping fill fraction constant the parasitic electrical resistance of the interconnects and semiconductor/metal junctions relative to the resistance of active thermoelectric material is related to the inverse of the number of thermocouples. Once the fill fraction has been chosen for optimal thermal resistance, it is beneficial to utilize many thermocouples with smaller cross-sectional area. This is typically convenient as increasing the number of thermocouples will increase the output Seebeck voltage from the device. The legs should also be as long as possible to minimize the relative impact of contact resistance.



**Figure 3-10.** Temperature efficiency at maximum matched power output vs. fill fraction, where fill fraction is adjusted by changing the area of thermoelectric elements with constant  $\eta_{TC}$  and  $t_{IC}$  is the interconnect thickness (or height). At each fill fraction value, the thermoelectric leg length  $l_{TE}$  is adjusted to reach maximum matched power.

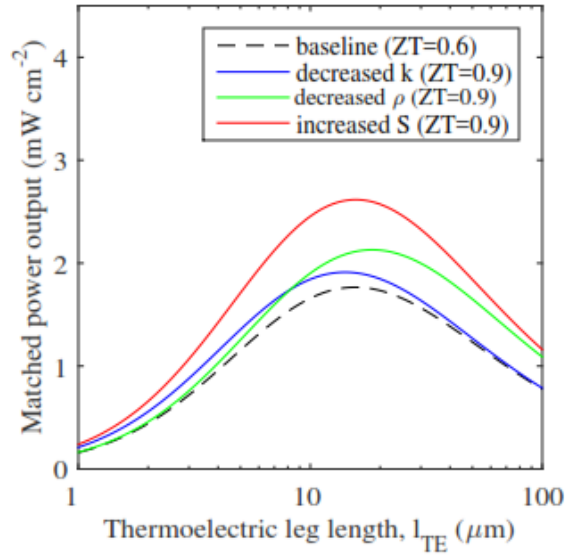
The required temperature efficiency for maximum matched power versus fill fraction is shown in Figure 3-10 for different numbers of thermoelectric leg pairs and filler materials in a  $10 \text{ mm}^2$  footprint. In the idealized case of interconnects with infinite electrical conductance, no electrical contact resistance, and negligible parasitic thermal losses, the optimal temperature drop is always half of the available temperature difference from the thermal reservoirs, as discussed in the literature [53]. When parasitic losses are included, a larger thermal resistance (*i.e.* longer leg length) must be reached to compensate. Furthermore, the required temperature efficiency for maximum matched power is significantly higher than the ideal temperature efficiency when the thermal conductivity of the filler material is very low. This demonstrates a weakness of the vast majority of previous system analyses, which not only neglect the impact of interconnect and contact resistance but assume no contribution from the

filler material, (*i.e.* assuming no parasitic interconnect resistance and the case for which this resistance is most significant). The concavity of the curve depends on the ratio of thermal resistance of the filler region to that of the active thermoelectric elements. If the filler material has very low conductivity, then the thermal shunt through filler material is very small even at low fill fractions, and it is beneficial to have a higher fraction of the available temperature difference across the active thermoelectric materials. Conversely, for high filler material conductivities there is a significant thermal shunt through the filler region, particularly at low fill fractions. In this case it is less desirable to have a large fraction of the available temperature difference dropped across the filler/thermoelectric.

The varying optimal temperature efficiency is a factor of the parasitic loss introduced by the interconnect electrical resistance since the geometry (*e.g.* leg length, fill fraction, etc.) must be altered to give a larger temperature difference, and the resulting increased Seebeck voltage compensates for the additional voltage drops through the series circuit. Inclusion of the Peltier heat contribution also affects the optimal temperature efficiency, although less significantly. If it is neglected as in the first order approximation [52,56], the optimal temperature efficiency is even higher, as that temperature-dependent loss is no longer contributing to the thermal equation.

### **3.4 Incompleteness of $ZT$**

Many analyses suggest that the magnitude of the parameter  $ZT$ , regardless of its composition, is the ultimate rule to device performance. However, due to the optimization balance of thermal and electrical resistance and the concurrent presence of thermal and electrical conductivity in  $Z$ , the optimal device design will be different depending on the ratio of these parameters even for identical values of  $Z$ .



**Figure 3-11.** Power vs. leg length curves calculated using closed-form solution for three different parameter combinations giving the same value of  $ZT$  (0.9) at room temperature.

**Table 3-3.** Maximum matched power and corresponding TE element leg length for a 50% increase in  $ZT$  by modifying each parameter of  $Z$  individually.

$k_{TE}$ [W m <sup>-1</sup> K <sup>-1</sup> ]	$\rho_{TE}$ [Ω m]	$S_{net}$ [μV K <sup>-1</sup> ]	$ZT$ @ 300 K [-]	$P_{matched,max}$ [mW cm <sup>-2</sup> ]	$l_{TE,max}$ [μm]
1.325	$1 \times 10^{-5}$	400	0.9	1.91	14.1
2	$6.63 \times 10^{-6}$	400	0.9	2.13	18.5
2	$1 \times 10^{-5}$	491	0.9	2.62	15.7

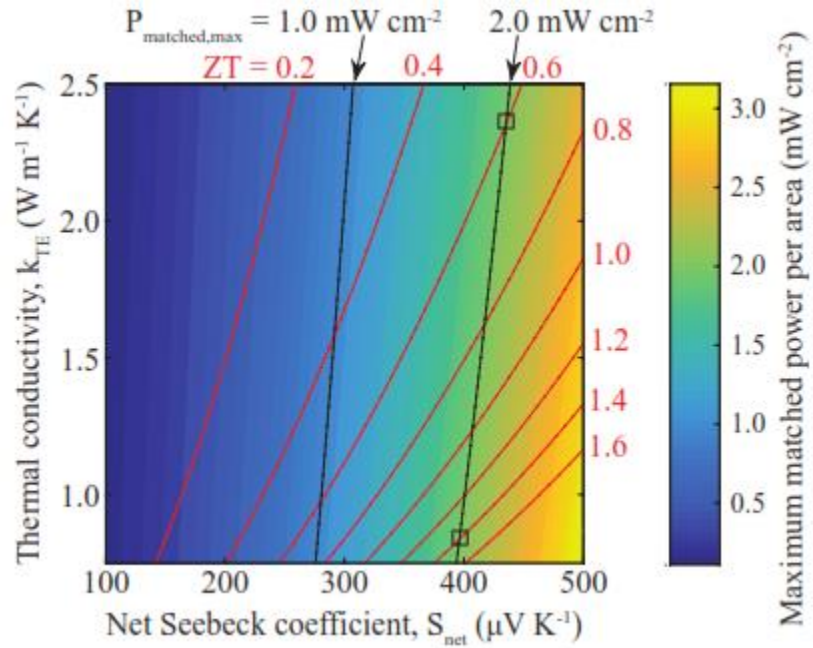
The data in Figure 3-11 and Table 3-3 reveal key points to consider for thermoelectric device design and materials selection. First, the tuning of individual material parameters does not give equivalent device performance, even if they result in the same  $ZT$ . This is due to the competing interaction between thermal and electrical resistance and how they differ according to device design. Second, depending on the attainable film thickness, it may be beneficial to optimize one parameter over another, if possible. While increasing the Seebeck coefficient consistently increases the performance in this example more than changes in  $k$  or  $\rho$  for a given design, if the leg

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lengths are very short (*e.g.* less than about 5  $\mu\text{m}$  in Figure 3-11 it is better to reduce thermal conductivity than to increase electrical conductivity. If longer leg lengths are attainable, the opposite is true. Finally, the optimization of the different parameters can lead to a shift in the optimal thermoelectric leg length. While increasing  $S$  does not alter the condition of maximum matched power, a decrease in  $k$  results in a decreased optimal leg length. This is because the thermal resistance of the device is increased and the ideal temperature drop across the thermoelectric elements can be achieved without adding increased electrical resistance. Conversely, when the device is optimized by increasing electrical conductivity the leg length at maximum matched power is increased. This is because a longer leg length can be reached to realize an optimal temperature drop before added electrical resistance from increased leg length becomes dominant.

These trends become even more impactful when examined in multi-parameter space. A contour plot of maximum matched power for varying thermal conductivity and net Seebeck coefficient is given in Figure 3-12. Electrical resistivity and fill fraction each remain fixed to nominal values, and the leg length is adjusted at each data point to maximize the matched power output. Iso- $ZT$  lines are shown in red, while two isopower lines are provided in black indicating 1.0 and 2.0  $\text{mW cm}^{-2}$ . As one example from this plot, the same maximum matched power of 2.0  $\text{mW cm}^{-2}$  can be reached in a device with  $ZT$  values of 0.6 and 1.4 within this parametric space. The variable system parameters for each point (indicated with a black box marker) are  $S_{\text{net}} = 435.4 \mu\text{V K}^{-1}$ ,  $k_{\text{TE}} = 2.36 \text{ W m}^{-1} \text{ K}^{-1}$ ,  $l_{\text{TE,max}} = 16.4 \mu\text{m}$  ( $ZT = 0.5987$ ), and  $S_{\text{net}} = 396.0 \mu\text{V K}^{-1}$ ,  $k_{\text{TE}} = 0.822 \text{ W m}^{-1} \text{ K}^{-1}$ ,  $l_{\text{TE,max}} = 13.0 \mu\text{m}$  ( $ZT = 1.422$ ).





**Figure 3-12.** Contour plot of maximum matched power per area for ranges of thermal conductivity and net Seebeck coefficient.  $ZT$  values are included as red isolines for reference, and two black isopower lines are included at  $1.0$  and  $2.0 mW cm^{-2}$ .

These findings are critical for device design decisions since a review of thermoelectric literature reveals an abundance of focus on tuning only  $ZT$  values for material and device performance.

# **Chapter 4**

## **Prototyping and Characterization of Microfabricated Thermoelectric Generators**

This chapter presents a discussion of common measurement techniques for thermoelectric devices, as well as the results from the performance characterization of fabricated prototype microgenerators.

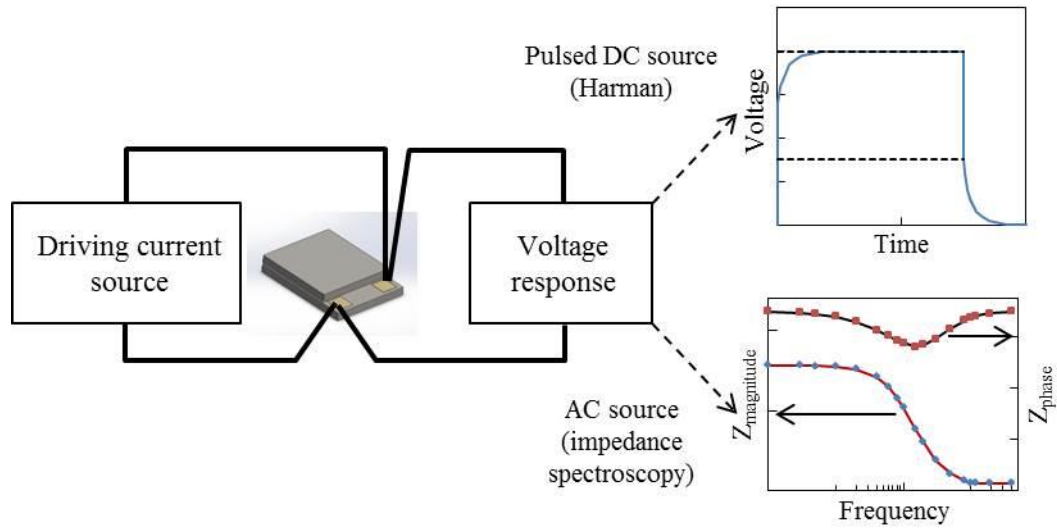
### **4.1 Characterization Techniques for Thermoelectric Devices**

Since thermoelectric devices act as transducers for both electrical and thermal stimuli, useful information can be extracted about the performance characteristics of the device by driving it with either a heat flow or an electrical current and measuring various responses in the system. What follows is a brief review of different techniques found in the literature for characterizing thermoelectric generators, broadly categorized into “electrical” and “thermal” measurement methods, with the recognition that electrical and thermal signals are inherently coupled in thermoelectric devices.

#### **4.1.1 Characterization by Electrical Measurement Methods**

A technique also known as the “ $ZT$  meter” or “Harman method” was developed in 1958 by Harman [58] initially for bulk thermoelectric materials, although it has been extended with success to the characterization of thermoelectric modules in subsequent works [59]. In principle, if a DC signal  $I$  is applied to a material or device of resistance

$R$ , a DC voltage of  $IR$  will develop across the device. With current flow, Peltier heating or cooling will also be acting at any junctions, establishing a temperature gradient, which produces an additional voltage rise due to the Seebeck effect. If the electrical time constant is much smaller than the thermal time constant, the current can be shut off and a decay in Seebeck voltage due to the residual thermal gradient from Peltier heating can be measured. With various assumptions, a relationship for  $ZT$  can be derived using the voltage contributions from Ohm's law and from the Seebeck effect. Techniques using AC signals have also been developed and demonstrated for thermoelectric modules. Downey *et al.* [60] reported the use of impedance spectroscopy for bulk thermoelectric generators using an AC voltage source and lock-in amplifiers. The complex impedance was fit to a lumped capacitor  $RC$  model to extract information about the thermal resistance, capacitance, and electrical resistance of the device. Later, De Marchi and Giaretto [61,62] suggested corrections to complex impedance analyses for thermoelectric generators to account for an additional pole in the transfer function related to a  $f^{1/2}$  slow decay from heat diffusion.

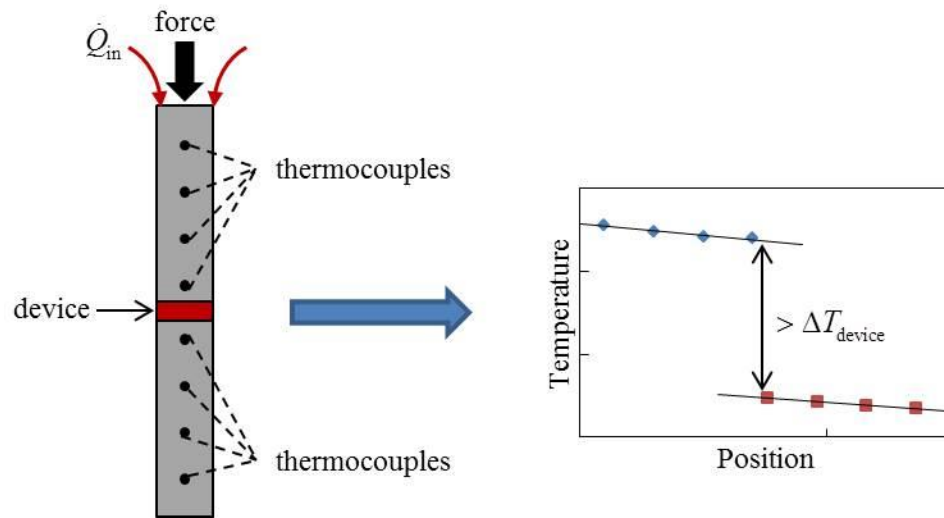


**Figure 4-1.** Schematic of driving and response signal components and characteristic output for Harman method and impedance spectroscopy techniques.

Electrical techniques such as the “ $ZT$  meter” can be useful in offering a lumped dimensionless figure of merit through which to make general comparisons between devices. However, the results of Chapter 3 indicate that evaluating a thermoelectric module, and particularly a microscale generator, by the traditional figure of merit may be ill-advised. Additionally, these techniques do not provide direct information about the relationship between applied thermal gradients and electrical power generation.

#### **4.1.2 Characterization by Thermal Measurement Methods**

A more philosophically-straightforward approach to characterization of thermoelectric generators involves applying a known steady-state thermal gradient to the device and measuring the resulting power output. Traditional techniques have involved variations on the use of a stacked heat delivery apparatus with embedded thermocouples [48,63–65]. In this approach, a device is placed in contact with a heat source and sink (see Figure 4-2). The most conservative estimate of the thermal gradient across the device is then the measured temperature difference from the source to the sink, which will be much higher than that across the device for any non-permanent thermal interface materials. For a mechanically-stable device, high levels of compressive force may be applied to minimize the thermal contact resistances and improve the accuracy of the extracted temperature gradient.



**Figure 4-2.** Schematic of compressed steady-state reference bar apparatus for thermal measurement.

Yang *et al.* [66] characterized a microfabricated polysilicon in-plane thermoelectric generator using a multimeter for open-circuit voltage and an infrared thermometer for temperature differences from 0-15 K, though no further details were provided on the methodology of the temperature measurement. Kao *et al.* [67] developed a suspended-structure in-plane thermoelectric module, and characterized the thermal performance using an unspecified infrared temperature detector. The use of infrared temperature detection makes particular sense for planar structures since all relevant temperatures can be viewed simultaneously from one angle. Dávila *et al.* [7] also developed a planar microfabricated generator device, but characterized the thermal gradients using a thermorefectance technique to extract the surface temperatures based on a measured reflectivity correlated to temperature.

### 4.1.3 Special Considerations for Microscale Devices

The characterization of microscale devices presents special challenges. When utilizing a traditional steady-state heater/thermocouple system, thermal contact

## *PROTOTYPING AND CHARACTERIZATION OF MICROFABRICATED THERMOELECTRIC GENERATORS*

resistance may easily be on the order of the device resistance due to the small contact area. In the measurement of the thermal conductivity of bulk material and thin films, a sequence of varying compression can be applied to the sample to extrapolate to a zero boundary resistance condition. However, due to the inherent design of microscale thermoelectric generators which are often supported by narrow pillars of material, the application of significant compression is unwise. Contactless temperature measurement such as described using infrared detectors or thermoreflectance offer great promise assuming the geometry is amenable to signal capture. Infrared microscopy holds significant advantages by being contactless so as to avoid thermal capacitance issues of thermocouples, and also features diffraction-limited resolution (typically  $\sim 2\text{-}3\ \mu\text{m}$ ) for observation of microscale features. This work is the first to the author's knowledge to demonstrate cross-plane characterization of a microfabricated thermoelectric generator using infrared microscopy technology.

### **4.2 Device Design and Fabrication**

We use the optimization methodology described in Chapter 3 and Ref. [37] to design for maximum power output for a fixed source-sink  $\Delta T$  and finite external thermal resistances, representative of solid contact to a heat source and passive fin array convection to ambient temperature. The equivalent 1D thermal resistance network with Joule and Peltier effects is shown in Figure 3-2a. Under the fixed source-sink  $\Delta T$  assumption, the presence of finite external thermal resistances limits the temperature drop, and therefore voltage, across the thermoelectric elements. While the device can be designed such that temperature drop across the active region asymptotically approaches the maximum (source-sink)  $\Delta T$ , the geometric means of achieving this are lengthening the thermoelectric elements or narrowing their cross-section to add thermal resistance, which also add competing electrical resistance. For maximum power output under a fixed source-sink  $\Delta T$  condition, there exists an optimum ratio of temperature drop (i.e. thermal resistance) between the active and inactive regions of the system. In a perfect system neglecting losses due to thermal

shunting in the filler section between the thermoelements, Peltier heats, Joule heat, electrical losses in the interconnects, and other effects, this optimum ratio is 1:1, meaning that the device should be designed such that half of the source-sink  $\Delta T$  is dropped across the thermoelectric elements and half across all other thermal resistances in the heat path. This analog to maximum power at matched electrical resistance is a good conceptual argument, but when realistic system losses are considered this optimum ratio can be much different and must be given appropriate consideration. The devices in this set were designed to have variable thermal and electrical resistances, in order to cross-validate experimentally with trends demonstrated by the closed-form modeling approaches developed in Chapter 3. As such, there are three devices with the same nominal size thermoelements (legs), but different numbers in each. This changes the electrical and thermal resistance for each device. Additionally, we look at two devices that have been bonded under different conditions to observe device sensitivity to bond force.

Devices were fabricated by depositing p- and n-type material on separately-processed 4" wafers. The 4- $\mu\text{m}$ -thick gold pad was fabricated on the Si wafer with  $\text{SiO}_2$  (500nm) as an insulator by successive sputtering, patterning, electroplating, and seed layer removal. The thermoelectric layer was sequentially prepared using the physical vapor deposition (PVD) system by RF co-sputtering the  $\text{Bi}_2\text{Te}_3$  target and the Te target for n-type, and RF single sputtering the  $\text{Sb}_2\text{Te}_3$  target for p-type. A 1- $\mu\text{m}$ -thick Bi film was then RF-sputtered as an adhesion layer. For prototyping, the p- and n-type wafers were diced into individual devices and assembled using flip-chip thermocompressive die-bonding. The general process is illustrated in Figure 4-3.

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## 1. Gold contact patterning



## 2. Photoresist mask



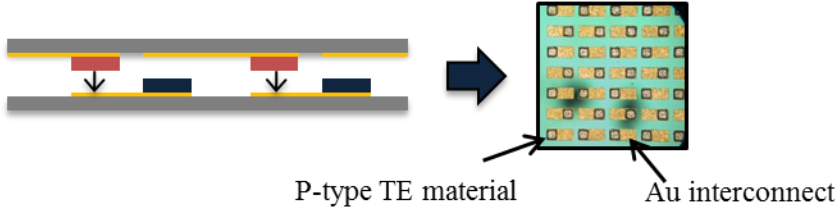
## 3. Sputtering of P- or N-type thermoelectric material + Bi bonding layer



## 4. Photoresist liftoff



## 5. Flip-chip bonding



**Figure 4-3.** Illustration of thin-film device fabrication process.

Four-point probe tests performed on test structures patterned onto each wafer measured electrical resistivities of  $1.56 \times 10^{-5} \Omega\text{-m}$  and  $0.90 \times 10^{-5} \Omega\text{-m}$  for the n- and p-type materials, respectively. A differential Seebeck measurement was performed which yielded n- and p-type Seebeck coefficients of  $-115 \mu\text{V K}^{-1}$  and  $+110 \mu\text{V K}^{-1}$ , respectively. Electrical resistivity of the gold interconnect depositions was measured to be  $2.57 \times 10^{-8} \Omega\text{-m}$ . Electrical and Seebeck material measurements were performed prior to the thermocompressive die-bonding process.

This study focuses on five fabricated devices, highlighting two parameters of interest. In one set, three devices are fabricated with the same thermoelement dimensions (nominally  $8.5 \mu\text{m}$  tall with  $30 \mu\text{m} \times 30 \mu\text{m}$  cross-section), but with



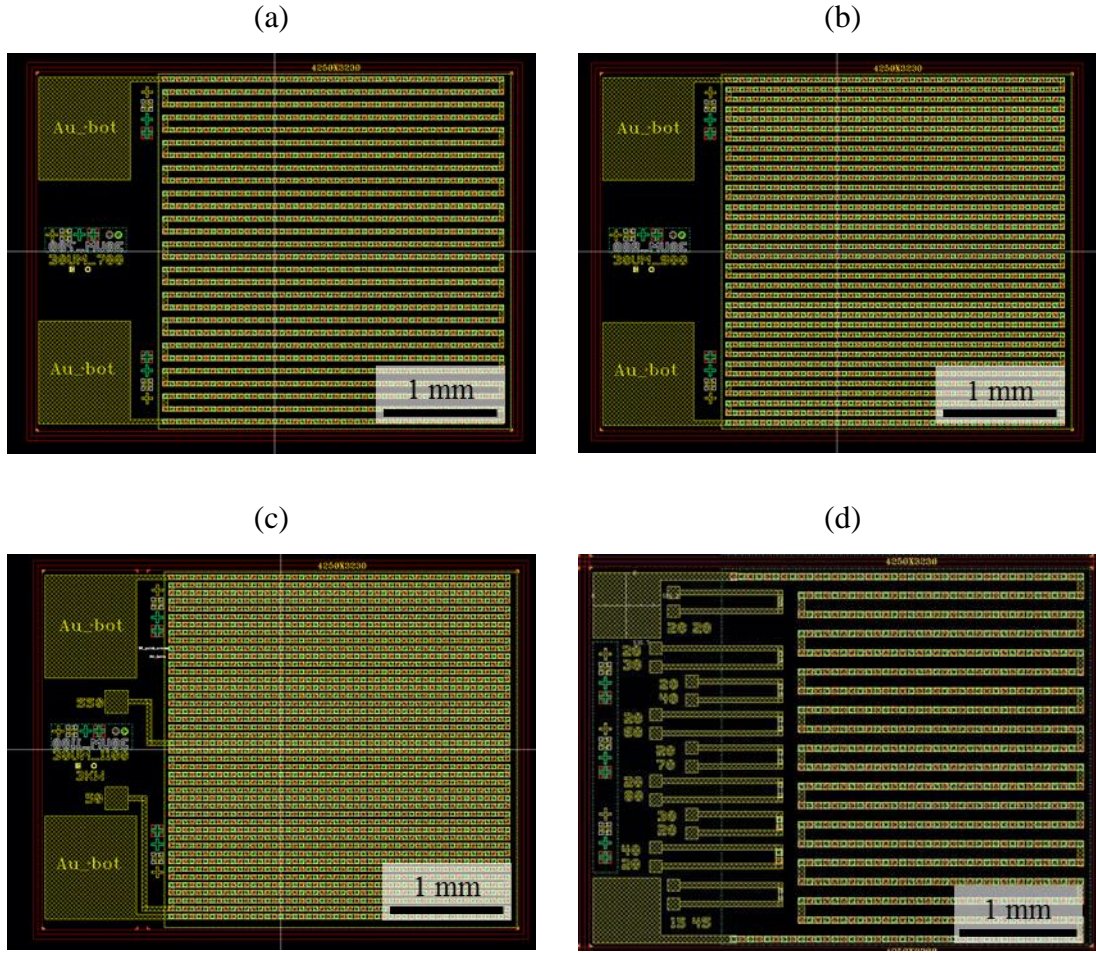
different numbers of thermocouples (700, 900, and 1100) in the same footprint, resulting in different fill fractions, and different thermal and electrical resistances. The bonding force was varied for the 700, 900, and 1100 thermocouple devices according to the fill fraction, in an attempt to apply consistent bonding pressure at the thermoelement/interconnect interfaces for the three prototypes. The second set includes two devices identical in design (348 thermocouples and  $40\text{ }\mu\text{m} \times 40\text{ }\mu\text{m}$  cross-section), but bonded with different forces to observe the sensitivity of device performance to compression during the bonding process. All devices were individually die-bonded at  $350\text{ }^{\circ}\text{C}$  for 2.5 minutes, followed by a 4 minute cool-down. A summary of the devices examined in this study is provided in Table 4-1.

**Table 4-1.** Summary of prototype devices characterized.

Device ID	$n_{\text{TC}}$	Nominal leg width [ $\mu\text{m}$ ]	Bonding Force [N]
1	700	30	55.2
2	900	30	70.9
3	1100	30	86.7
4	348	40	58.9
5	348	40	49.1

Patterning layouts for each of the 4 unique geometries listed in Table 4-1 are provided in Figure 4-4.

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**Figure 4-4.** Patterning layouts for (a) Device 1 (700 thermocouples, 30  $\mu\text{m}$  nominal leg width), (b) Device 2 (900 thermocouples, 30  $\mu\text{m}$  nominal leg width), (c) Device 3 (1100 thermocouples, 30  $\mu\text{m}$  nominal leg width), and (d) Devices 4-5 (348 thermocouples, 40  $\mu\text{m}$  nominal leg width). Devices 4 and 5 were designed with several single thermocouple test pads for diagnostic purposes.

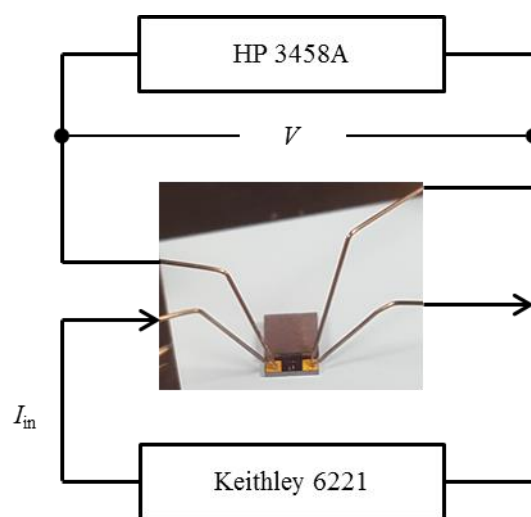
### 4.3 Measurements for Electrical Resistance

The Seebeck effect complicates the characterization of the electrical resistance of thermoelectric generators. In addition to the voltage rise from the resistance due to Ohm's law, the current flowing from the multimeter through the device induces Peltier

heating which establishes a temperature gradient resulting in an additional voltage contribution from the Seebeck effect. One way to circumvent this is to supply a pulsed direct current signal and make use of the difference in electrical and thermal time constants in the system.

### 4.3.1 Experimental Setup

The electrical resistance measurement is set up in a four-point probe configuration using four micromanipulators holding beryllium-copper probe tips. Two probes connect the device in series with a current source (Keithley 6221), while the remaining two probes connect the device in parallel with a high-impedance voltmeter (HP 3458A), as illustrated in Figure 4-5.

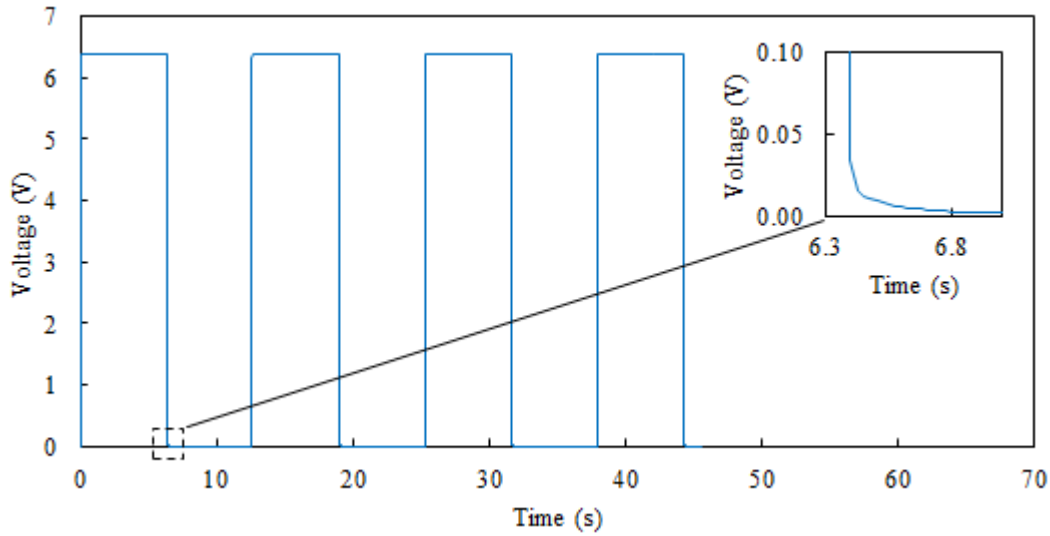


**Figure 4-5.** Schematic of experimental setup for electrical resistance with inset of device under test.

Devices were supplied with 25 mA of current for ~6 seconds, followed by zero current for an additional ~6 seconds. The current from the 6221 is controlled and raw voltage data from the 3458A recorded using a GPIB link to a Matlab script.

### 4.3.3 Results and Discussion

Voltage data recorded for Device 3 is shown for 4 pulsed current cycles in Figure 4-6. An inset plot zooms into the measured decay resulting from the Seebeck voltage due to Peltier heating.



**Figure 4-6.** Voltage vs. time for Device 3, showing 4 current pulse cycles and an inset of the decay due to Seebeck voltage.

Using Ohm's law, the resistance is calculated by dividing the ( $I \times R$ ) voltage contribution by the current input. This voltage is determined by subtracting the measured value immediately after the current is shut off from the last value measured with current flowing. A summary of the information extracted from the electrical measurements is provided in Table 4-2.

**Table 4-2.** Experimental results from electrical measurements of prototype devices.

Device ID	$n_{TC}$	Nominal leg width [ $\mu\text{m}$ ]	Measured Electrical Resistance [ $\Omega$ ]
1	700	30	166
2	900	30	211
3	1100	30	255
4	348	40	59
5	348	40	246

It is noted that the thermally-induced temperature decay shown in Figure 4-6 is the basis of the Harman technique described in Section 4.1.1. However, the small thermal capacitance and high electrical resistance of the microdevices did not prove amenable to extracting reasonable values of the figure of merit  $ZT$  by this method.

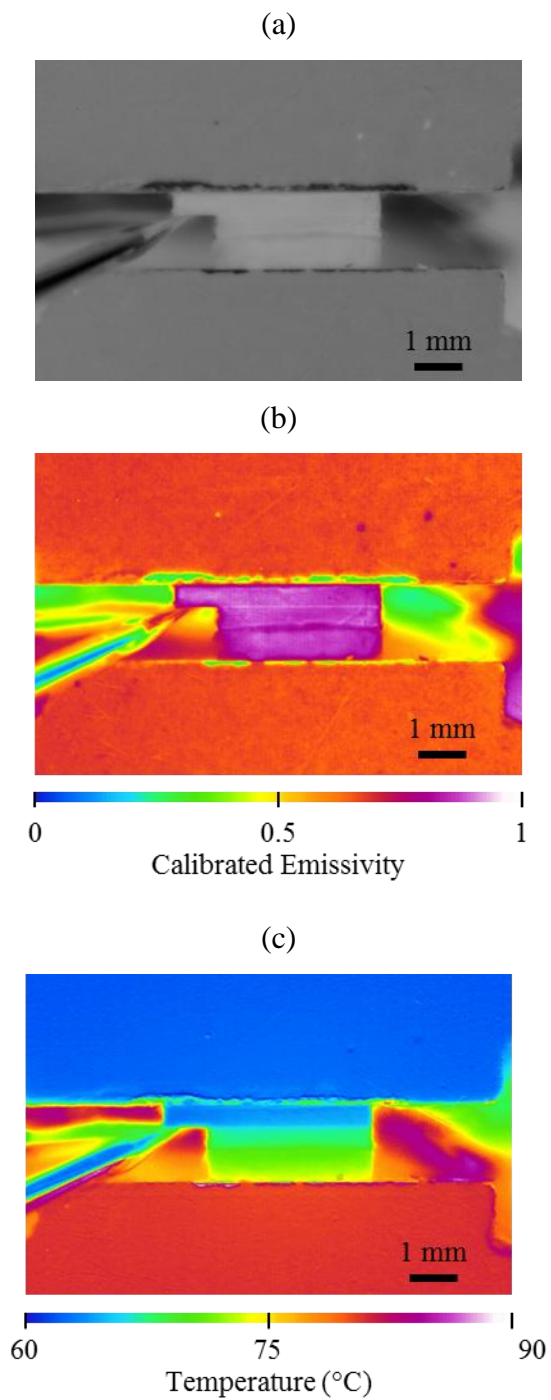
## 4.4 Performance Characterization by Infrared Microscopy

In order to circumvent the challenges with traditional steady-state thermoelectric generator measurements for microdevices described in Section 4.1.3, the technique of infrared microscopy was applied to measure the through-plane thermal gradient of the device.

### 4.4.1 Experimental Setup

For this study we use an infrared microscope (QFI InfraScope II) to directly measure the device temperature gradient with a spatial resolution of approximately 20 micron/pixel. The InfraScope software uses a pixel-by-pixel emissivity calibration feature to accurately convert the emission from gray bodies to temperature. Since the silicon substrates are not high emitters of infrared radiation, the surface emissivity was increased by applying a thin coating of black liquid electrical tape, manufactured by Gardner Bender. This particular coating was chosen over graphite lubricant spray [59] to avoid electrical shorting of the device, and over boron nitride spray [68] because of difficulty masking the narrow device edges and a concern for possible thermal shunting across the substrate gap. It also proved relatively easy to apply in a thin layer using a fine-tip brush when diluted with petroleum-based lighter fluid, and removed cleanly in a single film using tweezers when necessary. The calibrated emissivity of the coating was approximately 0.88-0.94 depending on variations in coating thickness and uniformity.

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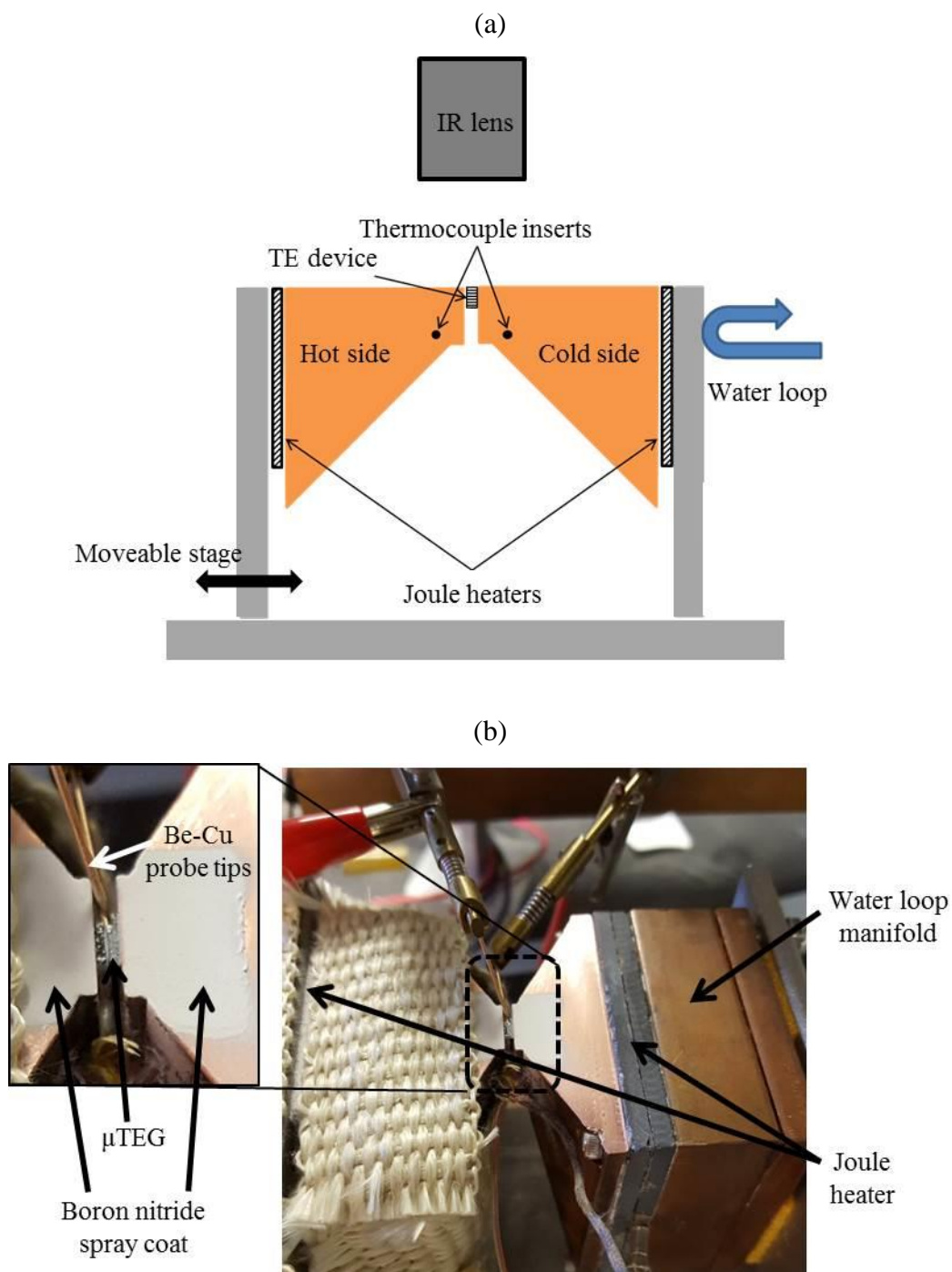
**Figure 4-7.** Image captures from infrared microscopy, showing (a) isothermal focus image for calibration, (b) resulting pixel-by-pixel emissivity map, and (c) 2D temperature field under thermal gradient.

Boron nitride spray was used to increase the emissivity of the copper block surface where a larger area required coating and thermal shunting was not a concern. A sequence of images showing (a) the IR focus image at isothermal conditions for calibration, (b) the calibrated 2D emissivity map, and (c) a temperature map showing thermal gradient is given in Figure 4-7. Artifacts are noticeable near certain interfaces, particularly on the copper blocks (see yellow/green at topmost interface in Figure 4-7c) where boron nitride coating has been scratched from sample loading/unloading. These artifacts can present themselves in the extracted temperature distributions as seemingly-nonphysical spikes or dips in the temperature profile.

A custom heating and linear compression apparatus is used to support the device under the infrared objective lens. Two copper blocks act as thermal reservoirs and sandwich the layers of interest. Joule heaters contact the outside of each block, while connections for a closed-loop water line are also affixed to one side. In these experiments, the water line is used to supply a constant supply of water at 62.5 C on one side, while the Joule heater is used to further heat the opposite side in order to establish various temperature gradients. Thermocouples (K-type) are embedded into the copper blocks to monitor the reservoir temperatures, and a miniature button load cell used to measure the compressive force. Electrical contact is made to gold pads on the device with micromanipulators holding beryllium-copper probe tips to minimize contact resistance. In tests, the presence of the probes was not found to influence the thermal profile of the device. A diagram and photograph of the setup is provided in Figure 4-8.



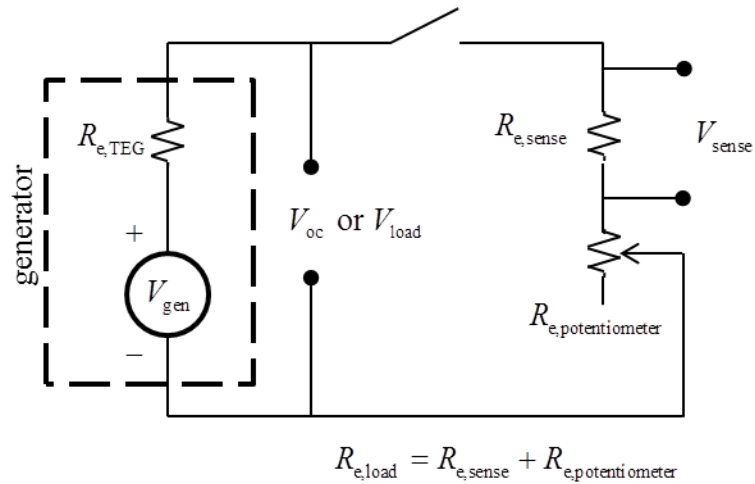
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**Figure 4-8.** (a) Illustration and (b) photo of setup used for thermoelectric device characterization with infrared microscopy. In (b), the micromanipulators carrying probe tips for access to device contact pads are visible. Care was taken to not short the probes with the copper blocks.



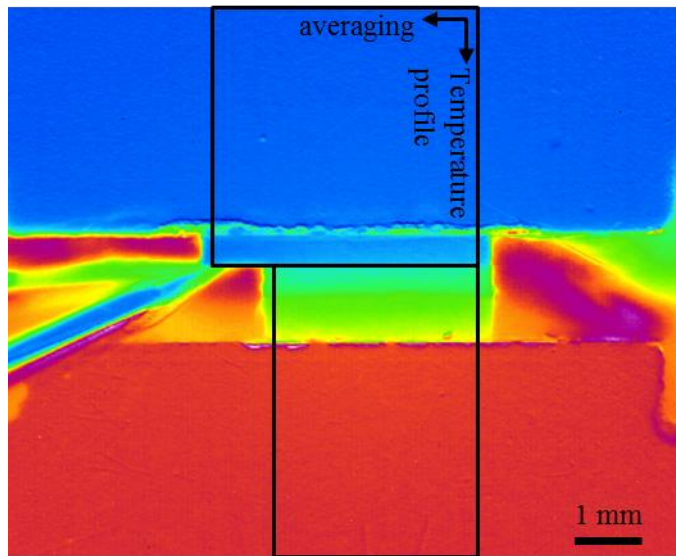
Throughout the majority of the experiment, open-circuit device voltage and copper block temperatures are recorded at a frequency of 4 Hz using a NI cDAQ-9174 chassis with modules for voltage (NI-9207) and thermocouples (NI-9213, with integrated cold-junction compensation). Data are visualized and recorded with a Labview VI. Infrared temperature and load power data are recorded for several steady-state temperature differences. The steady state criterion used is a total fluctuation of less than 0.2 °C in the thermocouple readings of each copper block and their difference over a 5 minute period. After reaching steady-state conditions, an infrared image is acquired with the InfraScope software, averaging over 20 frames to reduce noise. Then the device is connected to a circuit containing a 10-turn, 10 kΩ potentiometer to sweep a range of load resistances. Voltage is read across a fixed sense resistor (measured to be 4.76 Ω) to determine current and potentiometer value simultaneously, and the voltage across the sense resistor in series with the potentiometer is recorded as load voltage. The sense resistor value must be less than the electrical resistance of the device to present a peak in the load power vs. load resistance curve. The circuit is illustrated in Figure 4-9. For each load resistance, electrical data are averaged over 20 acquisitions.



**Figure 4-9.** Circuit diagram for electrical output measurements.

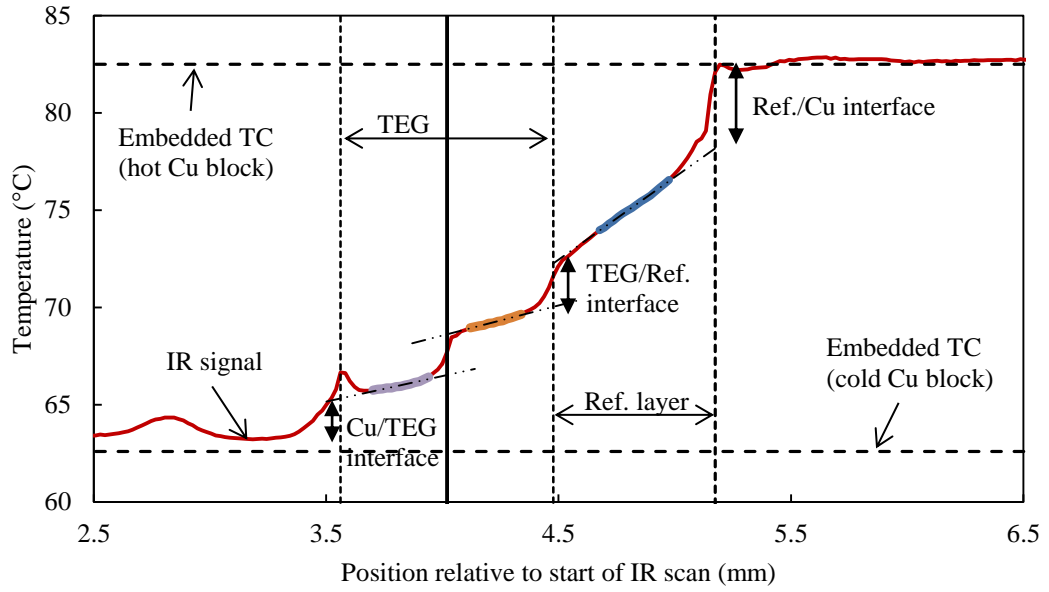
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For analysis, a rectangular region of interest spanning the device and several millimeters of each copper block is selected, and the temperature averaged in the direction perpendicular to heat flow to reduce noise. The substrate temperature profiles are identified, and linear fits used to extrapolate the temperatures at the outer surfaces of the device following Barako, *et al.* [59]. The infrared capture in Figure 4-10 shows the regions of the temperature map used to generate a temperature profile across the setup.



**Figure 4-10.** Regions selected for linear averaging of infrared capture. Temperature values are averaged in the horizontal direction to produce a temperature profile in the direction of heat flow, as shown in Figure 4-11.

A characteristic temperature profile is shown in Figure 4-11. We note the significant thermal boundary resistance between the device and adjacent media.



**Figure 4-11.** Characteristic temperature profile from IR scan. Data shown are for Device 2 with a copper block  $\Delta T \sim 20$  °C. At steady state, measured open-circuit voltage and maximum load power was 477 mV and 261  $\mu$ W, respectively.

#### 4.4.2 Power Output Characterization

When the switch in Figure 4-9 is closed and the electrical circuit with load resistance completed, the electric current through the load is calculated using the voltage across the sense resistor:

$$I_{\text{load}} = \frac{V_{\text{sense}}}{R_{\text{e,sense}}} \quad (4.1)$$

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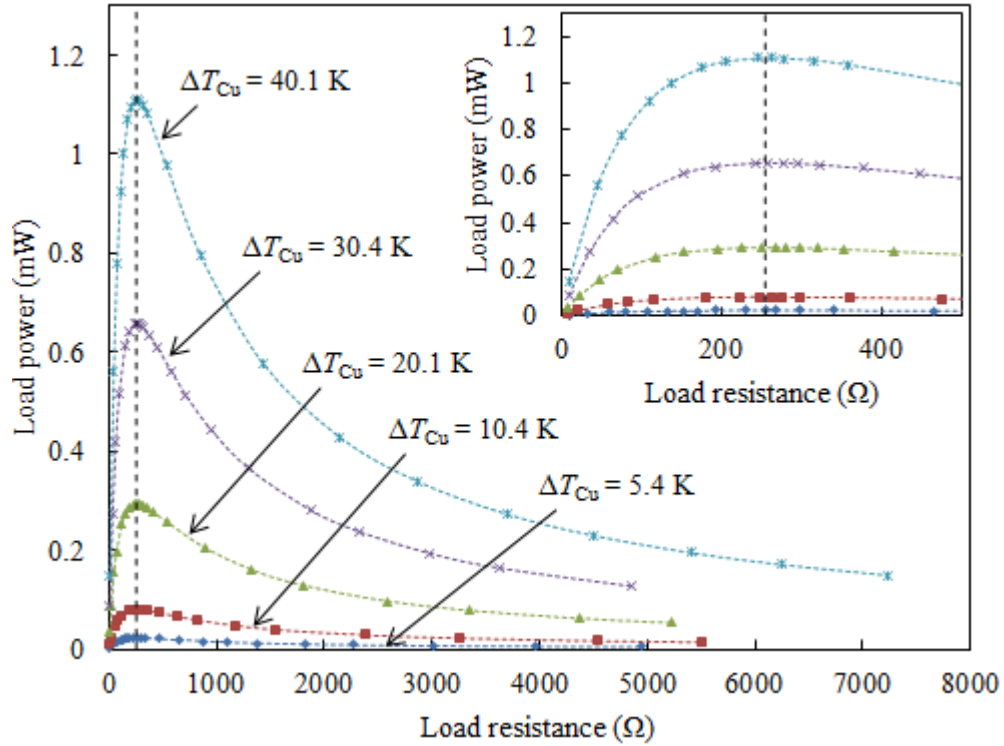
For load sweeps, the value of the potentiometer is calculated in real time using the current calculated in Equation 4.1 and the voltage across the potentiometer, measured by subtracting the measured sense voltage from the voltage across the series resistance (sense plus potentiometer resistors).

$$R_{\text{e,potentiometer}} = \frac{V_{\text{load}} - V_{\text{sense}}}{I_{\text{load}}} \quad (4.2)$$

The series combination of the sense resistor and potentiometer is considered to be the full load resistance, and the electric load power delivered is calculated using the series voltage and current.

$$P_{\text{load}} = V_{\text{load}} I_{\text{load}} \quad (4.3)$$

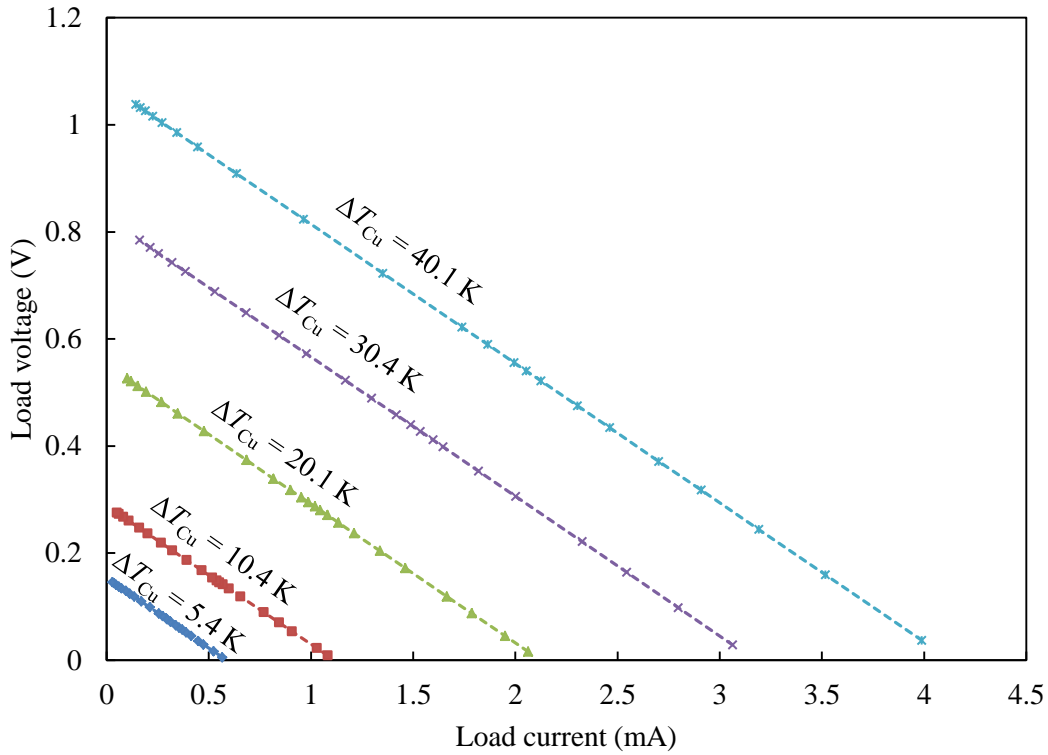
Load power vs. load resistance is plotted for 5 steady-state measurements of Device 3 in Figure 4-12. The temperature difference  $\Delta T_{\text{Cu}}$  of the copper blocks measured by the embedded thermocouples is indicated, as well as the resulting device temperature difference  $\Delta T_{\text{TEG}}$  extrapolated from the IR signal. We note that the device is thermally in series with the reference layer, so it sees a smaller fraction of  $\Delta T_{\text{Cu}}$  than if it were directly compressed between the blocks.



**Figure 4-12.** Measured load power vs. load resistance curves for Device 3 at 5 different steady-state temperature gradients. An inset plot shows the span of load resistances near the value of the generator resistance (black dashed line).

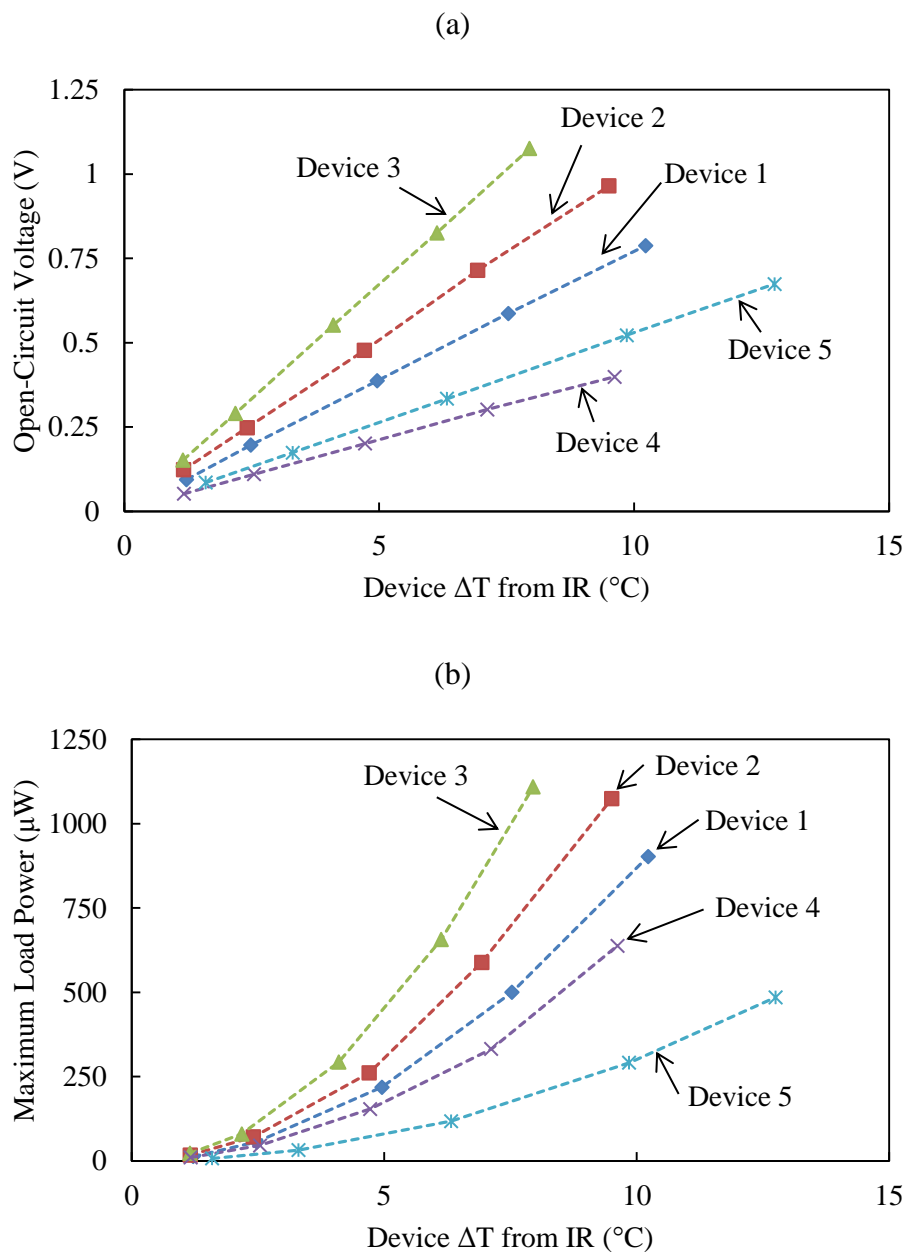
The power curves in Figure 4-12 are very promising. Even in 2008, Doms *et al.* [69] noted that operating power for existing wireless sensor node technology was on the order of 50-100  $\mu\text{W}$ . This prototype generator is proven to produce that amount of power from a very lossy thermal pathway (in series with a large reference layer thermal resistance and three compressed thermal grease interfaces) across only a 10.4 K reservoir temperature difference. Load voltage vs. current (I-V) lines are also plotted from the measured load data, and shown in Figure 4-13 for the same 5 steady-state conditions for Device 3. Power vs. load resistance and load voltage vs. current lines for all 5 prototype devices are included in Appendix A.

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**Figure 4-13.** Measured load voltage vs. current lines for Device 3 at 5 different steady-state temperature gradients.

While the block thermocouples provide an upper bound on the temperature gradient available to the device, the infrared microscope approach allows for much more precise determination of the temperature difference across only the device, removing the need for assumptions about the thermal resistances due to interfaces, etc. By generating temperature profiles like the one in Figure 4-11 (temperature traces for all devices are provided in Appendix B) the average temperature at the interfaces of the device can be calculated by extrapolating a linear fit through each of the substrate profiles to the device boundaries. Open-circuit voltages and maximum measured load power are plotted vs. the device temperature difference extracted from IR data in Figure 4-14.



**Figure 4-14.** Results for all 5 devices of (a) open-circuit voltage and (b) maximum load power as a function of the device  $\Delta T$  determined by infrared microscopy analysis. Devices 1-3 have the same nominal  $30\ \mu\text{m}$  leg width, but 700, 900, and 1100 thermocouples, respectively. Devices 4 and 5 each have 348 thermocouples with  $40\ \mu\text{m}$  nominal leg width, but assembled with 58.9 and 49.1 N bonding force, respectively.

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The open-circuit voltage produced per degree of temperature drop for each device is then:  $S_{\text{Device},1} = 77 \text{ mV K}^{-1}$ ,  $S_{\text{Device},2} = 101 \text{ mV K}^{-1}$ ,  $S_{\text{Device},3} = 136 \text{ mV K}^{-1}$ ,  $S_{\text{Device},4} = 41 \text{ mV K}^{-1}$ , and  $S_{\text{Device},5} = 53 \text{ mV K}^{-1}$ . As Figure 4-14b shows, all 5 devices are capable of producing well over the 50-100  $\mu\text{W}$  of power characteristic of wireless sensor nodes. However, a complete study requires an analysis of the device thermal resistance so that its performance can be predicted when coupled with necessary external resistances like thermal packaging and heat sinks.

### **4.4.3 Thermal Resistance Characterization**

The reference layer, a high-density, high-alumina ceramic, was cut to 3.3 mm x 3.2 mm to match the area of the smaller device substrate and placed in series with each generator during the infrared measurements. The thermal conductivity of the material was measured using a steady-state reference bar method under high compression to be  $27 \text{ W m}^{-1} \text{ K}^{-1}$ , and provided a layer thermal resistance ( $2.44 \text{ K W}^{-1}$ ) on the same order of magnitude expected for the generator devices. With known cross-section and thermal conductivity, the slope in the IR temperature signal through the reference layer allows for calculation of the heat flow through the reference layer/generator assembly via Fourier's law:

$$\dot{Q} = -kA \frac{dT}{dx} \quad (4.4)$$

We then define the generator thermal resistance as the extrapolated device temperature drop, determined using the methodology described in Section 4.3.3, divided by the heat flow determined using the reference layer and Equation 4.4:

$$R_{t,\text{TEG}} = \frac{T_{h,\text{TEG}} - T_{c,\text{TEG}}}{\dot{Q}} \quad (4.5)$$



For each device, the thermal resistance is reported in Table 4-3 by averaging the values calculated from each of the 5 steady state measurements. Second-order polynomial fits of measured load power vs. IR temperature gradient were used to calculate the maximum load power for all devices under two assumptions: (1) 5 K across the device directly, and (2) 5 K across the device and the alumina reference layer. These calculations are provided for each device in Table 4-3, and demonstrate significant drops in load power, which are more significant as the thermal resistance of the device decreases. This is because the lower resistance device is able to draw less of the available 5 K when in series with a parasitic external thermal resistance, which could be representative of packaging material or fin array. This can motivate the design of devices to feature fewer thermocouples giving higher thermal resistance if a large external thermal resistance is anticipated.

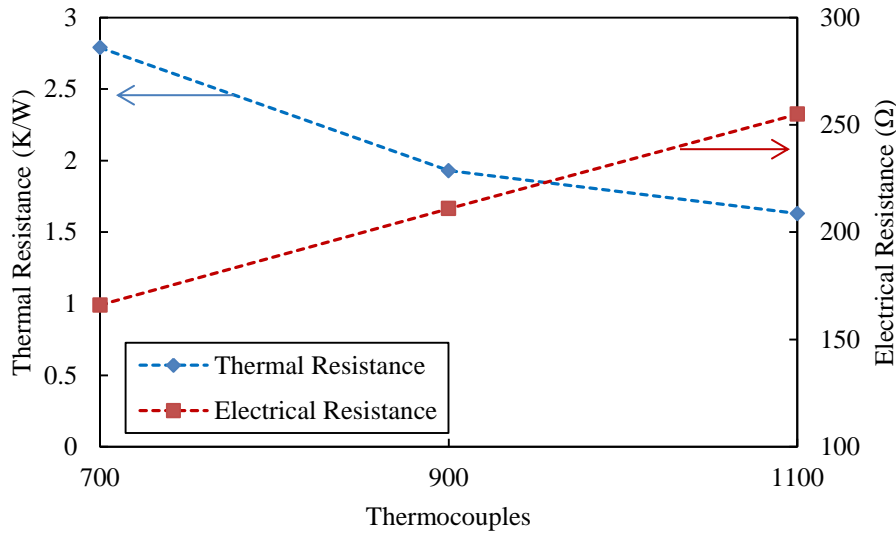
**Table 4-3.** Measured thermal resistance and maximum power outputs for Devices 1-5.

Device ID	$n_{TC}$	Nominal leg width [ $\mu\text{m}$ ]	Thermal Resistance [ $\text{K W}^{-1}$ ]	Max power for 5 K device $\Delta T$ [ $\mu\text{W}$ ]	Max power for 5 K device+reference layer $\Delta T$ [ $\mu\text{W}$ ]
1	700	30	2.79	223	70
2	900	30	1.93	302	66
3	1100	30	1.63	436	74
4	348	40	2.44	167	41
5	348	40	3.34	74	26

#### 4.4.4 Functional Dependence on Number of Thermocouples

We now focus on the set of Devices 1-3 to analyze and discuss the functional dependence of thermal resistance and power output on a changing number of thermocouples having the same nominal dimensions. Figure 4-15 provides a plot of the measured thermal and electrical resistances of Devices 1-3 as a function of the number of thermocouples.

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**Figure 4-15.** Measured variation in electrical and thermal resistances for Devices 1-3.

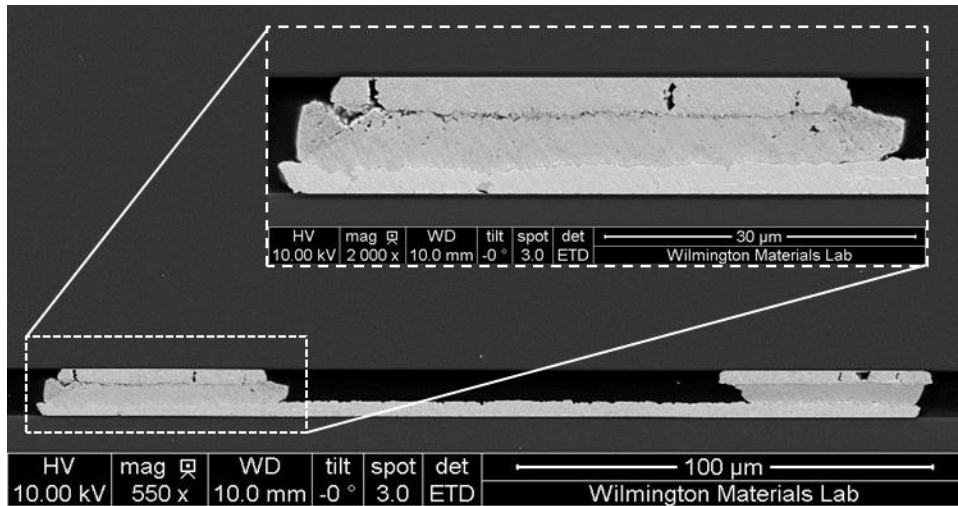
Measured electrical and thermal resistance each follow expected trends, as electrical resistance should vary linearly with number of thermocouples and thermal resistance should vary inversely with  $n_{TC}$  as the fill fraction changes with the number of identical thermoelements. In the limit of 100% fill fraction, the thermal resistance should approach the 1D resistance through both substrates and a fully-densified film of thermoelectric material.

However, measured thermal resistances for the devices were generally lower than expected from typical material assumptions and the nominal leg dimensions inside the device. Cross-sectional SEM images (see Figure 4-16) of devices produced and bonded from the same wafers as those in this study were prepared by filling the device with an epoxy resin for mechanical stability, then mechanically polishing to expose the internal structure for microscopy. The visible structural defects are believed to be from the bonding process. The SEM images showed that the active thermoelectric material was notably shorter ( $\leq 5.5 \mu\text{m}$ ) than nominal design parameter of  $8.5 \mu\text{m}$ . The numerical models for devices designed with  $8.5 \mu\text{m} \times 30 \mu\text{m} \times 30 \mu\text{m}$  nominal dimensions were therefore adjusted to assume thermoelement dimensions of  $5.5 \mu\text{m} \times 37.3 \mu\text{m} \times 37.3 \mu\text{m}$ , assuming leg volume remains constant.

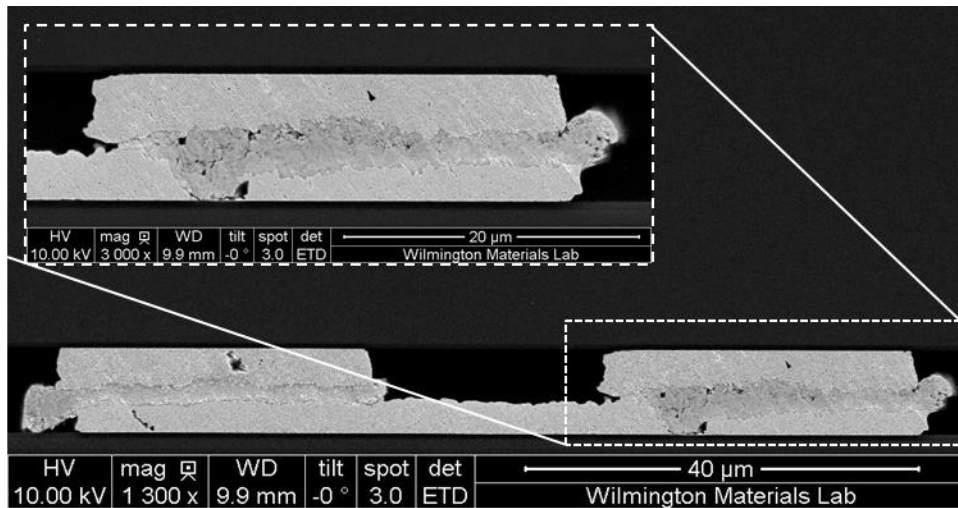
It was also observed during the analysis that the thermal conductivity of the substrate layers appears to increase monotonically with the number of thermocouples (or fill fraction), from  $\sim 47 \text{ W m}^{-1} \text{ K}^{-1}$  for Device 1 (700 thermocouples) to  $\sim 86 \text{ W m}^{-1} \text{ K}^{-1}$  for Device 3 (1100 thermocouples), determined by comparing linear fits through the reference layer and substrate layer. One hypothesis is that the fits provide an effective thermal conductivity which includes resistances due to spreading effects from the relatively low fill fractions, or non-negligible thermal boundary resistances at the bond surfaces resulting from non-optimized bonding processes, or a combination. In the 3.3 mm x 3.2 mm top substrate, the thermal resistance through 450  $\mu\text{m}$  of monocrystalline silicon assuming  $125 \text{ W m}^{-1} \text{ K}^{-1}$  at  $\sim 70^\circ \text{C}$  is  $0.34 \text{ K W}^{-1}$ . The resistance through the 500 nm  $\text{SiO}_2$  passivation layer likewise is  $0.034 \text{ K W}^{-1}$  assuming  $1.38 \text{ W m}^{-1} \text{ K}^{-1}$ . Subtracting these contributions from the effective substrate resistances calculated from the IR slopes and multiplying by the nominal leg area (with assumed leg shortening) bonded to one substrate (one leg per thermocouple), gives area-specific boundary resistances of  $5.18 \times 10^{-7} \text{ m}^2 \text{ K W}^{-1}$ ,  $2.23 \times 10^{-7} \text{ m}^2 \text{ K W}^{-1}$ , and  $1.84 \times 10^{-7} \text{ m}^2 \text{ K W}^{-1}$  for the 700, 900, and 1100 thermocouple devices, respectively. These values are within an order of magnitude of the values predicted using the diffuse mismatch model theory for thin film  $\text{Bi}_2\text{Te}_3/\text{Cu}$  and  $\text{Sb}_2\text{Te}_3/\text{Cu}$  interfaces by da Silva and Kaviani [57]. These resistances enter into the closed-form model from Chapter 3 via the external resistance terms  $R_{t,h}$  and  $R_{t,c}$  in Equation 3.11. Average thermoelectric properties are assumed for the n- and p-type materials:  $S_{\text{net}} = 225 \mu\text{V K}^{-1}$ ,  $\rho = 1.23 \times 10^{-5} \Omega\text{-m}$ , and  $k = 2.0 \text{ W m}^{-1} \text{ K}^{-1}$ . A leg/interconnect electrical contact resistance of  $3.2 \times 10^{-11} \Omega \text{ m}^2$  fits to the measured generator resistance values for all three devices. The total device thermal resistance is given in Figure 4-17a for numerical and experimental calculations. Calculated experimental and numerical maximum load power for 5 K directly across Devices 1-3, and for 5 K across Devices 1-3 in series with the reference layer is given in Figure 4-17b as a function of thermocouples with the respective TBR values discussed previously.

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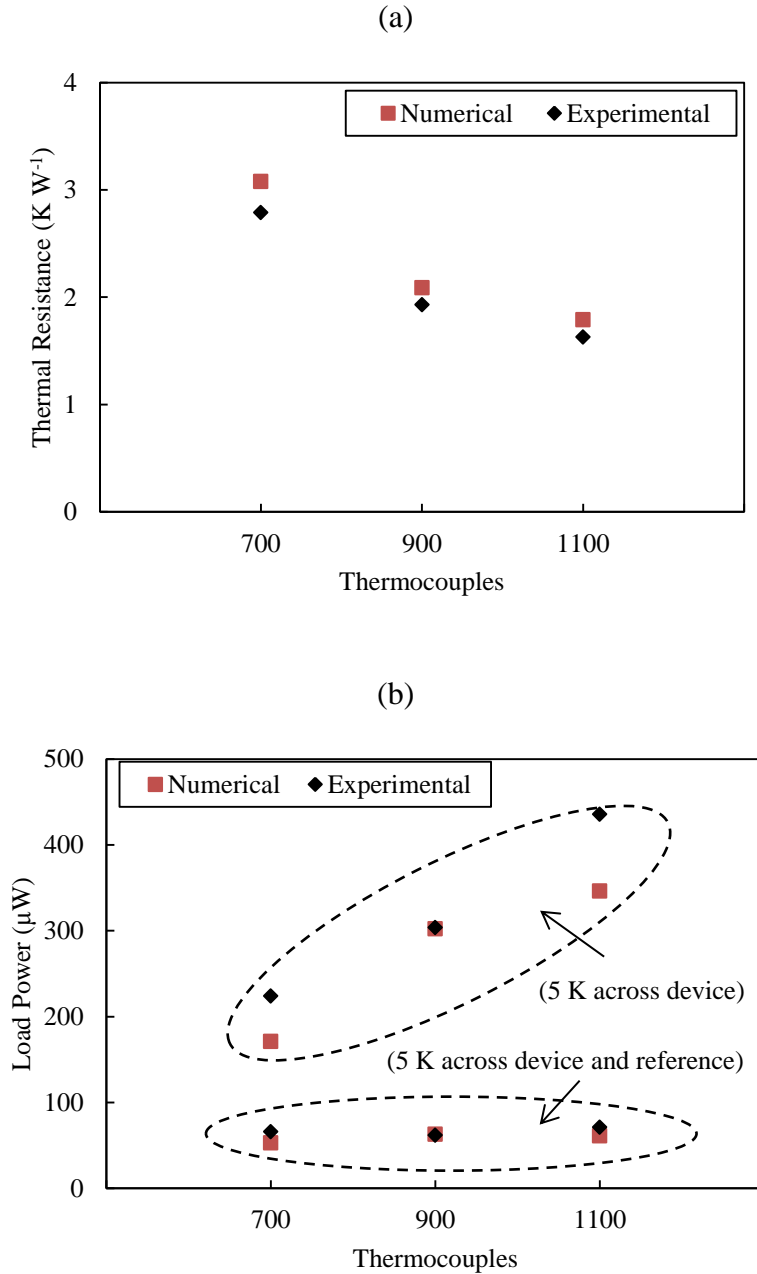
(a)



(b)



**Figure 4-16.** Cross-sectional SEM of devices bonded from the same wafer as the devices in this set. The image in (a) shows a single thermocouple with inset of an individual leg for a device with 378 thermocouples, nominal leg height and width of 8.5  $\mu\text{m}$  and 40  $\mu\text{m}$ , respectively, and bond force of 53.0 N. The image in (b) provides the same views of a device with 1620 thermocouples, nominal leg height and width of 8.5  $\mu\text{m}$  and 20  $\mu\text{m}$ , respectively, and bond force of 56.8 N.



**Figure 4-17.** (a) Interpolated maximum load power for 5 K temperature difference across Devices 1-3 and for 5 K temperature difference across Devices 1-3 in series with alumina reference layer, comparing experimental results with numerical modeling outputs. (b) Comparison of numerical and experimental calculations of thermal resistance for Devices 1-3 as a function of the number of thermocouples.

#### **4.4.5 Impact of Bonding Force**

Devices 4 and 5, with identical geometries, reveal important information about the impact of bonding force in the assembly process. Assuming that their leg lengths have also been reduced to 5.5  $\mu\text{m}$  through the bonding process, leg width dimensions increase to 49.7  $\mu\text{m}$  on a side. However, the force of bonding used to assemble Devices 1-3 was normalized by the total leg contact area (nominal leg cross-section times two legs per thermocouple) in an attempt to keep the pressure on the contact points even between devices. This was not true for Devices 4 and 5, and based on the SEM results presented in Figure 4-16, it is likely that the legs in Device 5 are closer to their original dimensions than those in Device 4. From effective substrate conductivities of 67 and 61  $\text{W m}^{-1} \text{K}^{-1}$  for Device 4 and 5, respectively, we can fit to the measured device thermal resistances of 2.44 and 3.34  $\text{K W}^{-1}$  by varying the leg thickness. The final leg volume is assumed to be equal to the nominal leg volume (8.5  $\mu\text{m} \times 40 \mu\text{m} \times 40 \mu\text{m}$ ). This process gives final leg dimensions for Devices 4 and 5 of 5.0  $\mu\text{m} \times 52.1 \mu\text{m} \times 52.1 \mu\text{m}$  and 6.4  $\mu\text{m} \times 46.1 \mu\text{m} \times 46.1 \mu\text{m}$ , respectively. With these dimensions the corresponding leg/interconnect TBR values are  $2.47 \times 10^{-7}$  and  $2.39 \times 10^{-7} \text{ m}^2 \text{K W}^{-1}$  for Device 4 and 5, respectively. Using electrical contact resistance as a fitting parameter to measured device resistance gives values of  $5.3 \times 10^{-11} \Omega \text{ m}^2$  and  $3.1 \times 10^{-10} \Omega \text{ m}^2$  for Devices 4 and 5, respectively. Parameters used to fit to thermal and electrical resistance and the corresponding power outputs for 5 K temperature difference are given in Table 4-4.

**Table 4-4.** Fitting parameters and power output calculations for Devices 4 and 5.

Device ID	Bond force [N]	Fitted leg dimensions [μm]	Fitted leg/IC TBR [m <sup>2</sup> K W <sup>-1</sup> ]	Fitted leg/IC contact resistance [Ω m <sup>2</sup> ]	Max power for 5 K device ΔT – Sim./Exp. [μW]	Max power for 5 K device+reference layer ΔT – Sim./Exp. [μW]
4	58.9	5.0 x 52.1 x 52.1	$2.47 \times 10^{-7}$	$5.3 \times 10^{-11}$	166 / 165	41 / 43
5	49.1	6.4 x 46.1 x 46.1	$2.39 \times 10^{-7}$	$3.10 \times 10^{-11}$	56 / 74	19 / 26

The results discussed in this chapter present the first known efforts to characterize cross-plane microscale thermoelectric generators using infrared microscopy. Functional dependence of thermal and electrical resistance and power output on the number of thermocouples and the device assembly bonding force were observed and discussed. Finally, experimental results were cross-validated with the reduced-order modeling methodology presented in Chapter 3.

## **Chapter 5**

# **Packaging and Application Considerations for Microfabricated Thermoelectric Generators**

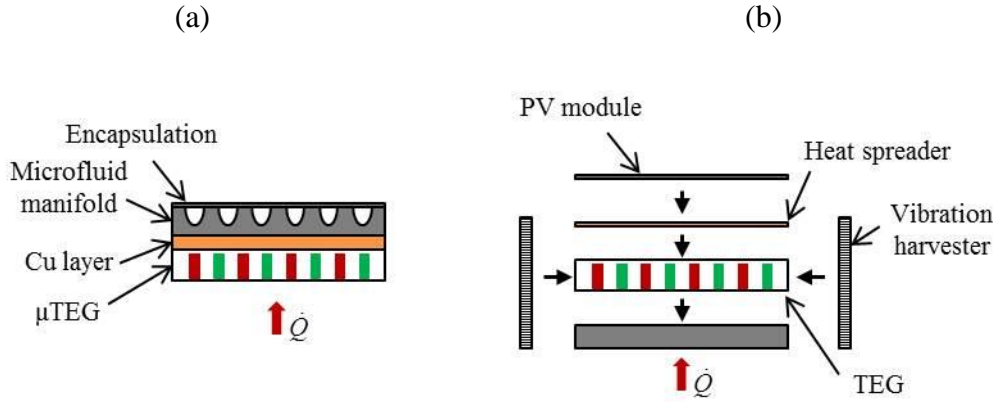
This chapter introduces the broader topic of packaging of microfabricated thermoelectric generators, as well as efforts in the literature for integration low-output thermoelectric generators with power electronics. The chapter, and this dissertation, concludes with the author's perspectives on the outlook for thermoelectric microgenerators and recommendations for future work.

### **5.1 Thermomechanical Packaging**

Once its constituent parts (thermoelements, interconnects, etc.) are assembled, a thermoelectric generator must be packaged for use in a way that both ensures mechanical robustness and minimal thermal losses into and out of the generator unit. A search of the literature does not at this time reveal a wealth of efforts in the design of efficient packaging for thermoelectric microgenerators, as most work is still being performed in tuning materials and device assembly processes. Among the available studies focused on packaging of microscale generators, Wojtas *et al.* [70] fabricated and measured an encapsulated microfluidic channel bonded to a device (see Figure 5-1a), referred to collectively as a micro thermoelectric generator/microfluidic heat transfer system ( $\mu$ TEG/ $\mu$ HTS). The study reported an enhanced thermal conductance from the generator due to the liquid cooling, but a minimum  $\Delta T$  of  $\sim 12$  K was required to produce a positive net power output due to the pumping requirements of the  $\mu$ HTS. However, the authors' simulations indicated an increase in material  $ZT$  to



0.5 would reduce the positive net power output threshold to  $\sim 2.5$  K. Francioso *et al.* [71] proposed a patterned conformal coating of thermoelectric material on a “wave-shaped” PDMS/Kapton assembly for flexible energy harvesting of body heat from the skin, although a full encapsulation was not implemented and the thermoelectric material was left exposed on the non-skin side. Liu *et al.* [72] discussed the integration of a MEMS-fabricated thermoelectric device into the packaging of a high power LED for cooling. The authors noted that for on-chip application (which is frequently proposed for both microfabricated cooler and generator thermoelectric devices), the use of silicon substrates should reduce the impact of mechanical stress from the coefficient of thermal expansion (CTE) mismatch between traditional ceramic substrates and silicon host chips. Wang *et al.* [73] reported a fully-packaged microfabricated SiGe thermopile used to harvest body heat in a wristwatch-style form factor. In their design, the bottom-up-assembled thermopile was capped with a silicon wafer prior to assembly in the wristwatch package. They compared the performance of bare contact with the thermopile structure to flip-chip bonding of a silicon chip with a thin coat of BCB resin and found a factor of 2.5 improvement in the voltage output vs. temperature gradient. However, the authors acknowledged that the low-conductivity ( $\sim 0.29 \text{ W m}^{-1} \text{ K}^{-1}$ ) polymer bonding layer is limiting and suggested future exploration of metal-metal bonding to reduce thermal losses. In a more conceptual note, Venkatasubramanian *et al.* [74] proposed a packaging configuration comprising other energy harvesting devices (photovoltaic and mechanical vibration) with a nanostructured superlattice material thermoelectric generator (see Figure 5-1b), but did not describe specific materials or modes of heat rejection from the theoretical assembly.



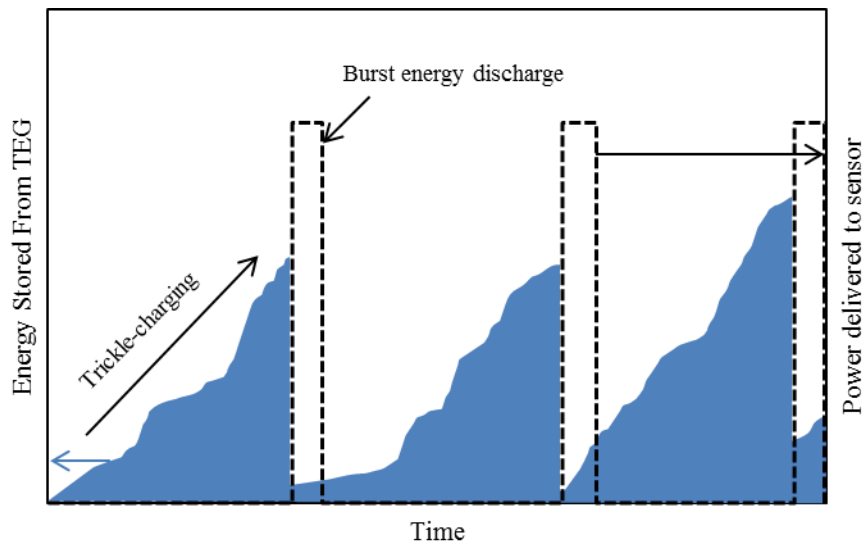
**Figure 5-1.** Illustrations of (a) prototype  $\mu$ TEG/ $\mu$ HTS packaging, adapted from Wojtas, *et al.* [70] and (b) concept multi-mode energy harvester assembly, adapted from Venkatasubramanian, *et al.* [74].

As the design and fabrication of optimized thermoelectric microgenerators becomes better-understood, the effectiveness of thermal packaging implementation is likely to become a bottleneck. Adding to the complexity of the microgenerator fabrication process, thermomechanical packaging efforts must be carried out on two regimes: at the macro scale with efficient heat rejection to ambient air or other heat sink, and at the MEMS scale for which best-practices and industry standards in packaging are still far from mature. The author considers this to be a very high-impact area of research for the advancement of microfabricated thermoelectric energy harvesters in terms of technology readiness level.

## 5.2 Integration with Power Electronics

A critical consideration in the application of thermoelectric microgenerators is how the power supply will be integrated with the power consuming device. In thermal energy harvesting applications it is likely that the temperature gradient used by the

harvester to generate power will be highly transient, leading to unsteady power delivery that could damage the electronic components receiving the converted energy. Further, when temperature gradients are small the voltage output from the device may not be sufficient to power electronic devices directly. For example, the typical forward voltage of 1.8-3.3 V for an LED, a generator drawing 1 K of temperature gradient across the thermoelements would need 4500-8250 parallel thermocouples of highly-optimized bismuth telluride-based materials ( $S_{\text{net}} \sim 400 \mu\text{V K}^{-1}$ ) to simply match the forward voltage of a single diode, estimated by  $V_{\text{load}} / (S_{\text{net}} \times 1 \text{ K})$ . As such, efforts have been made in the literature to integrate microgenerators with power management circuitry that can both buffer transients and provide discharge from storage devices at increased voltage and/or current, which would often be practical to run in a duty cycle as illustrated in Figure 5-2.



**Figure 5-2.** Illustration of power energy storage/discharge concept for thermoelectric harvesters.

The following provides an abbreviated review of literature treating the concept of power management circuitry for the integration of small, low-power thermoelectric generators with power consuming devices.

In 1997, Stordeur and Stark [44] published the results of a prototype device capable of producing tens of  $\mu\text{W}$  with relatively low  $\Delta T$  ( $\sim 10+ \text{ K}$ ), while previous thin film prototypes had able to output power only in the nW range. They proposed that, as low power electronics had progressed toward the range of  $\mu\text{W}$  consumption, thin film generators showed promise as a self-sufficient power supply for micro sensor systems but that a “smart low power management” circuit would be required. Two years later, Fleuriel *et al.* [45,46] described in their published results of electrochemically-deposited “thick” film harvesters an “energy harvesting” scheme based on the trickle-charging of a set of rechargeable batteries or capacitors. In this way, the authors estimated the technology’s ability to deliver 100 mW in a 10% duty cycle using thermal gradients between soil and air, but a power management circuit was not described or prototyped. In the same year, Kishi *et al.* [75] published the results of the development of a wristwatch powered by body heat using a small thermoelectric module. While not a true “thin film” generator, having 104 thermoelements  $80 \times 80 \times 600 \mu\text{m}$  in dimension, the system was one of the first examples of a functionally-integrated microscale thermoelectric generator with power management circuitry. In comparison, true thin film technology offers an advantage in greatly increased thermocouple density, which increases the voltage available to the boost circuit. The wristwatch circuit was demonstrated to boost the output voltage from a series of generators from a few hundreds of mV to 1.5 V with battery storage allowing the watch to operate for days after being removed from the wrist.

In 2007, Doms *et al.* [76] reported a comparative study of DC-DC converter architectures for integration with micro-machined thermoelectric generators producing power in the range of a few  $\mu\text{W}$ . The authors noted that, at the time, DC-DC converters utilizing Maximum Power Point Tracking (MPPT) algorithms had been successfully tested for thermoelectrics delivering power higher than 1 W, but that in the output range of microgenerators power management circuits were “practically non-existing.” The study concluded that the specific application will dictate the

optimal converter architecture, but that their calculations showed higher efficiency using larger, external inductors (100  $\mu\text{H}$ ) vs. small, on-chip inductors (215 nH). In a following study, Doms *et al.* [69] developed a power management circuit specifically for microscale thermoelectric power supplies. Noting that the control circuit's power consumption should be a small fraction of the already-low operating power of wireless sensor nodes ( $\sim 50\text{--}100\ \mu\text{W}$ ), their circuit contained a Dickson charge pump with variable number of stages as a DC-DC converter and a controller to optimize the number of stages of the charge pump, reporting an overall power management circuit efficiency up to 58%. In 2009, Becker *et al.* [77] published a study of autonomous sensor nodes utilizing power from thermoelectric generators to monitor aircraft structural health. While the study focused on commercial, bulk thermoelectric modules as power supply, the authors focused on low power DC-DC converters which can operate below 100 mV in open-circuit mode and configured for startup voltages around 250 mV, which is well within the capacity of microscale generators. The authors noted an issue with long startup times when using supercapacitors for the energy storage solution, and were able to circumvent it by introducing a system of coupled capacitors using first a small capacitor to charge to the circuit startup voltage level. They reported an overall power management circuit efficiency up to 65%.

The pace of published work proposing low power thermoelectric generators integrated with functional power management circuitry has accelerated since 2010. That year, Carmo [49] described integration of a thermoelectric microdevice with a simple DC-DC step-up converter that could deliver 3 volts when triggered with 300 mV output from a generator. Lu *et al.* [78] considered a commercial microfabricated TEG as a potential power source in a systems-level discussion of micro-scale energy harvesting with power management and energy buffering. They noted the growing popularity of adaptive power management for embedded energy harvesting systems as an area of research. Tan and Panda [79] proposed and demonstrated a hybrid solar photovoltaic + microfabricated TEG for energy harvesting from indoor ambient light and thermal energy sources. The outputs from each harvester were fed into a single

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power management circuit to power a TI CC2500 wireless sensor node. The circuit consisted of a boost converter with maximum power point tracker and pulse width modulation generation circuit, energy storage, and a regulating buck converter, consuming approximately 135  $\mu\text{W}$ . In 2012, Zhang *et al.* [80] demonstrated an ECG experiment on a human subject using a wireless body area sensor node powered by a small TEG. The system was designed to operate at different levels of power consumption, with demonstrated consumption from 397  $\mu\text{W}$  in raw data transmit mode to 19  $\mu\text{W}$  in an AFib detection mode transmitting the last 8 beats of raw ECG after detection of a rare AFib event. Im *et al.* [81] designed and demonstrated a transformer-based self-starting boost converter architecture optimized for low-voltage TEG applications. The circuit included an improved maximum power point tracking control system and was designed to operate with an input voltage range from 40-300 mV, and provided a maximum output power of 2.7 mW at an output voltage of 2 V and peak end-to-end efficiency of 61%. Desai *et al.* [82] proposed and simulated a circuit for low-output thermoelectric power management using a single transformer for startup and steady state operation, and supporting a dual-polarity input source. The ability for bipolar input support could be important in environmental harvesting applications where the direction of temperature gradient (and therefore polarity of the harvester output) may reverse periodically. Simulations of the circuit demonstrated a peak 68% steady-state conversion efficiency at a 5.5 V output with 30-500 mV magnitude input voltage.

Research in the area of power management circuitry for low-output thermoelectric power supplies is an important one that has clearly been gaining in popularity and necessity as power consumers become more efficient and the benefits of technologies like distributed wireless sensor networks become realized. While the issues surrounding the design of microfabricated thermoelectric devices themselves are already quite challenging, the inherent need for power conditioning adds further layers of complexity. Keeping in mind that a ~60% end-to-end peak efficiency is characteristic of a noteworthy power management and storage circuit in the literature,

a comprehensive system design will require careful attention to the expected environmental conditions and output of the generator to ensure that the system will operate as efficiently as possible.

## 5.4 Final Thoughts

The aim of this dissertation is to connect the concepts of thermoelectric material and device design from the nanoscale to the macro scale and present strategies for an integrated system optimization methodology. More specifically this work has been performed with the intention of contributing to the growing area of microfabricated thermoelectric generators, which show great promise for integration with low-power electronics including wireless sensor nodes and wearables for autonomous power delivery from near-ambient sources of waste heat. While only a small set of technologies were discussed here for the fabrication of nano/microscale materials and devices, the findings offer robust guidelines which may be applied to a broader range of assemblies in a rapidly-accelerating area of research.

First, we evaluated experimentally the cross-plane thermal transport in a new class of nanostructured polysilicon thermoelectric materials that exhibit enhanced thermoelectric power factor. A unique feature about these films was the engineered presence of nanoscale voids, which were previously hypothesized to have contributed to exceedingly-high room temperature thermoelectric power factors. Using a combination of measurement techniques, we demonstrated a positive correlation between the cross-plane material thermal conductivity and the mean diameter of nanoscale voids present inside the films, varying from  $\sim 14 \text{ W m}^{-1} \text{ K}^{-1}$  to  $\sim 21 \text{ W m}^{-1} \text{ K}^{-1}$  for mean void diameters of  $\sim 4 \text{ nm}$  to  $\sim 30 \text{ nm}$ , respectively. We then validated these trends with Matthiessen's rule scaling arguments, and numerically using Monte Carlo ray tracing to quantify the effects of geometric scattering on cross-plane thermal transport due to void and grain boundary contributions. Charting the films on a thermal conductivity vs. power factor space, we showed their properties to rest in a gap between two classes of nano-featured silicon in the thermoelectrics

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literature: doped thin films and nanowires. Further, we have suggested a potential opportunity to further optimize the relationship between thermal conductivity and power factor by altering the post-deposition treatment processes.

Second, the perspective was shifted from nanoscale materials to microscale devices and the design optimization space was evaluated for thermoelectric generators fabricated using micron-scale thin-film technology. Through thoughtful design of factors such as the fill fraction and number of thermocouples, among others, a roadmap was developed for optimization of thin-film generators used for near-ambient thermal energy harvesting. The appropriateness of the common thermoelectric “figure of merit”  $ZT$  on the device scale was called into question and examples provided which showed significantly different performance for device designs using materials with different constituent properties resulting in equivalent  $ZT$  values.

Third, we discussed the fabrication process for prototype devices using a thin film deposition technique and designed with the developed device optimization methodologies as a guide. Five working prototype generators were presented which featured parametric variation in the number of thermocouples (Devices 1-3) and the bonding force used in flip-chip assembly (Devices 4 and 5). We first characterized their electrical resistance using a pulsed current four-point probe method to mitigate interference from the Seebeck effect. We then demonstrated the first known use of infrared microscopy as a tool for the characterization of cross-plane structure microfabricated thermoelectric generators, extracting temperature differences directly across the device and implementing a reference layer in series for simultaneous characterization of thermal resistance. Two of these early-stage prototype generators were shown to produce more than 1 mW actual load power from less than 10 °C device temperature difference.

Finally, higher-level discussions of system-level thermomechanical packaging and integration with power conditioning circuitry were provided to enhance awareness of further optimization opportunities for small form factor thermoelectric systems as autonomous power supplies.



## *CHAPTER 5*

The field of research in distributed-scale thermoelectric energy harvesters for autonomous sensor networks, wearable electronics, medical devices, and other low power electronics is rapidly expanding and represents a complex space of optimization targets to bring real devices to market. My hope is that the work presented in this dissertation will be useful in the broader pursuit of energy harvesting within the hugely-underutilized domain of near-ambient thermal energy sources.

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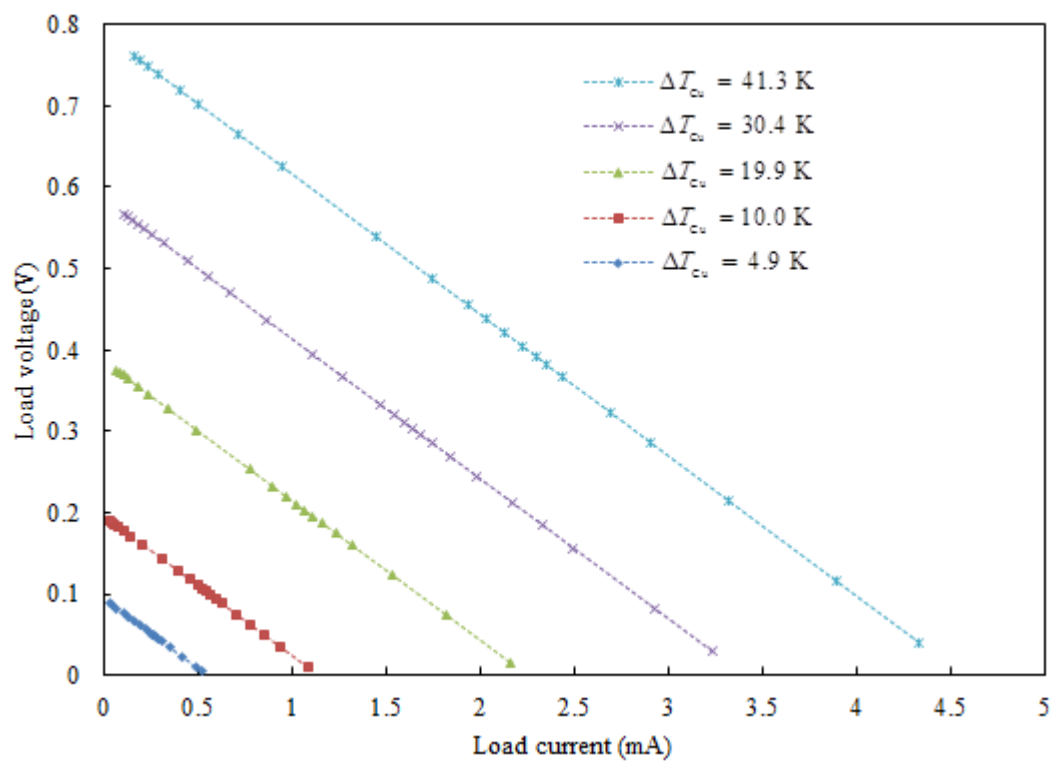
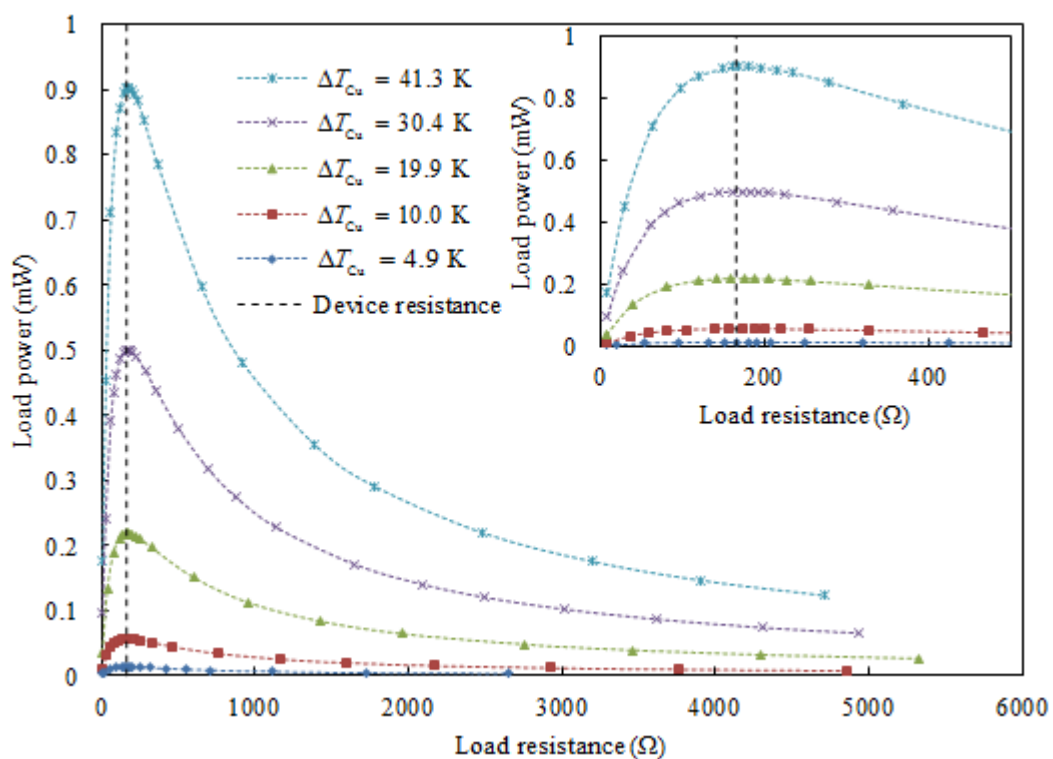
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# **Appendix A:**

## **Device Performance Plots**

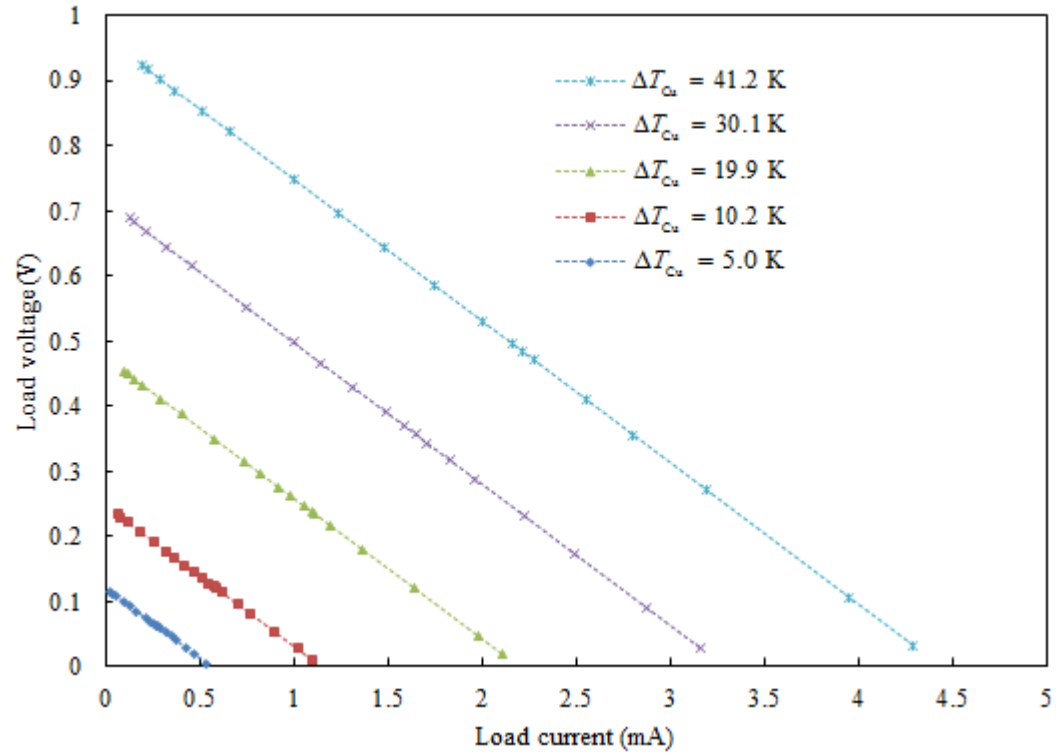
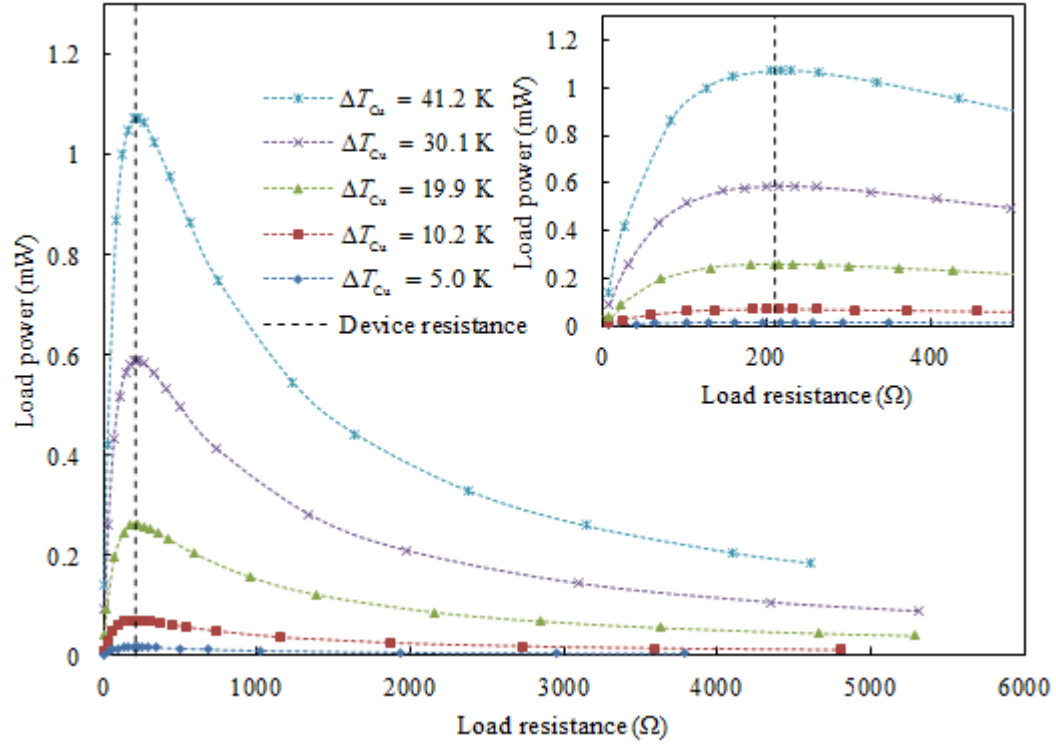
This section includes the full performance characterization plots for the set of 5 devices examined, in the form of load power vs. load resistance curves and load voltage vs. current lines. The legend entries indicate the temperature difference measured by thermocouple from hot reservoir copper block to cold reservoir copper block.

Device 1:

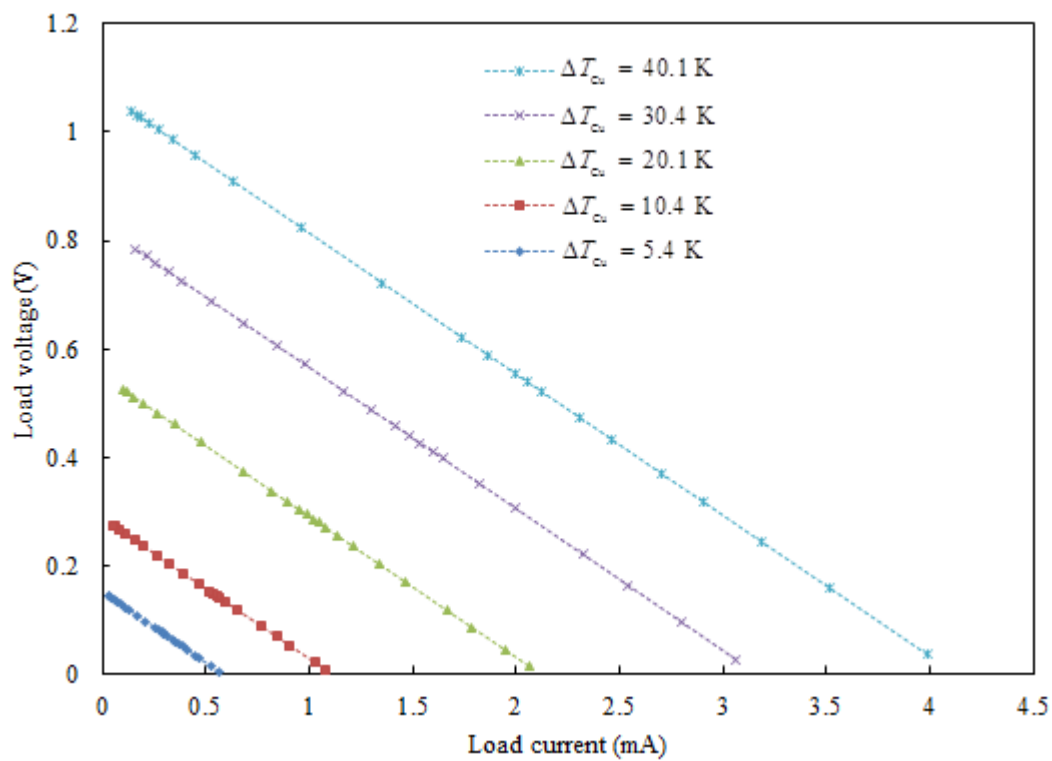
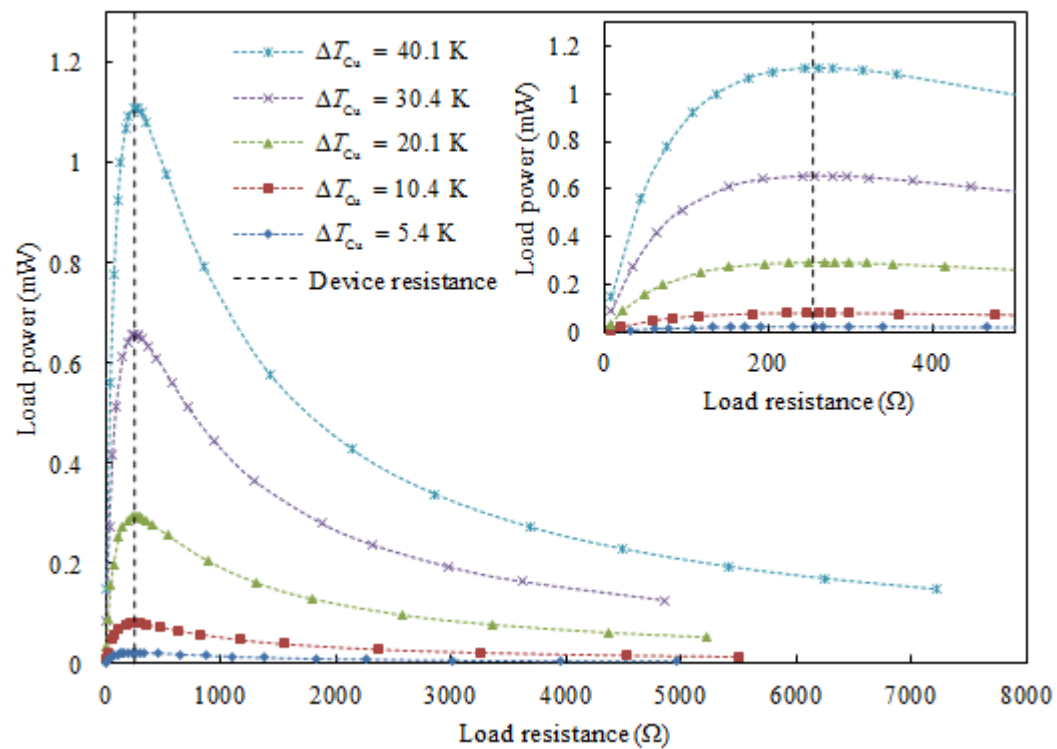




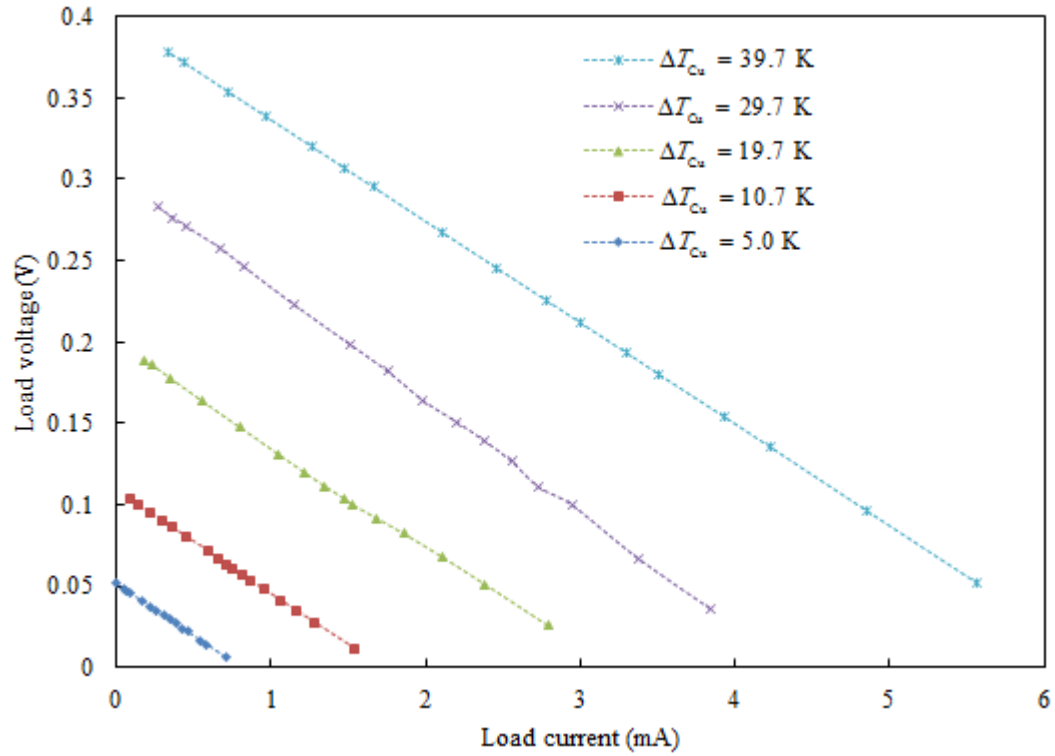
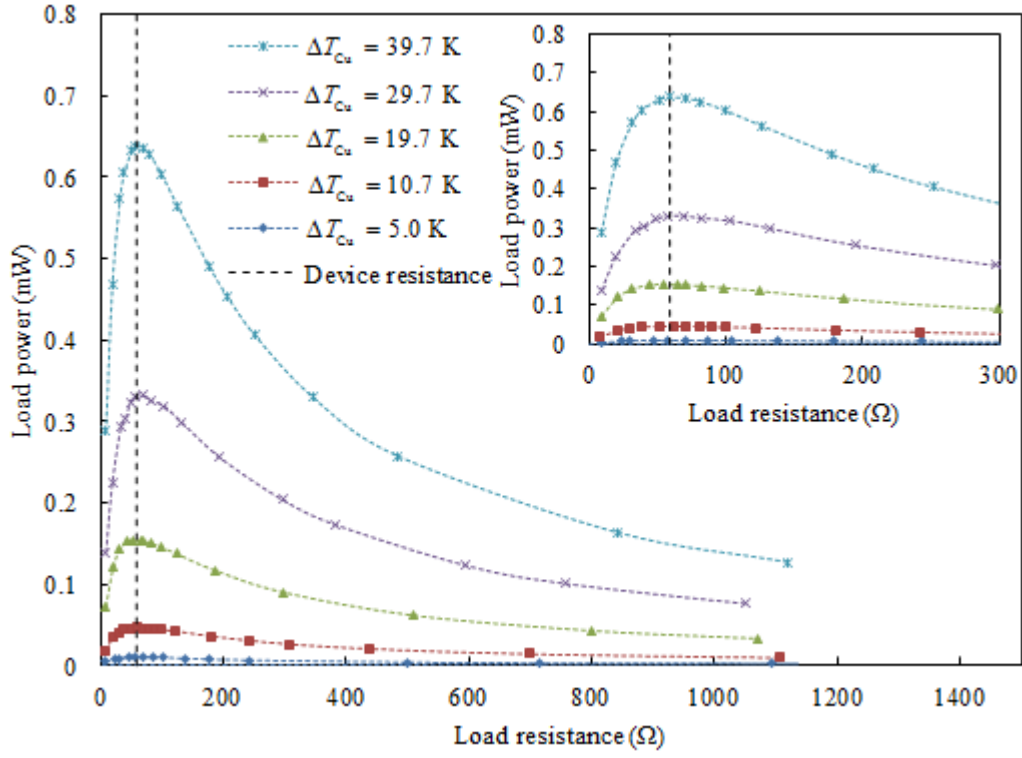
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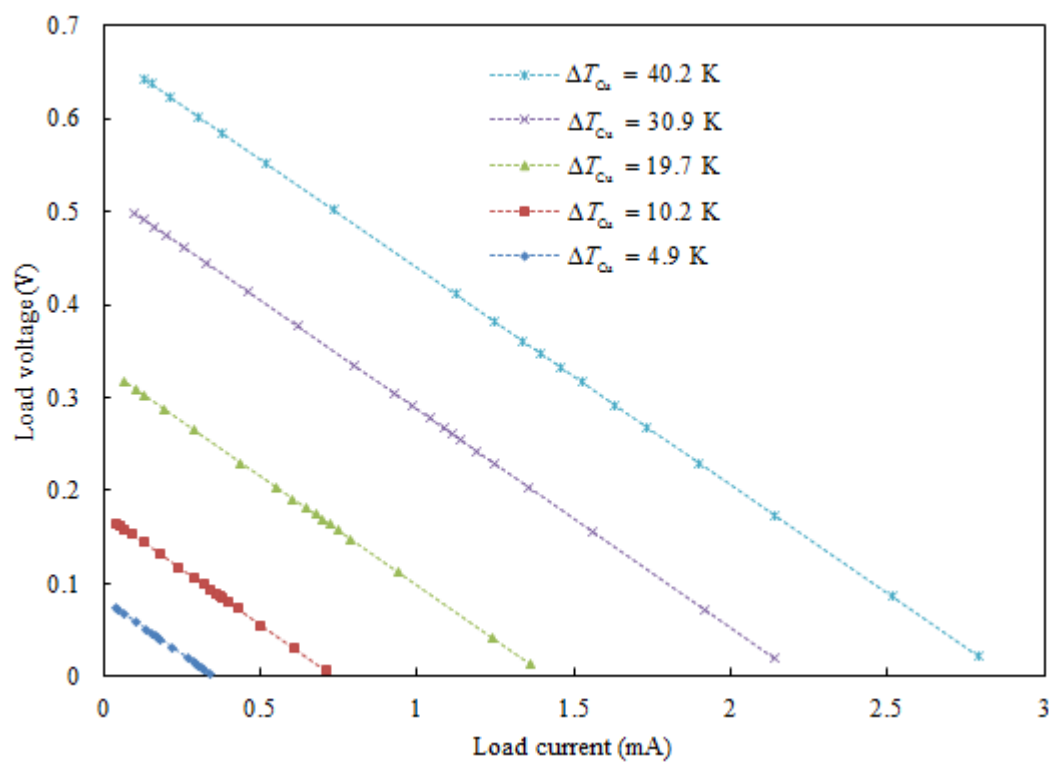
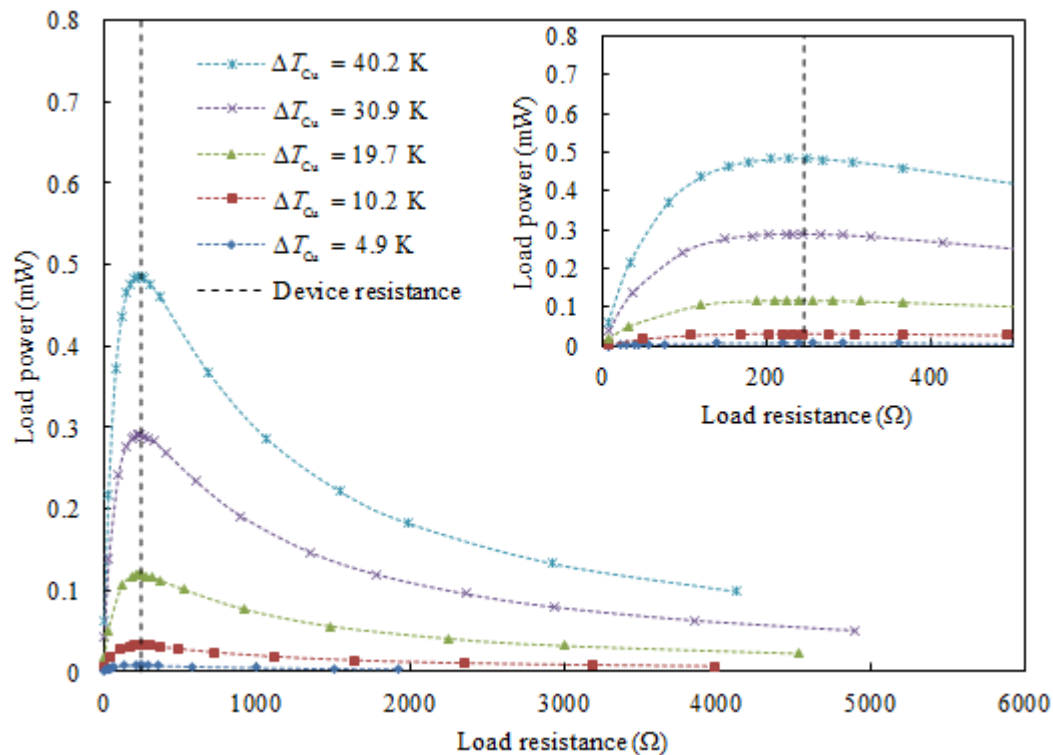
**Device 3:**



**Device 4:**



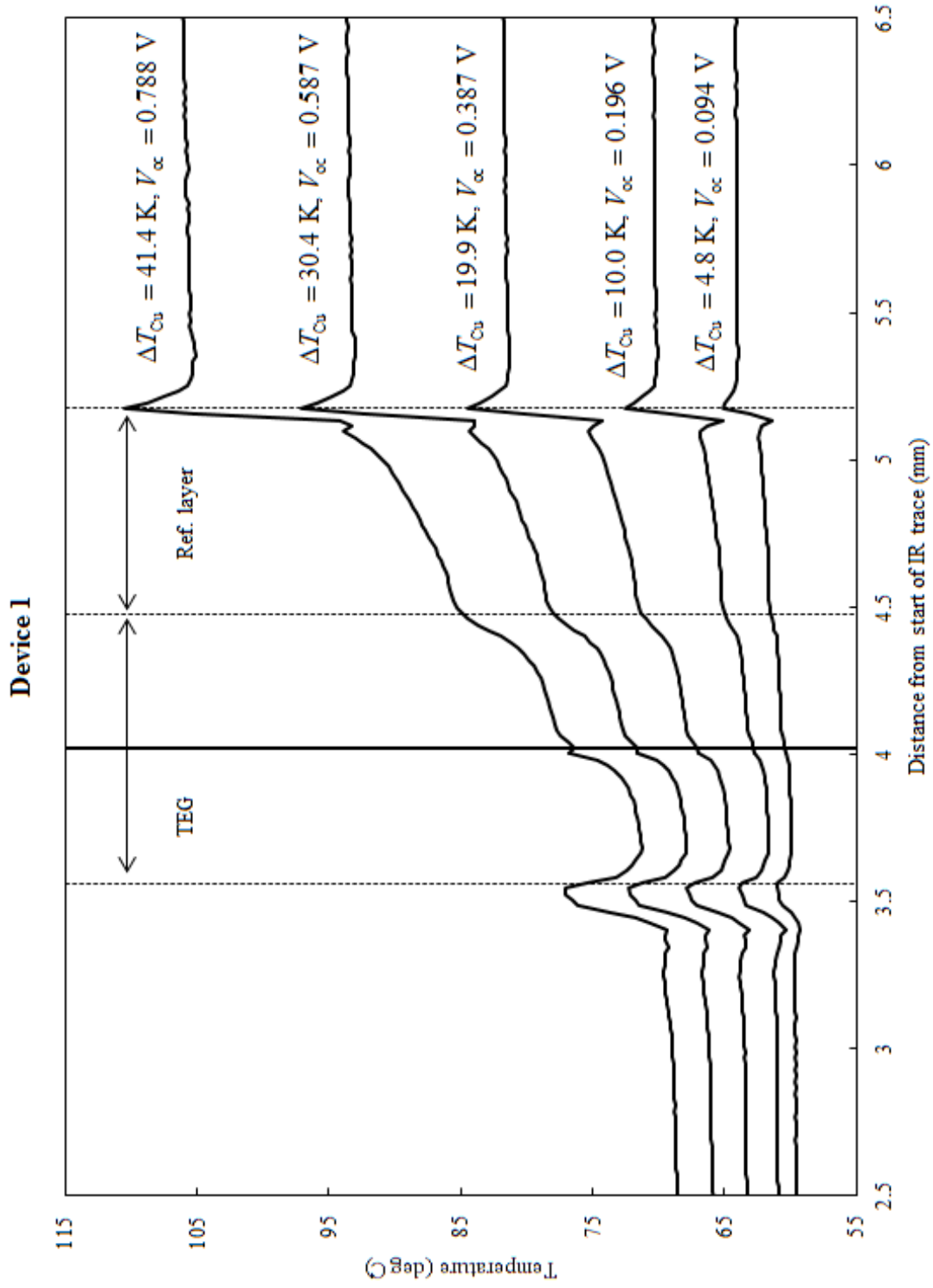
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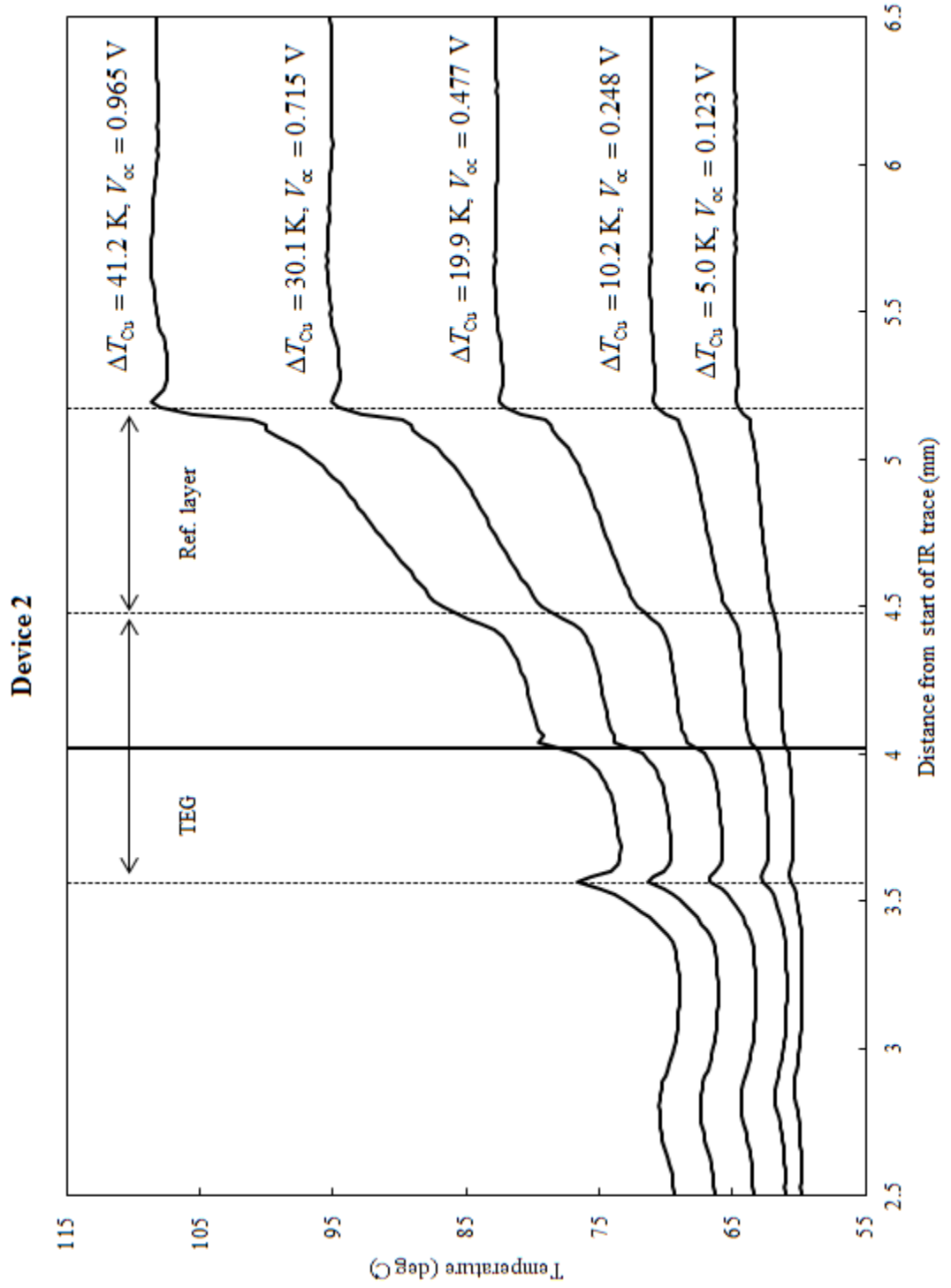


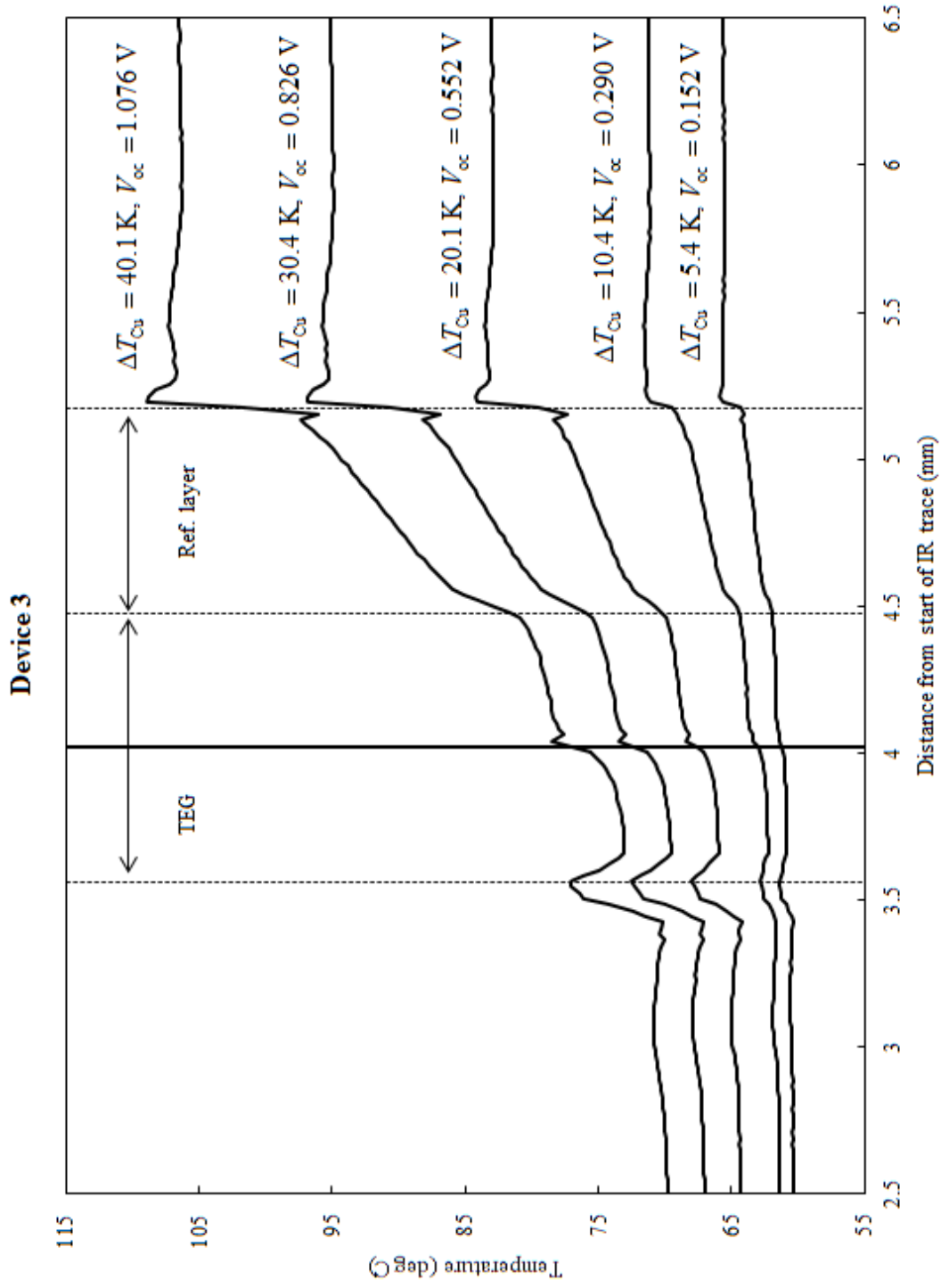
## **Appendix B:**

# **Device Temperature Traces**

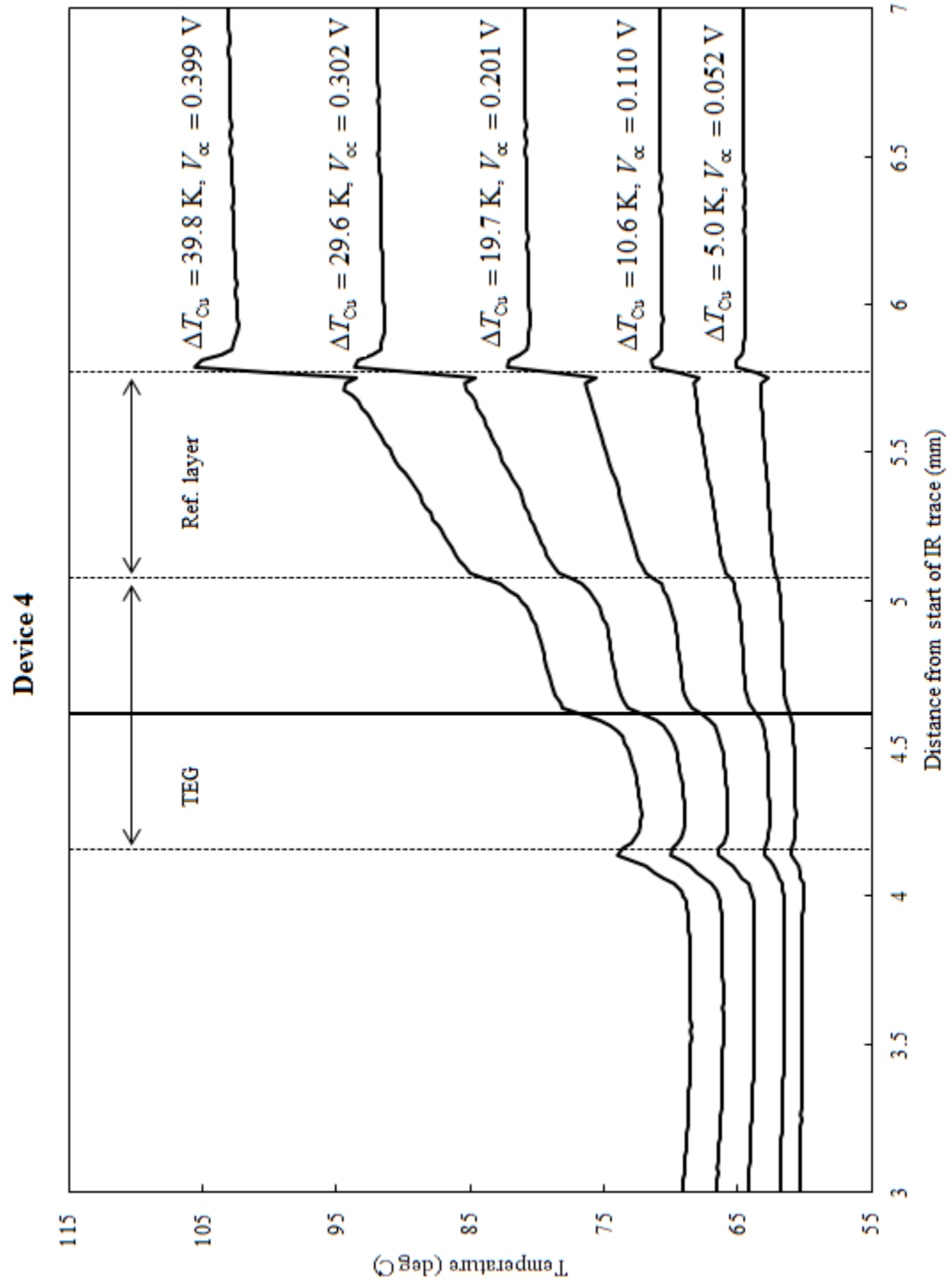
This section provides all of the line-averaged IR temperature traces used to extract device temperature gradients and thermal resistance information. Also included adjacent to each temperature trace is the recorded steady-state copper block temperature difference as measured by thermocouples, and the open-circuit voltage.



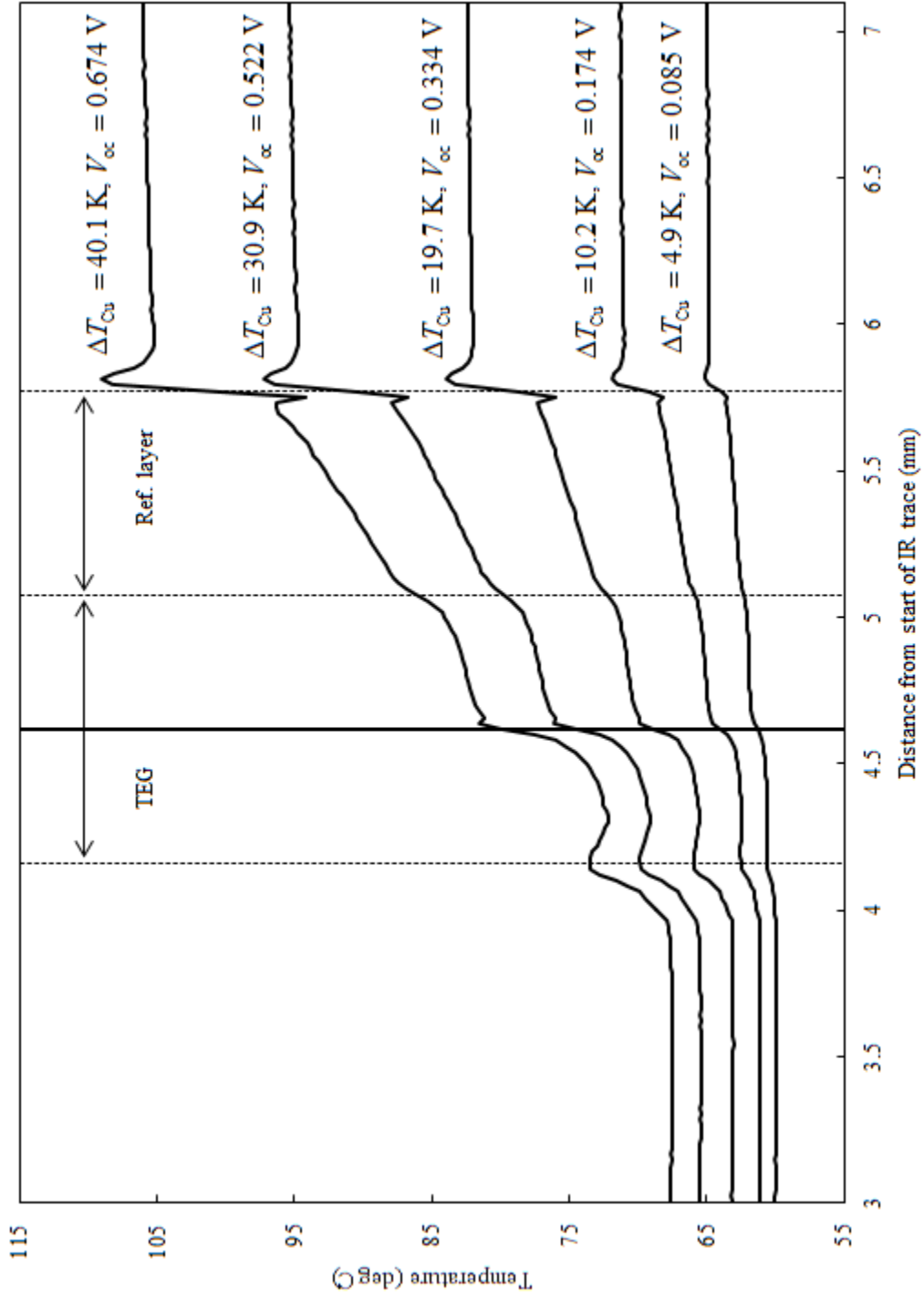








Device 5



## Appendix C:

### Pun with Phonons

On October 2, 2013 I took over the role of sending e-mail announcements for weekly NanoHeat group meetings. Mostly out of self-amusement, I hastily put my mark on the first notice with the simplest thermal physics joke I could think of:

“Why did the phonon cross the road? To get to the colder side!”

Upon hearing a laugh from the other end of the office, I knew that I had raised the stakes and would have to continue producing a new joke each week. Two and a half years later and around 90 jokes in all, some stretched farther than a spin-coated polymer, I handed off my announcement responsibilities in the group, although my ears have become irreversibly trained to jump on any opportunity for a technical pun. This section includes all of the group meeting e-mail jokes from my tenure as Group Meeting Announcer. Compiled, they not only capture a part of my personality as ingrained as my passion for heat transfer or homemade pizza, but at many points serve as a sort of time capsule for the topics in which I was engaged at the time. I hope someone enjoys them as much as I did.

## *APPENDIX C: PUN WITH PHONONS*

10/9/2013

Given a semi-infinite group meeting calendar with oscillating lunch condition, predict the menu  $M(R,t)$  for room  $R=530-212$  and time  $t=\text{noon}$ . Or just acknowledge that there will be lunch!

10/23/2013

So Planck's constant walks into a bar...

10/30/2013

I prefer to spend my time with protons; electrons are too negative.

11/13/2013

Always remember what the sensei said to his pupil in "Quantum Kid": Fermi-on, Fermi-off... Fermi-on, Fermi-off...

11/20/2013

What did the electron say to the resistor? Ohm sweet ohm!

12/3/2013

I think all of AC/DC's songs should have been about Tesla and Edison. I guess they wouldn't have had the same power though...

1/15/2014

What did the photon write on his holiday card? "Happy Nu Year!"

1/22/2014

Two electrons get into an elevator, and the first asks the second, "Going up?" "No, I don't have the energy for that."

## *APPENDIX C: PUN WITH PHONONS*

1/29/2014

What did Silicon say to reporters after leading a failed orchestra performance?  
"Sorry, I'm just a semi-conductor."

2/5/2014

What do you call thermal conductivity measurements with no acoustic phonon contribution? MIME domain thermoreflectance!

2/12/2014

Why was silicon's medal taken away at the Winter Olympics? Further tests confirmed excessive doping.

2/19/2014

What is the phonon's favorite cheer at baseball games? The wave!

2/26/2014

We know about the phonon, but what is the electron's favorite cheer at baseball games? The wave, but only when no one is watching!!

3/5/2014

What did the exact differential say when asked where he wanted to go for lunch?  
"I'm impartial."

3/12/2014

What is a theoretical physicist's favorite time of the school year? String Break.

4/2/2014

Why do electrons prefer the Sommerfield model? They think going around in circles is Bohr-ing.

## *APPENDIX C: PUN WITH PHONONS*

4/9/2014

What is an ideal turbine's favorite vacation destination? The isentropics!

4/16/2014

Phonon 1: "I just told my boss I was trapped in a box and couldn't make it to work yesterday"

Phonon 2: "Debye it?"

4/23/2014

What kind of subatomic particle runs the friendliest car wash? Neutrons. There's never any charge!

4/30/2014

How does one find out what noodles are made of? Ramen spectroscopy!

5/7/2014

What do crystals cheer at the end of a great performance? "Bravais! Bravais!"

5/14/2014

Why did Mr. and Mrs. Electron name their son "Bandgap"? They thought he had a lot of potential!

5/21/2014

What is the electron's favorite class in school? Current events!

6/4/2014

What was the casting director's main critique of Nano Wire's acting abilities? He was too one-dimensional.

## *APPENDIX C: PUN WITH PHONONS*

6/11/2014

What parameter determines a thermoelectric material's likelihood to attend an alt-rock concert? Its Seebeck coefficient!

7/2/2014

Why was the spelling of IBM using atoms on the cover of Nature? It just wasn't big enough for Nano Letters.

7/9/2014

What is the phonon's favorite sandwich? Bacon-Lattice-Tomato!

7/23/2014

What did Darth Vader say when he met Quark? "The force is strong with this one."

7/30/2014

What is a phonon's least favorite cereal? Anything with lots of grains.

8/6/2014

What do you call a microstructured Thermal Interface Material around the holidays? A Tiny TIM!

8/13/2014

What is the most irritable type of ion? A cat-ion; even when they're positive, they're negative.

9/24/2014

What did the experimentalists name their band? The Rock-in' Amplifiers!

## *APPENDIX C: PUN WITH PHONONS*

10/1/2014

Which region of the USA would make the best conductor? New England; it has the highest density of States!

10/15/2014

What is a beaver's favorite (or least favorite, maybe) thermoelectric phenomenon? The PELTier effect!

10/22/2014

What was the big news in Quantumville? Little Timmy Oscillator got stuck in the potential well!

10/29/2014

What did the ion provide in response to a court summons? An electro-deposition!

11/5/2014

Why is a football team with lots of running backs a good electrical conductor? High carrier concentration!

11/12/2014

What unit of energy does Buckingham Palace use? Crown Joules!

1/7/2015

Why was the phonon fired from Nanowire Railroads? He was too scattered to conduct...

1/14/2015

What did the wavefunction say in response to one of Marc's puns? "Psi...."



## *APPENDIX C: PUN WITH PHONONS*

1/28/2015

What TV show is most popular among young phonons? Boson the Clown!

2/4/2015

What was the phonon's favorite internet fad? Planck'ing!

2/18/2015

Why don't electrons like to eat at steakhouses? They have a relatively low meat capacity at room temperature.

2/25/2015

Why do nanowires prefer glasses? They tend to have high contact resistance!

3/4/2015

How do phonons say hello? They wave!

3/11/2015

What was the Fermion's favorite musical genre? Electronica!

4/1/2015

What is the LEGO man's favorite solid-state physics concept? Block theorem!

4/22/2015 (author acknowledges this was an unwitting repeat of 10/22/2014)

Why were all the electrons gathering in the village square? Little Timmy fell down the quantum well!

4/29/2015

What is a heat transfer specialist's favorite dessert garnish? Convectioner's sugar!

## *APPENDIX C: PUN WITH PHONONS*

5/5/2015

Why couldn't the carbon nanotube find a job? He was awful at making contacts...

5/13/2015

Which superhero is most famous for getting into sticky situations? Kapton America!

5/20/2015

Why are arrogant crystals the best for XRD? They have the most Bragg scattering!

5/27/2015

What do electrons at a concert call intermission? The band gap!

6/3/2015

What was the phonon's favorite nursery rhyme? "Mary had a little  $\lambda$ "!

6/24/2015

Why didn't the phonon cross the plane? The medium was highly anisotropic!

7/8/2015

What is the Teenage Mutant Ninja Turtles' favorite technical conference? SplinterPACK!

7/15/2015

What is a long-wave phonon's favorite low-calorie alcoholic beverage? Absolut Zero!

7/22/2015

Where do semiconductors buy their clothes? The Band GAP!

## *APPENDIX C: PUN WITH PHONONS*

7/29/2015

What was the electron and high-energy photon's favorite song to sing at karaoke?  
Straight Outta Compton (Scattering)!

8/5/2015

Who did the electron dress up as for Halloween? Dirac-ula!

8/12/2015

What is it called when two phonons have been dating for a long time? They're  
going steady-state!

9/16/2015

What was glass's favorite TV show as a young highly-disordered material? Mighty  
Amorphous Power Rangers!

9/23/2015

What was the pop star Nano Stencil's biggest hit? Blurred Lines!

10/7/2015

What textbook did the young dielectric use in school? Hooked on Phononics!  
(inspired by Michael)

10/14/2015

What did the warm phonon say to the cold phonon? "Why the long wave?"

10/22/2015

What is the most useful Halloween decoration for performing lab measurements?  
A DAQ-o-lantern!

## *APPENDIX C: PUN WITH PHONONS*

10/29/2015

Why is (ideal) graphene like a frequent traveler? It's always in-plane!

11/5/2015

What was the con-artist's favorite characterization tool? Scamming Electron Microscopy!

11/12/2015

Where do all the high-energy phonons congregate at Target? The optical department!

11/19/2015

How do you diagnose problems with a tiny car engine? Using a transmission electron microscope!

12/3/2015

What is the least trustworthy piece of nanofab equipment? The FIB!

12/10/2015

Why don't p-type semiconductors write good plotlines? They're all full of holes!

1/13/2016

What is a polymer solution's preferred winter clothing? A spin coat!

1/21/2016 (author acknowledges repeat of 6/3/2015)

Why was Mary such a poor heat conductor? Because "Mary had a little  $\Lambda$ "!

## *APPENDIX C: PUN WITH PHONONS*

1/28/2016

What big-ticket event is periodically organized for thin films? The Superlattice Bowl!

2/11/2016

What popular 1970s film told the story of an unlikely phonon romance? “Thermal Grease”!

2/18/2016

What did the electron say when all the phonons started pushing him around? “What a drag...”

2/25/2016

How do carbon atoms get their news? From the nano-tube!

3/31/2016

What do chemists call it when opposites attract in a relationship? Ionic bonding!

4/7/2016

What chair did the 3-omega specialist hold in the orchestra? Third harmonica!

4/14/2016

How did the mechanical engineer assist in understanding the meaning behind Stonehenge? By using Computational Druid Dynamics!

4/28/2016

What was the poet’s favorite thin-film thermal metrology? Rhyme-domain thermoreflectance!

## *APPENDIX C: PUN WITH PHONONS*

5/12/2016

What was the name of the materials scientists' band that always played out of tune? Acoustic Mismatch Theory!

5/19/2016

How do dogs measure electrical properties of thin films? Using the van der Paw technique!