FABRICATION AND CHARACTERIZATION OF VERTICAL SILICON NANOWIRE ARRAYS: A PROMISING BUILDING BLOCK FOR THERMOELECTRIC DEVICES

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ABSTRACT

Thermoelectric devices, which convert temperature gradients into electricity, have the potential to harness waste heat to improve overall energy efficiency. However, current thermoelectric devices are not cost-effective for most applications due to their low efficiencies and high material costs. To improve the overall conversion efficiency, thermoelectric materials should possess material properties that closely resemble a "phonon glass" and an "electron crystal". The desired low thermal and high electrical conductivities allow the thermoelectric device to maintain a high temperature gradient while effectively transporting current. Unfortunately, thermal transport and electrical transport are a closely coupled phenomena and it is difficult to independently engineer each specific conduction mechanism in conventional materials. One strategy to realize this is to generate nanostructured silicon (e.g. silicon nanowires (SiNWs)), which have been shown to reduce thermal conductivity (κ) through enhanced phonon scattering while theoretically preserving the electronic properties; therefore, improving the overall device efficiency.

The ability to suppress phonon propagation in nanostructured silicon, which has a bulk phonon mean free path ~ 300 nm at 300 K, has raised substantial interest as an ultra-low κ material capable of reducing the thermal conductivity up to three orders of magnitude lower than that of bulk silicon. While the formation of porous silicon and SiNWs has individually been demonstrated as promising methods to reduce κ, there is a

lack of research investigating the thermal conductivity in SiNWs containing porosity. We fabricated SiNW arrays using top-down etching methods (deep reactive ion etching and metal-assisted chemical etching) and by tuning the diameter with different patterning methods and tuning the internal porosity with different SiNW etching conditions. The effects of both the porosity and the SiNW dimensions at the array scale are investigated by measuring κ of vertical SiNW arrays using a nanosecond time-domain thermoreflectance technique.

In addition to thermoelectric devices, vertical SiNW arrays, due to their anisotropic electronic and optical properties, large surface to volume ratios, resistance to Li-ion pulverization, ability to orthogonalize light absorption and carrier transport directions, and trap light, make vertical SiNW arrays important building blocks for various applications. These may include sensors, solar cells, and Li-ion batteries. Many of these applications benefit from vertical SiNW arrays fabricated on non-silicon based substrates which endow the final devices with the properties of flexibility, transparency, and light-weight while removing any performance limitation of the silicon fabrication substrate.

We then developed two vertical transfer printing methods (V-TPMs) that are used to detach SiNW arrays from their original fabrication substrates and subsequently attach them to any desired substrate while retaining their vertical alignment over a large area. The transfer of vertically aligned arrays of uniform length SiNWs is desirable to remove

the electrical, thermal, optical, and structural impact from the fabrication substrate and also to enable the integration of vertical SiNWs directly into flexible and conductive substrates. Moreover, realization of a thermoelectric device requires the formation of electrical contacts on both sides of the SiNW arrays. We formed metallic contacts on both ends of the SiNW arrays with a mechanical supporting and electrical insulating polymer in between. Electrical characterization of the SiNW devices exhibited good current-voltage (I-V) characteristics independent of substrates materials and bending conditions. We believe the V-TPMs developed in this work have great potential for manufacturing practical thermoelectric devices as well as high performing, scalable SiNW array devices on flexible and conducting substrates.

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Chapter 1. Introduction

1.1. Motivation

Prior to the industrial revolution, the world population growth and natural resource consumption were relatively insignificant compared to what they are today. This started to change with the invention of the steam engine and continued with the development of the internal combustion engine. These engines allowed society to transport and move goods efficiently around the world, sparking the future for rapid technological development and consumption of our natural resources [1]. Again in the mid-twentieth century, society hit another monumental landmark with the invention of the transistor. Since then, the number of transistors on an integrated circuit has been growing at an exponential rate, almost doubling every two years. This has led technology to grow at an unprecedented rate. Developed countries are continuing to make technology faster, cheaper and smaller, allowing individuals to consume more than ever. At the same time, modern technology is becoming available to non-developed countries, who can now gain access to electricity and health care, drastically improving their quality of life and life expectancy, resulting in a rapid increase in the population of the world. The combination of the rapid population growth and increased power consumption has had a severe impact on the pollution of our planet and the depletion of our natural resources. In order to further mitigate these risks, society needs to adopt clean energy technologies to replace the technologies consuming our natural resources while still meeting the demands from society [1].

The demand to improve efficiency in current systems is also highly desired. Thermoelectric devices, which are solid-state energy harvesting devices capable of converting a temperature gradient into an electrical voltage, offer the potential to achieve this goal. Currently, heat engines are used to produce ~90% of the world's energy in a useful form, of which ~60% is lost to the environment as waste heat, opening up promising opportunities for thermoelectric devices [2]. For example, a typical automobile has an efficiency of 20-25% due to the production of waste heat, of which the majority is expelled in the exhaust and radiator [2, 3]. The waste heat from the exhaust or radiator could be harvested with a thermoelectric device to convert this energy back into useful electricity, which would reduce the mechanical load placed on the alternator and increase the overall engine efficiency. The gas mileage would increase, allowing automobiles to be manufactured with smaller engines that would require less power.

Thermoelectrics have characteristic traits that make them promising in many applications. For example, typical heat engines become less efficient as they are scaled down, while thermoelectric devices maintain a relatively stable efficiency over a wider range of power generation levels, opening up opportunities for thermoelectrics in low power (< 1 kW) applications [4]. Figure 1-1a shows a representative illustration of the low power regime where the thermoelectric efficiency is more efficient than conventional heat engines [4]. The range of power levels where thermoelectrics are more efficient will only increase as the efficiency of thermoelectric materials continues to improve. Furthermore, the demand for systems capable of supplying small amounts of power is becoming more important as technology is allowing devices to decrease in size and

increase in performance. Examples of applications that fall into this range are shown in Figure 1-1b [5]. In addition, most of these applications require the devices to be wireless, portable, and long lasting: this mandates an onboard power source since they can no longer rely on power from the grid. While batteries are typically used in such applications, there are two major drawbacks: batteries (1) contain toxic materials and (2) need to be replaced. On the other hand, thermoelectric devices can harvest waste heat from their surrounding environment without a finite energy density, large components, and noise since they possess no moving parts [4, 6]. These characteristic traits have allowed thermoelectrics to be used in some maintenance-free applications for up to 20 years or more, even under extreme conditions with very little performance degradation [6]. With current performance and cost, the primary applications for thermoelectric devices are for space exploration and wireless devices in harsh and dangerous environments where the benefits outweigh the current cost and performance limitation. It is unlikely that thermoelectric devices will soon become cost-effective and efficient enough to compete with conventional large scale heat engines. However, if the material cost, manufacturing and integration technologies can be substantially improved, then thermoelectric devices could harvest the ~60% heat lost from conventional heat engines. With future improvements in the efficiency and cost, thermoelectrics can become commonly used energy harvesting devices, capable of powering a variety of applications such as implantable biomedical devices, remote sensors in hard to access locations, personal hand held electronics, and hybrid conventional heat engines.

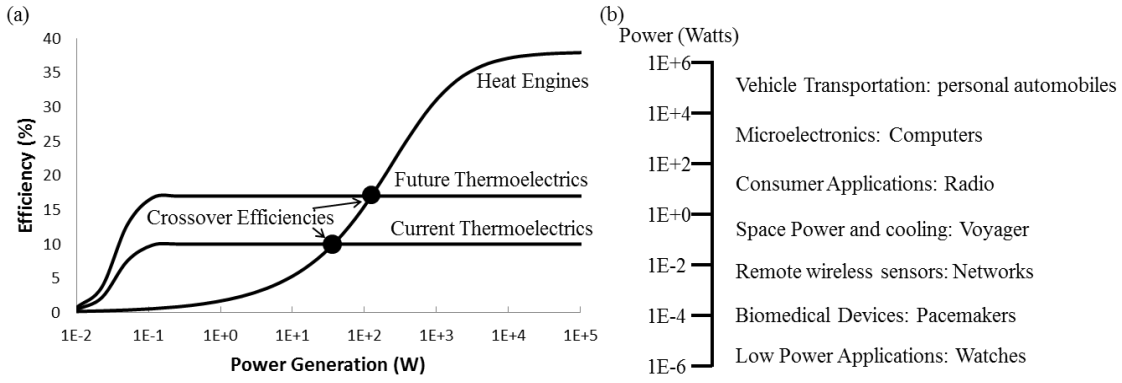


Figure 1-1. Relative efficiency and possible applications of thermoelectric materials. (a) Power generation vs. efficiency plot illustrating how thermoelectric devices can become more efficient than conventional heat engines as the power consumption is scaled down to low power applications [4]. (b) Representative applications requiring a wide range of power consumptions that would benefit from thermoelectric devices [5].

1.2. Background on Thermoelectrics

1.2.1. The Thermoelectric Theory

The thermoelectric effect is the physical phenomenon describing the relationship between a temperature gradient in a material and a corresponding electrical voltage. A thermoelectric device is a solid-state configuration of thermoelectric materials, which are often semiconductors, that utilize this phenomenon to convert a temperature gradient into a useful electrical voltage and current, or vice versa. The fundamental working principle is based around the movement of charge carriers within the thermoelectric materials: electrons in n-type materials and holes in p-type materials. In the presence of a temperature gradient, the respective charge carriers diffuse across the material from the warmer side to the cooler side. At the same time, an electrostatic repulsion potential

prevents a buildup of charge carriers at the cooler side. An equilibrium is reached between the diffusion potential and the electrostatic repulsion potential of the charge carriers, known as the thermoelectric or Seebeck effect [7]. In order to maximize the efficiency, thermoelectric materials need to preserve their temperature gradient by impeding thermal energy carriers while allowing the electrical charge carriers to flow with relative ease. Therefore, semiconductor based materials are most commonly used since metals have high thermal conductivities and low Seebeck coefficients while insulators restrict the flow of charge carriers due to their low electrical conductivity. A typical thermoelectric device consists of alternating p- and n-type semiconductors that are connected electrically in series and thermally in parallel (Figure 1-2). This configuration allows the holes and electrons to flow in opposite directions within their respective material, resulting in the flow of an electric current for power generation [6].

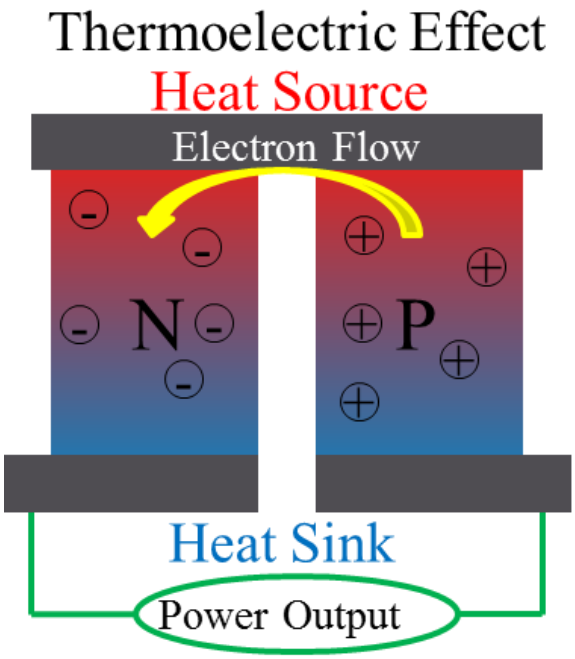


Figure 1-2. Schematic illustrating a representative thermoelectric device. A temperature gradient is applied across alternating p- and n-type semiconductors that are connected electrically in series and thermally in parallel.

The efficiency of a thermoelectric device is closely related to the semiconductor's material properties. In a non-degenerate semiconductor, phonons are the dominant thermal energy carrier. Ideally, a good thermoelectric device should behave as a "phonon glass", where phonons possess a very short mean free path such as found in glass and minimizing the thermal conductivity, but also as an "electron crystal" where electrons can travel over long distances unimpeded and maximizing the electrical conductivity [7]. The thermoelectric figure of merit, ZT, is often used to describe the conversion effectiveness:

$$zT = \frac{\alpha^2 \sigma T}{\kappa} \qquad 1\text{-}1$$

which is a dimensionless unit containing the Seebeck coefficient (α), mean absolute temperature (T), electrical conductivity (σ), and thermal conductivity (κ) [2, 5, 6, 8-12]. The thermoelectric figure of merit can be inserted into a modified Carnot efficiency equation to get the overall expected thermoelectric efficiency:

$$\eta = \frac{\Delta T}{T_h} \cdot \frac{\sqrt{1+ZT}-1}{\sqrt{1+ZT}+T_c/T_h} \quad \text{1-2}$$

where the first term is simply the conventional Carnot efficiency and the second term is the correction factor based on the material's thermoelectric performance [7]. Current high performing thermoelectric materials have a zT close to 1, which needs to improve to greater than 3 to be competitive with conventional generators [7, 9, 13].

It is challenging to improve zT since the three intrinsic material properties that make up zT (α, σ and κ) are closely coupled. Thus, as one parameter is tailored to improve zT another parameter counteracts the improvement [7]. For example, the Seebeck coefficient is the magnitude of the thermoelectric voltage under a temperature gradient. This effect is formed from the electric field that is generated when charge carriers are separated from their oppositely charged counterpart. Therefore, as the semiconductor carrier concentration (n) increases, α decreases as show by:

$$\alpha = \frac{8\pi^2 k_B^2}{3eh^2} m^* T \left(\frac{\pi}{3n}\right)^{2/3} \quad \text{1-3}$$

where k_b is Boltzmann's constant, e is the elementary electron charge, h is Planck's constant, and m^* is the effective mass of the charge carrier [7]. At the same time, when the carrier concentration is increased, σ is also increased as shown by:

$$\sigma = ne\mu \tag{1-4}$$

where μ is the carrier mobility. Therefore, the power factor ($\alpha^2\sigma$) reaches a peak, typically in the heavily doped semiconductor range as show in Figure 1-3a [7]. In addition to α being coupled to σ through the carrier concentration, κ is also coupled σ through the transport properties of the material. In any solid material, κ has two contributions:

$$\kappa = \kappa_e + \kappa_l \tag{1-5}$$

where κ_e is the transfer along with charge carriers and κ_l is transfer via phonons traveling along the lattice. The electron component κ_e is directly related to σ through the Wiedemann-Franz law:

$$\kappa_e = L\sigma T = ne\mu LT \tag{1-6}$$

where L is the Lorenz factor, typically $2.44 \cdot 10^{-8}$ $J^2K^{-2}C^{-2}$ for free electrons in bulk metals [14]. The primary contribution to the total thermal conductivity is κ_e in metals but κ_l in insulators and semiconductors. If κ_l can be reduced within a semiconductor without changing the electrical properties (α and κ) then zT would be increased (Figure 1-3b). However, increasing the ratio of σ/κ is a challenge since low κ_l materials are typically amorphous and insulating in nature, leading to low electrical properties compared to crystalline materials and therefore low zT values. Therefore, an efficient semiconductor

thermoelectric material possesses the electrical transport properties of a good crystalline material while being capable of effectively interfering with the phonon propagation to reduce the thermal conductivity [7].

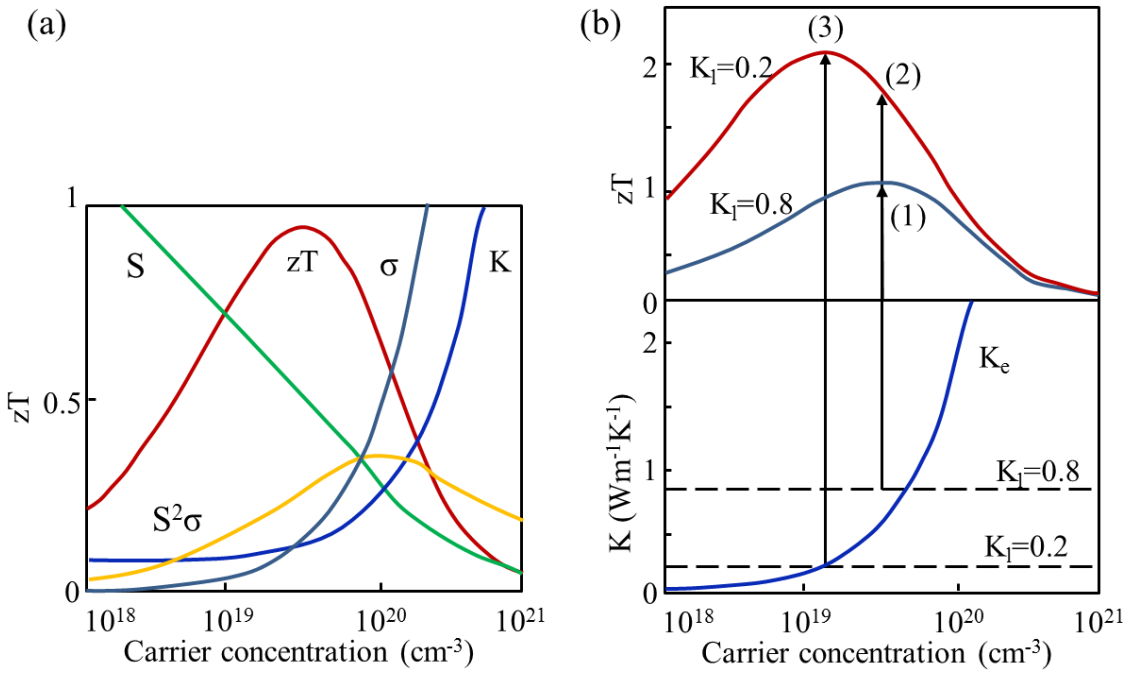


Figure 1-3. (a) Representative illustration of the dependence of zT, α, σ, and κ over a range of carrier concentrations. Note that zT reaches a maximum value within a material due to the dependence between α, σ, and κ. (b) Illustration demonstrating that decreasing the lattice thermal conductivity can independently improve zT [7].

1.2.2. State-of-the-Art Thermoelectric Materials

Recent research on improving thermoelectric materials has focused on achieving three main goals. The first approach was sparked by Hicks and Dresselhaus in 1993 when

they suggested that nanostructured materials exhibit quantum confinement effects, which could provide a method to independently increase α without decreasing σ [15]. The second approach is to increase the Seebeck Coefficient using phonon drag to transfer momentum from phonons to electrons [16]. This will slow down the phonon propagation while pushing the electrons forward. Unfortunately, this effect is only significant when the electron-phonon scattering is relatively high compared to the other phonon scattering mechanisms. Therefore, phonon drag only has a significant contributions when the electron-phonon scattering is dominate, which occurs around 1/5 ΦD, where ΦD is the Debye temperature (~645°K for Si). Below 1/5 ΦD there are too few phonons for drag and above 1/5 ΦD the phonon-phonon scattering becomes the primary scattering mechanism. Low dimensional structures also have a relatively minor contribution from phonon drag since the low frequency phonons, which are the mainly responsible for phonon drag, tend to scatter on the low dimensional surfaces [16]. The third, and more sought after approach, is to increase σ/κ by typically reducing κ_l without reducing the electrical conductivity. The most common and successful approach to achieve an increase in σ/κ is with heavy-element based materials, in particular various alloys of Bi_2Te_3 which have a zT close to 1 at room temperature [17]. In general, these materials create atomic disorder in the lattice by inserting point defects such as heavy elements. These effectively act as dampers to suppress the phonon propagation while still maintaining the crystalline structure to preserve the electrical conductivity. While somewhat successfully, this approach has major drawbacks to scalability: the heavy element based materials tend to be rare earth materials that are rather toxic, which makes the technology expensive, hard to mass produce, undesirable and detrimental to our natural resources (Figure 1-4).

An alternative approach is to engineer thermoelectric materials that are comprised of cheap, abundant, and environmentally friendly materials that can be mass produced despite having low zT values. These materials include oxides, silicides and polymers [17, 18]. While these methods are promising for their cost, scalability, and lack of toxicity, their zT values are far from practical due to their low carrier mobility or high lattice thermal conductivities [12]. Figure 1-4 shows another group of materials, Si/Ge, that can be used for thermoelectrics. Si, in particular, is always a great material to invest a technology on since it is the second most abundant element on earth after oxygen. Also years of knowledge and technology have been devoted to processing devices based around Si, making it very well characterized. However, crystalline Si in bulk form is a poor thermoelectric due to the high κ_l and low α, resulting in a zT around 0.01 [19].

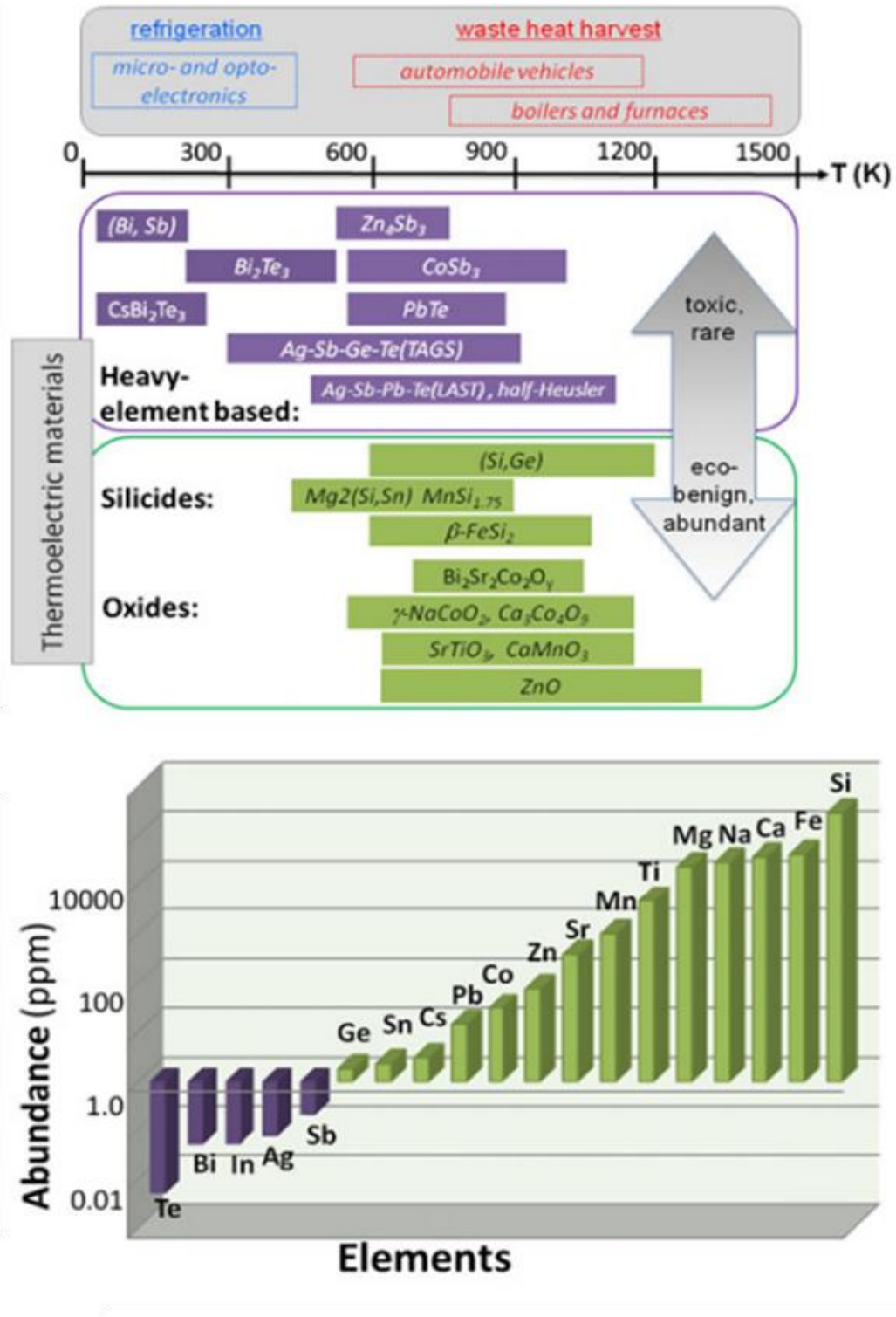


Figure 1-4. Summary of promising thermoelectric materials and their relative element abundance. Heavy element based thermoelectric materials are currently the best

performing thermoelectric materials but suffer from cost, limitations to scalability, and toxicity, while silicides and oxides are cheap, abundant, and environmentally friendly but suffer from poor performance. Bulk Si, although not very efficient, has the benefits of being very abundant with years of knowledge and technology invested into modifying Si for desirable application. Reprinted from [17].

1.2.3. Potential of Nanostructured Silicon

Nanostructuring of semiconductors into thin films, wires, and quantum wells has been used since the 1960s to achieve unique material properties not possible in bulk form [11]. Nanostructured silicon, in particular, has the potential to reduce κ_l without reducing $\alpha^2\sigma$ due the relatively long average bulk Si phonon mean free path (λ_{bulk_Si} = ~300 nm) compared to the average electron mean free path (~10 nm). The large difference in these mean free paths allow Si nanostructures to be fabricated with critical internal and/or external dimensions larger than the average electron mean free path but smaller than the average phonon mean free path (λ). Under these conditions, the nanostructured dimensions will increase phonon scattering at the surfaces resulting in a reduced average phonon mean free path (λ_{nano_Si}) as shown by Matthiessen's rule:

$$\frac{1}{\lambda_{nano\_Si}} = \frac{1}{\lambda_{bulk\_Si}} + \frac{1}{d} \qquad 1\text{-}7$$

where d is the critical nanoscale dimension. The thermal conductivity will be reduced proportionally to the reduction in λ through the following equation:

$$\kappa = \frac{1}{3} C v \lambda \qquad 1\text{-}8$$

where C is the phonon specific heat capacity and ν is the phonon group velocity. An illustration demonstrating enhanced phonon scattering within nanostructured Si is shown in Figure 1-5.

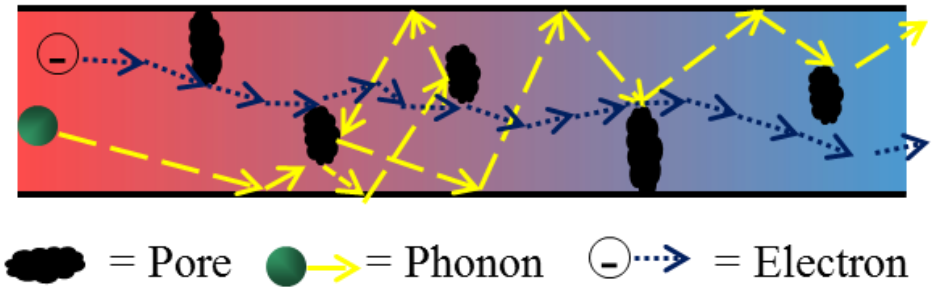


Figure 1-5. Schematic illustrating the electron and phonon transport in nanostructured Si. Notice the electron can move relatively easily through the structure without being affected while the phonon scatters at various internal and external boundaries, leading to a reduced average phonon mean free path.

Si-Ge superlattices were one of the first nanostructured Si materials developed with the goal of reducing κ_l for thermoelectric applications. These structures have layers ranging from 20 to a few hundred angstroms thick and estimated κ_l around the equivalent alloy composition [20, 21]. While the superlattice structures hold promise to reduce κ_l, the time-consuming and expensive molecular-beam-epitaxy process makes it unlikely to be cost-effective for scalable thermoelectric devices. On the other hand, porous Si is a cost-effective nanostructured Si material capable of reducing κ_l up to three orders of magnitude compared to bulk Si [22-25]. Computational results of ordered porous Si has

been shown to have relatively little degradation in the electrical properties making it promising for thermoelectrics [26-28]. However, typical porous Si has random, disordered pore formation with deteriorated electrical properties [25, 29-32]. Researchers have expanded the porous Si concept by patterning two-dimensional periodic larger microporous thin films to alleviate the electrical deterioration concern [33-35]. These films have shown an increase up to 50 times in performance with a zT of 0.4 [35]. While promising, these two-dimensional structures are formed using expensive silicon-on-insulator wafers and would be a challenge to scale up for three-dimensional configurations.

Si nanowires have recently received substantial interest as building blocks for thermoelectric devices with material properties that could closely resemble an ideal "phonon glass, electric crystal" material. Experimental measurements have demonstrated that a single Si nanowire could have as much as a 100x decrease in thermal conductivity compared to the bulk Si with the phonon contribution reduced close to the amorphous limit [19, 36, 37]. In particular Si nanowires with rough surfaces have shown to have a more substantial thermal conductivity reduction compared to smooth Si nanowires fabricated with similar diameters [19, 38-42]. However, the observation of reduced thermal conductivity has been limited to a single nanowire, so this theory needs to be tested over bulk nanostructured nanowires to evaluate the actual performance of a practical device.

1.3. Opportunities and Challenges

1.3.1. Vertical Si Nanowire Array Based Thermoelectric Devices

Preliminary research has demonstrated that nanostructured Si, particularly nanowires, are a promising low cost, non-toxic material for future thermoelectric materials. It is believed that Si nanowires with rough surfaces are capable of achieving a 100x reduction in the thermal conductivity, which would increase zT to around 1. While this current projected efficiency is on par with the best performing heavy element based thermoelectric materials, the drastic reduction in cost and environmental impact would make Si based thermoelectric devices applicable for large range of everyday applications. However, in order to achieve the substantial improvement in zT, several fundamental and fabrication challenges need to be addressed. First, the fundamental understanding of the Si nanowire fabrication methods needs to be improved to accurately and repeatedly fabricate and characterize the nanoscale features within the Si nanowires. Second, highly dense vertical Si nanowire arrays need to be fabricated to enable array-scale characterization. Third, the general trends of the Si nanowire features need to be investigated to determine the impact on the thermal conductivity. Fourth, fabrication methods need to be developed to remove the residual and performance-limiting Si substrate from the Si nanowire arrays without disturbing the array morphology. Finally, Si nanowires arrays need to be directly integrated between metal electrodes for complete thermoelectric device assembly as well as electrical characterization while still maintaining their vertically aligned morphology and uniform length.

1.3.2. Additional Vertical Si Nanowire Arrays Based Applications

In addition to reducing thermal conductivity, vertical SiNW arrays possess unique material properties opening up new opportunities as potential building blocks for numerous other applications including sensors [43-50], solar cells [51-59] and Li-ion batteries [60-66]. For example, ultra-sensitive chemical and biological sensors are possible due to the high surface area to volume ratios and the reproducible electronic properties allow Si nanowires to be uniquely sensitivity to surface analyte adsorption. Conventionally Si nanowire based sensors are fabricated by depositing nanowires suspended in a solution on a planar substrate that are subsequently connected between metal source and drain electrodes [44, 47]. While promising, commercialization of the planar Si nanowire configuration has been limited due to slow processing times, unreliable results from irreproducible nanowire dimensions and surface chemistry, size dependent noise sources, and substrate effects [49]. The ability to overcome the challenge of separating vertical Si nanowire arrays from the Si substrate is necessary to enable metal electrodes to contact both sides of the array directly, minimizing the above problems and exhibiting high sensitivity capable of detecting as little as a few parts per billion [49, 50].

Vertical Si nanowire-based solar cells are another promising application, leveraging the Si nanowire capabilities to enhance light absorption and decouple the direction of light absorption from carrier extraction, making these arrays promising for low-cost, efficient solar cells. The highly aligned Si nanowire array structure is capable of trapping light, allowing the photons more opportunity to be absorbed and therefore requiring less

silicon [54]. In typical planar silicon, a photon is absorbed in the silicon, which can be a couple of hundred micrometers into the Si to form an electron/hole pair. The minority carriers then have to travel this same distance back towards the p-n junction, increasing the chance of recombination and thus requiring highly pure Si. Radial junction solar cells, are capable of decoupling the direction of light absorption from carrier extraction, so when a photon is absorbed in Si, the minority carriers only have to travel a maximum distance equal to the radius of the wire, reducing the need for highly pure silicon [53, 59]. The ability to separate Si nanowire from a reusable substrate can drastically reduce the quantity and quality of silicon required for a low-cost, efficient solar cell.

A third additional example demonstrating the potential of vertical Si nanowire arrays is the anode of Li-ion batteries. Conventional Li-ion batteries use carbon based materials for the anode material, which has a theoretical storage capacity of 372 mAh/g [62]. Silicon, on the other hand, has a much larger theoretical storage capacity of ~4200 mAh/g, resulting in a more than six times increase in the overall storage capacity [62]. One issue that arises during operation is the large volume expansion of Si, up to 400%, when Li ions are inserted into Si. This results in the pulverization of Si which can damage the contact to the current collection and decrease the overall charge storage capacity over time [62-64]. Vertical silicon nanowires array, due to their small dimensions are capable of withstanding the high strain formed during the lithiation process. This allows Si nanowires to be used as an anode material capable of being used over many charge and discharge cycles without a decrease in performance. The vertical Si nanowire arrays will need to overcome the challenge of removing the Si nanowire

array from the bulk Si substrate in order to be directly connected to a current collector, bypassing any bulk Si that can lead to pulverization.

1.4. Scope and Organization of Thesis

The main body of this thesis contains 5 chapters. The first main chapter (Chapter 2) examines a range of methods that are used to form a wide variety of nanostructured Si. The next chapter measures the thermal conductivity of the nanostructured Si nanowire arrays. The last three body chapters tackle the challenge of transferring large area, high dense Si nanowire arrays to non Si substrates.

- Chapter 2 describes a variety of top-down Si nanostructuring methods that range from porous Si to non-porous Si nanowire arrays and everything in between.
- Chapter 3 develops a fabrication method capable of using an optical method to measure the thermal conductivity of a Si nanowire array film. The Si nanowire fabrication method is varied to control both the internal and external phonon scattering sites with a range of porosity and Si nanowire diameter.
- Chapter 4 develops a method to chemically form a horizontal crack through a SiNW array, effectively weakening the adhesion between the array and bulk substrate. The array can subsequently be transferred from the Si substrate to any material, including flexible, transparent or conducting substrates.
- Chapter 5 utilizes the transfer method in Chapter 4 to fabricate Si nanowire array electronic devices. The properties of the Si nanowires are varied to achieve the electrical performance of both highly porous and marginally-porous Si nanowires.

- Chapter 6 expands on the methods in Chapter 4 and 5 to develop a new more universal method that is capable of transferring any Si nanowire array to arbitrary substrates for device integration regardless of the Si nanowire array fabrication method.

Chapter 2. Experimental Nanostructured Silicon Fabrication Methods

Nanostructuring of silicon (Si) has received increasing substantial interest over the past few decades due to its ability to possess unique material properties that are not possible in bulk form [67, 68]. The fabrication of these Si nanostructures is often separated into two categories; bottom-up and top-down. Since the early 1990's, bottom-up techniques have been the more favorable single crystalline Si nanostructuring method. In particular the vapor-liquid-solid (VLS) growth method has received substantial attention for the synthesis of Si nanowires (SiNWs). VLS SiNWs form in a chemical vapor deposition (CVD) chamber through the absorption of a Si based gas precursor at a liquid catalytic alloy, typical gold (Au), at a temperature higher than the eutectic point (300-400 °C) [69-71]. The liquid catalyst serves as the preferred decomposition site of the Si atoms from the gas precursor until the catalyst becomes supersaturated with Si, at which point Si crystallizes beneath the catalyst, forming SiNWs. While the VLS method is a well-developed SiNW synthesis method, it suffers from a few limitations and drawbacks. First, the CVD setup and growth process is rather expensive and is typically limited to small growth areas due to the chamber size. Second, the SiNW density is relatively low due to the challenge of preventing the close-packed catalyst particles from merging at the growth temperature [72]. Third, achieving a high degree of vertical alignment is often a challenge. Fourth, the SiNWs can be doped through a variety of methods, including with the metal catalyst or the addition of a dopant gas; however, accurately predicting the resulting dopant level is very challenging [68]. Finally, during

the high temperature growth process, the metal catalyst diffuses into the SiNWs forming crystallographic defects and trap sites that reduce the minority carrier lifetimes [68, 73].

Top-down etching methods start with a bulk Si wafer and remove materials rather than add material. These offer the potential to alleviate some of the limitations and drawbacks associated with the bottom-up synthesis of Si nanostructures. For example, since the resulting SiNWs are etched from a bulk wafer, the doping concentration is based on the original wafer and the high temperature growth conditions are eliminated, removing the crystallographic defect sites. Furthermore, precise scalable patterning methods can be used to form highly aligned, dense Si nanostructures over a large area, making the top-down technique a very promising method. This chapter will go over a range of top-down etching methods beginning with the basics of forming porous Si and expanding to highly aligned SiNW fabrication and modification methods.

2.1. Porous Silicon Formation: Etching Chemistry and Theory

Porous Si was discovered by accident in the mid-1950s, while attempting to develop an electrochemical method to polish the surface of Si and germanium (Ge) [74]. Instead of polishing the Si as expected to form a reflective surface, a brittle dark film was found that contained porous holes propagating primarily in the <100> direction through the Si wafer. Although this was recorded in a technical report at Bell Labs, it did not receive substantial interest until the early 1990s when it was determined that porous Si can emit visible light [75, 76]. A plethora of work focused on creating porous Si based

optoelectronics was reported during the mid-1990s until it slowly calmed down due to disappointing electroluminescence efficiency, and poor chemical and structural stability [77]. Since then, the fundamental understanding of porous Si has been improved and is currently being used in a wide range of applications from drug delivery systems, optoelectronics, sacrificial materials, energy storage and harvesting devices [26, 77-81].

2.1.1. Anodization

While Si is thermodynamically unstable in air and water, forming a native oxide layer, in the presence of hydrofluoric acid (HF) the oxide is rapidly removed leaving the surface hydrogen terminated (Si-H) [82]. The Si-H bonds passivate the surface preventing further oxidation in aqueous HF without the presence of strong oxidation agents. A common and controlled method to promote the continued oxidation of Si is through anodizing the Si in an HF solution. A typical anodization cell, shown in Figure 2-1, is composed of a Teflon chamber with a circular opening where a clamped piece of Si wafer is exposed to the solution. A power supply is connected to the cell, supplying a constant current to flow through the Si wafer with a metal back contact, acting as an anode, to a platinum (Pt) counter electrode submerged in the HF electrolyte solution, allowing an electrochemical reaction to form at the interface of the Si and solution (see Appendix A for more details). Although porous Si forms in HF solutions diluted with deionized water, the hydrophobic properties of the hydrogen terminated surface hinder the ability of the solution to infiltrate the pores and therefore induces lateral and in-depth inhomogeneity [79]. Thus, ethanolic solutions are commonly used to increase the wettability on the porous Si surface, allowing the solution to infiltrate the pores [77].

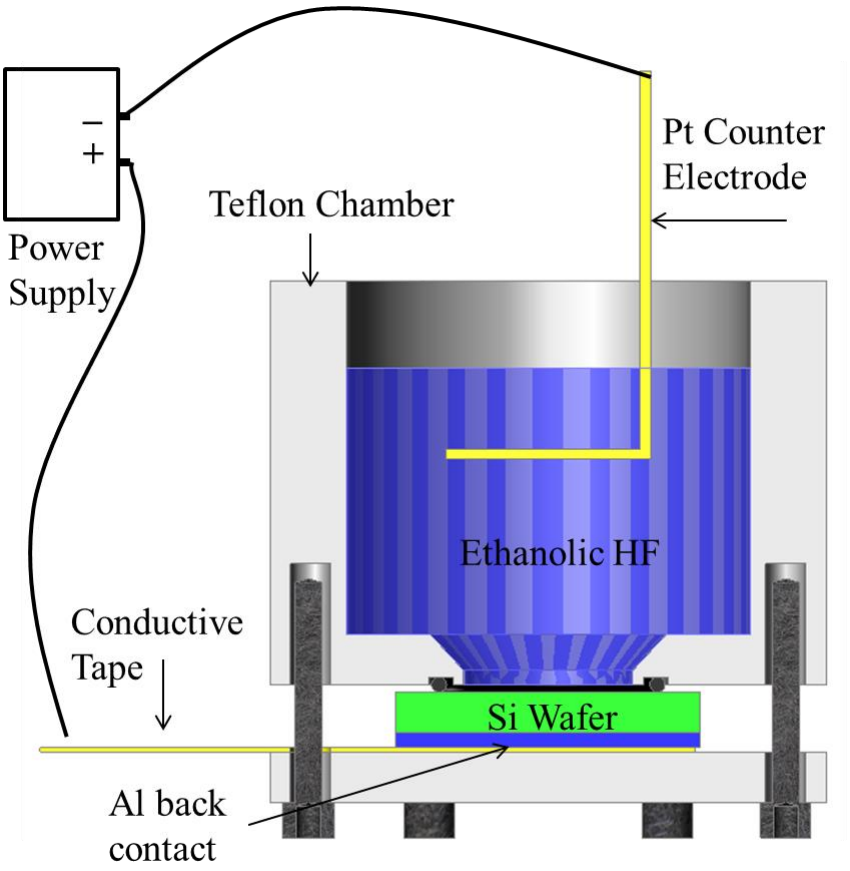
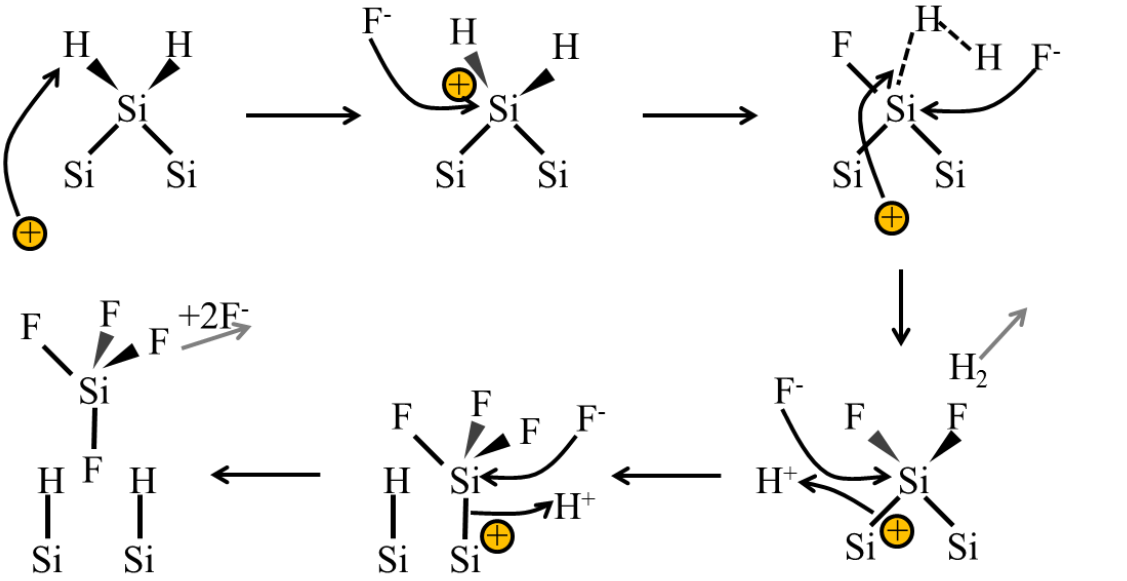


Figure 2-1. Cross-sectional schematic of an anodization cell used to form porous Si.

The dissolution of Si is obtained by supplying either an anodic current or potential; however, supplying a constant current allows for superior control and reproducibility [83]. The power source supplies holes to the Si valence band, oxidizing the Si surface. The holes are driven to the surface by diffusion from the electric field generated within the wafer. At the Si surface, holes break apart the Si-H bonds causing competition between the formation of Si-H, Si-O and Si-F bonds [77]. The Si-F bond has the highest electronegativity, making it the favorable bond with Si-O being the second most likely. The high electronegativity makes the Si-F bond highly polarized, so as soon

a fluoride ion attaches to a Si atom it becomes the preferred atom for the subsequent holes to attach to, leading to the rapid dissolution of the Si atom into water as soluble SiF_6^{2-} as shown in Figure 2-2 [77].



Overall Reaction at Silicon Surface: $Si + 6F^- + 2H^+ + 4h^+ \rightarrow SiF_6^{2-} + H_2$

Figure 2-2. Reaction model for the anodic dissolution of Si in the presence of hydrofluoric acid [77].

The preferred crystal plane direction for the removal of Si in HF is related to the energy associated with cleaving the Si back-bonds [84]. The effected number density of back-bonds increases relative to the crystal plane in the order of (100) < (110) < (111); therefore, the pores typically propagate along the <100> direction [85]. However, the pore morphology, size and overall porosity greatly depend on the wafer, solution, and

applied conditions during the porous Si formation process. Varying the wafer type and doping level will affect the pore formation mechanism, which in turn affects the size and directionality of the pores [86]. For example micropores (pore width ≤ 2 nm) are often formed in low and moderately doped p-type Si with the most uniform porosity. Mesopores (2 nm < pore width ≤ 50 nm) are often formed with highly doped p- and n-type wafers with pores perpendicular to the wafer surface due to the enhanced electric field driving the holes towards the base of the pore. Macropores (pore width > 50 nm) are often formed in low doped n-type wafers with pores forming perpendicular to the surface due to the space charge region depleting the holes around the pore [77, 83]. The pore size and morphology can also be tuned through varying the solution or conditions. In general, increasing the current density, increasing the temperature or decreasing the HF concentration has a similar affect, leading to an increase in the pore size and porosity [77, 78, 84, 86-88].

2.1.2. Electropolishing

As mentioned earlier, the Uhlirs discovered porous Si formed under certain conditions while trying to develop an electrochemical method to polish Si and Ge [74]. If the porous Si conditions are modified in a particular way, electropolishing occurs which is very beneficial for releasing thin porous layers from bulk Si wafers [89]. The key condition required for electropolishing is the rate the current injects holes into the Si surface has to exceed the rate that fluorine ions can be transports to the pore tip [77, 90-93]. Under this condition, the fluorine ions cannot keep up with the rate the holes are injected into Si valence band, which leads to the formation of Si-O bonds as shown in

Figure 2-3a. After a brief amount of time, a continuous oxide layer will spread underneath the entire porous layer which will be followed by the HF attacking the continuous oxide layer, resulting in the liftoff of the original porous film (Figure 2-3b).

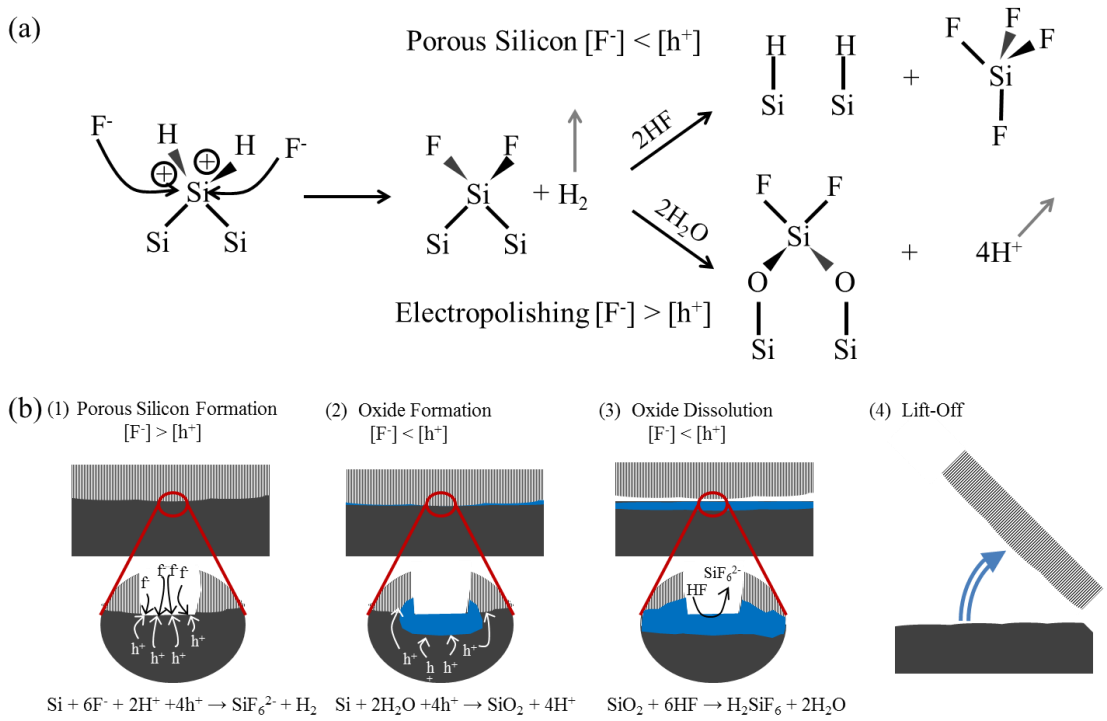


Figure 2-3. (a) Reaction model pathways of the anodic dissolution of Si during porous Si formation and electropolishing. (b) Schematic demonstrating the lift-off of a porous Si film: (1) A porous Si layer is formed, (2) the hole inject rate exceeds the fluorine mass transport rate as an oxide layer starts to form, (3) hydrofluoric acid attacks the now continuous oxide layer, (4) the oxide layer is removed, allowing the free-standing porous Si film to be lifted off from the Si substrate [77].

There are two primary methods to ensure that the rate of hole injection into the valence band exceeds the mass transport rate of fluorine ions to the Si/solution interface

as shown in Figure 2-4. The first method is to substantially increase the current density while keeping the solution constant (blue line). The second method is to reduce the HF solution concentration which in turn reduces the number of available fluorine ions (blue to red line). Both of these or a combination of these methods work; however, it has been reported that a higher surface quality is obtained when the HF concentration is reduced rather than increasing the current density (see appendix A for additional details) [92]. A transition region occurs between the pore formation and electropolishing regions. In this region the number of holes injected into the valence band and fluorine ion concentration are approximately equal so oxygen and fluorine ions compete for control over the Si surface bonds [84]. The resulting surface is porous in nature; however, the pore sizes significantly increase as the potential approaches the electropolishing potential [84, 86, 87]. It is important to note that porous Si is very fragile, so a delicate drying method, such as critical point drying, is often required to preserve the porous Si especially after a lift-off process.

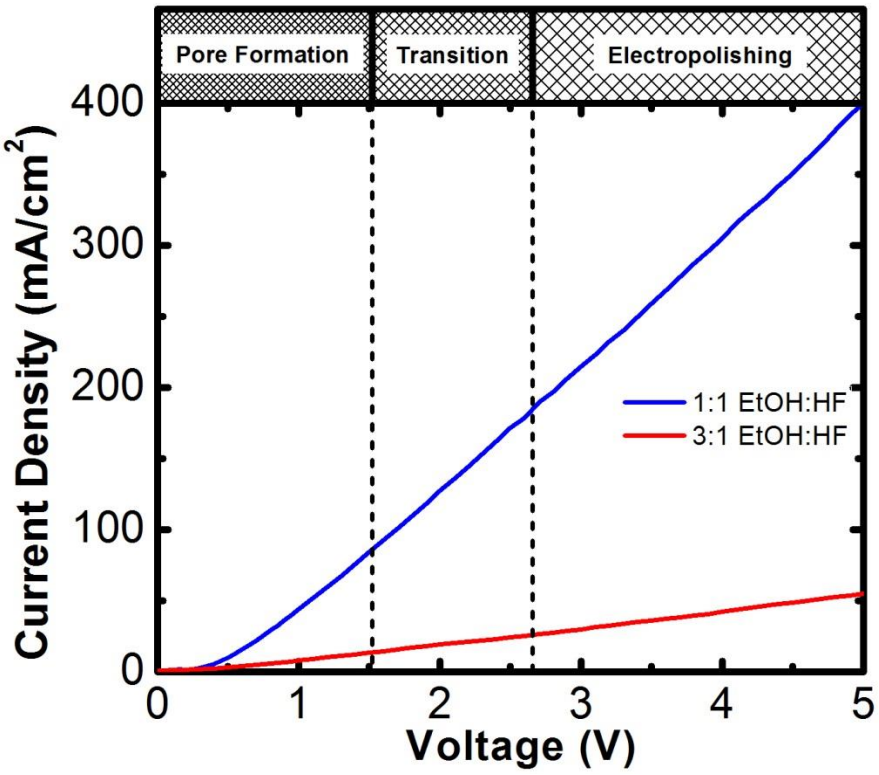


Figure 2-4. Exemplary current density vs. voltage curve for a Si wafer with a p-type boron dopant concentration of 10^{16} cm^{-3} in a 1:1 and a 3:1 ethanol:hydrofluoric acid solution. The Si dissolution goes from porous Si formation to electropolishing with a transition region in the middle as the voltage potential is increased by either increasing the current or decreasing the hydrofluoric acid concentration.

2.1.3. Stain Etching

Stain etching is a less common but easier alternative method to prepare thin porous Si layers. This method produces porous Si films on crystalline Si wafers with a red or brownish color, hence the name "stain etching" [94]. Instead of anodically oxidizing the Si with a constant current or potential, an oxidizing agent is added to the

hydrofluoric acid solution, typically nitric acid (NHO_3). The nitric acid is reduce to nitric oxide (NO) by equation (2-1 below, which serves as the hole injector to oxidize the Si valence band [95].

$$HNO_3 + 3H^+ \rightarrow NO + 2H_2O + 3h^+ \quad (2\text{-}1)$$

It has been reported that the hole injection into the Si is actually catalyzed by NHO_2 rather than NHO_3, so that there is a necessary incubation period required for the concentrated nitric acid to react before the initiation of pore formation [96]. The incubation time can vary from a few seconds to multiple minutes and is also linked to the Si wafer doping type and density [97]. Although stain etching is a simple and easy method, its nonunifomity, unreliable reproducibility, and slow induction period limit its use as a porous Si formation method.

2.2. Top-Down Non-porous Silicon Wire Formation

2.2.1. Deep Reactive Ion Etching

Vertically aligned non-porous Si wires are fabricated using the conventional Deep Reactive Ion Etching (DRIE) process, often referred to as the Bosch Process. Prior to DRIE, a Si wafer was cleaned in a 3:1 (v/v) H_2SO_4:H_2O_2 for 10 minutes, followed by a 10 minute 2% HF dip. The Si wires are patterned with photoresist or a silica sphere masking layer (see Appendix B for more details). The Si wire arrays are formed by DRIE with cycles of 6 second etching with 130 sccm of SF_6 and 5 second passivation with 120 sccm of C_4F_8 in a 600W plasma. The etch time will vary depending on the exposed Si area and the desired Si wire length. The Si wires are fabricated approximately 10-20 μm

in length with diameters ranging from a few microns to approximately 300 nm depending on the patterning method. The Si wire diameter is limited to above 300 nm due to the on/off etch/passivation steps forming scalloped sidewalls along the length of the wire which is too severe in Si wires below 300 nm in diameter.

Si microwires, as shown in Figure 2-5a,b, are patterned using conventional photolithography. The DRIE masking layer consists of a 1 μm thick photoresist layer that is exposed and developed, leaving behind an array with 3 μm diameter circular features at a 7 μm pitch. SiNWs, as shown in Figure 2-5c,d, are patterned using nanosphere lithography with silica spheres, which is described in more detail in the following sections. In this case, it is important to note that the final SiNW diameter is smaller than the original sphere size and slightly tapered along the length of the wire [53]. This is due to the silica spheres being etched despite the 100:1 selectivity of silica to Si which therefore limits the possible SiNW aspect ratio.

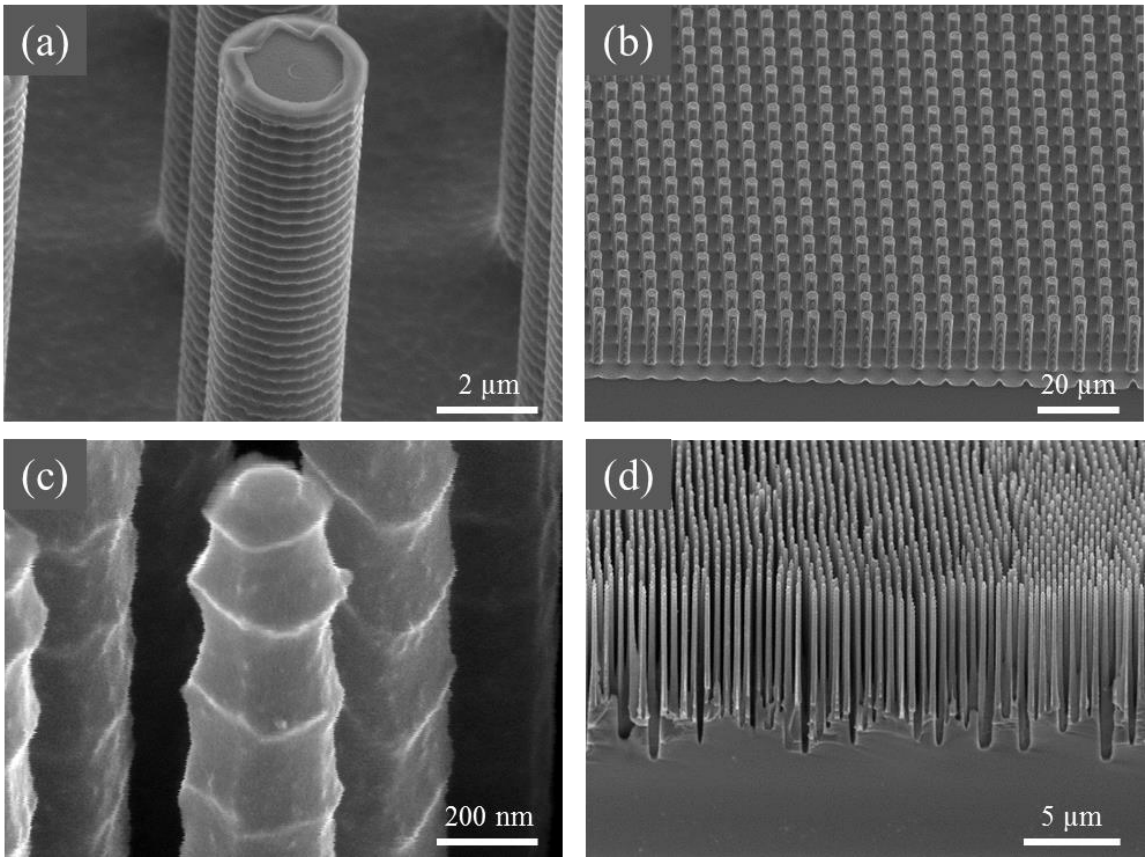


Figure 2-5. SEM images of (a,c) close-up and (b,d) zoomed-out Si (a,b) microwire and (c,d) nanowire arrays formed by the DRIE process**.**

2.2.2. Nanosphere Lithography

Nanosphere lithography is a simple, inexpensive, high throughput, self-assembly method to pattern periodic uniform nanoscale features [98-103]. It typically consists of the formation of a hexagonal close-packed monolayer of nanospheres, although recent research has investigated the benefits of creating double or multiple layers of spheres for the formation of unique patterns or inverse opal structures [98, 100, 103-108]. In order to form a masking layer for individual SiNWs, the close-packed monolayer of spheres needs

to become non-close-packed. While there are large area methods to manipulate the spheres to be non-close-packed such as deformable soft lithography [109-111], the most reliable technique involves dry etching the spheres to reduce their size. Dry etching of the spheres allows precise control over the SiNW diameter and spacing [112].

Nanosphere lithography can be performed using a range of sphere materials and deposition methods. Dip coating, drop casting and spin coating are some of the methods that are considered as quick and cost effective methods to deposit a monolayer of spheres; however, the as-formed monolayers suffered from forming close-packed domains with multiple defective areas of voids or sections of multilayers distributed over the sample area. The Langmuir-Blodgett (LB) method, while more labor intensive, provides an alternative method of forming a high quality monolayer over a large area, which is crucial for fabricating reliable and consistent large-area vertical SiNW array devices. The LB method is achieved by first filling an LB trough (Figure 2-6) with DI water, followed by the slow injection of silica spheres through a syringe. The barrier walls are then slowly compressed while the surface pressure is carefully monitored using a Wilhelmy plate. A quick spike in the surface pressure occurs when barriers are compressed enough to form a close-packed monolayer of spheres on the water surface. A substrate is then dipped into the DI water and slowly pulled out at a constant rate allowing the spheres to be transferred from the water surface to the substrate.

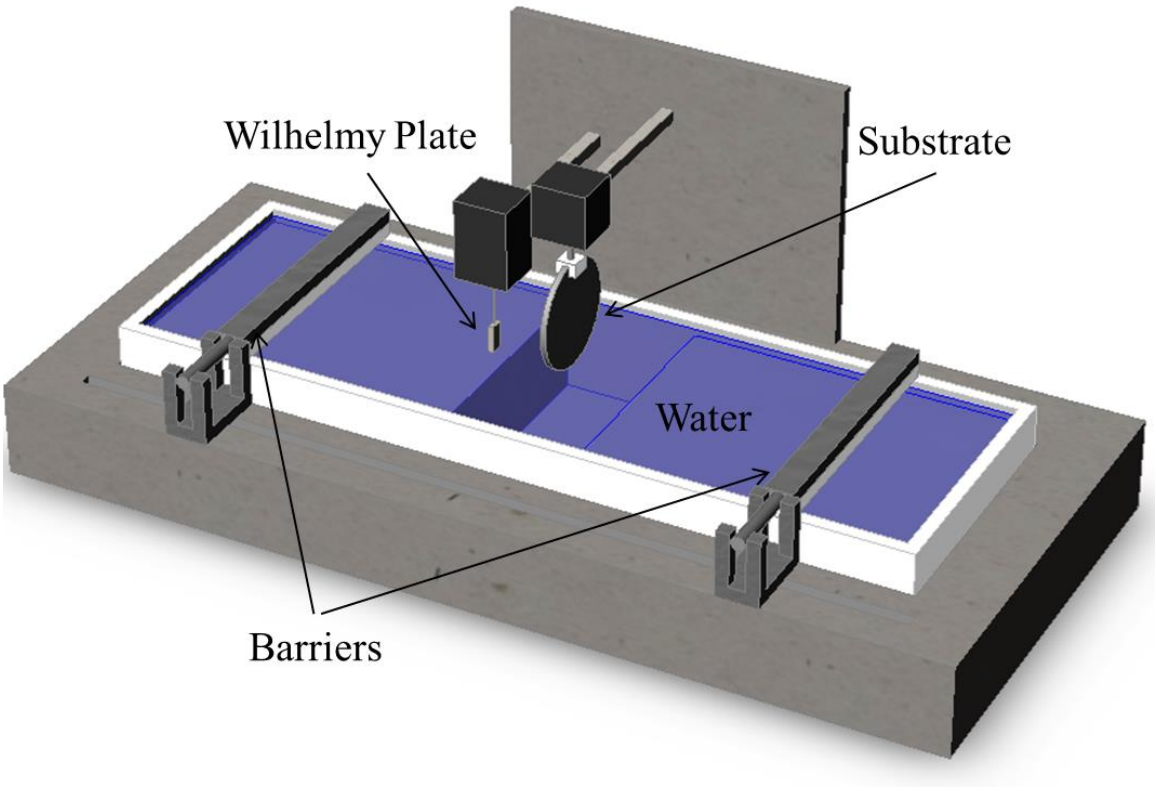


Figure 2-6. Schematic of the Langmuir Blodgett Trough used to deposit a monolayer of silica spheres for nanosphere lithography.

Polystyrene and silica spheres are the most common materials used for nanosphere lithography. Polystyrene spheres have the benefit over silica spheres of isotropic sphere reduction in O_2 plasma which allows greater sphere spacing to diameter ratios, smaller SiNW diameters, and a sphere etching method that does not affect the Si substrate (Figure 2-7) [113]. However, silica spheres offer the advantage of in-lab sphere synthesis and controlled functionalization capable of preparing spheres for use in a LB trough and therefore are the preferred sphere material used in the majority of the work in this thesis [72].

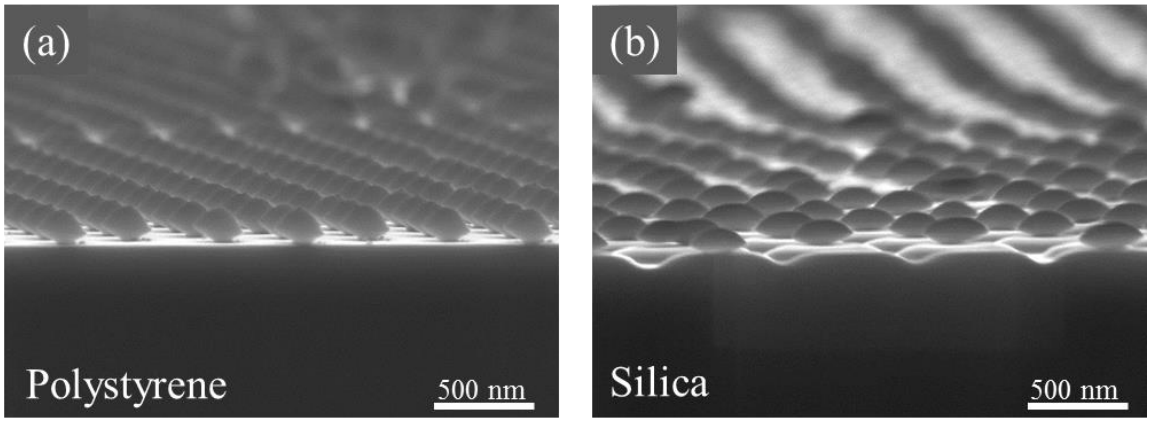


Figure 2-7. SEM images of (a) 490 nm polystyrene spheres etched in O_2 plasma (3 minutes, 20 sccm O_2, 50 mtorr, 100 W) and (b) 650 nm silica spheres etched in a fluorine-based plasma (7 minutes, 6 sccm O_2, 85 sccm CHF_3, 40 mtorr, chamber power of 1600 W)

2.2.3. Silica Sphere Creation and Functionalization

Although silica spheres can be readily purchased, I synthesized our own nanospheres in lab using a modified Stöber synthesis [114]. This sol-gel synthesis is based on the reaction of tetraethoxysilane (TEOS) with water in the presence of an ammonia catalyst to produce silica as show in equation 2-2 [115-117].

$$Si(OC_2H_5)_4 + 2(H_2O) \xrightarrow{NH_3} SiO_2 + 4(C_2H_5OH) \quad (2\text{-}2)$$

The resulting silica particle diameters are a function of a number of factors, including solution pH, temperature, mixing conditions, reaction time, reagent and catalyst concentration [114-116, 118]. The following equation can be used as a rough

approximation to determine the silica sphere size, *d*, in nanometers as a function of the reagent concentration in mol/L [115, 119].

$$d = A[H_2O]^2 exp\left(-B[H_2O]^{1/2}\right) \tag{2-3}$$

where

$$A = [TEOS]^{1/2}(82 - 151[NH_3] + 1200[NH_3]^2 - 366[NH_3]^3)$$

$$B = 1.05 + 0.523[NH_3] - 0.128[NH_3]^2$$

Silica spheres with diameters ranging from roughly 75 nm up to 700 nm can be fabricated using this method while spheres, as large as 1 μm can be purchased from online suppliers (Figure 2-8). A general fabrication recipe used to synthesize 650 nm spheres can be found in appendix C. Silica spheres with diameters less than 150 nm are unable to be cleaned through solvent exchange due to limitations in separating the silica sphere from the solvent during centrifuge cycles.

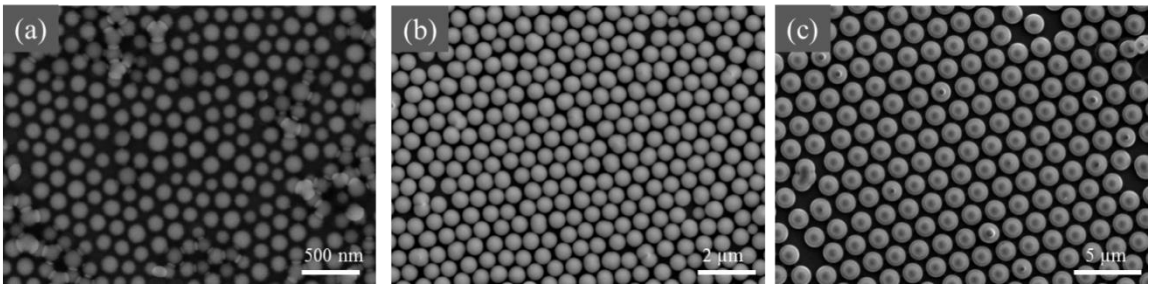


Figure 2-8. SEM images of a monolayer of silica sphere with diameters of (a) 175 nm, (b) 650 nm and (c) 2 μm.

A successful deposition of a monolayer of spheres via Langmuir Blodgett assembly requires the silica spheres to have amphiphilic properties with a hydrophilic and hydrophobic balance. The surface of the silica spheres can be modified from a hydroxyl group to amino group using a surfactant, such as 3-aminopropyltriethoxysilane (APTES). The positively charged amino group prevents aggregation of the silica spheres while also supplying an attractive force to a hydroxyl terminated Si wafer, as shown in Figure 2-9. Detailed steps on the functionalization of silica spheres with APTES can be found in appendix D.

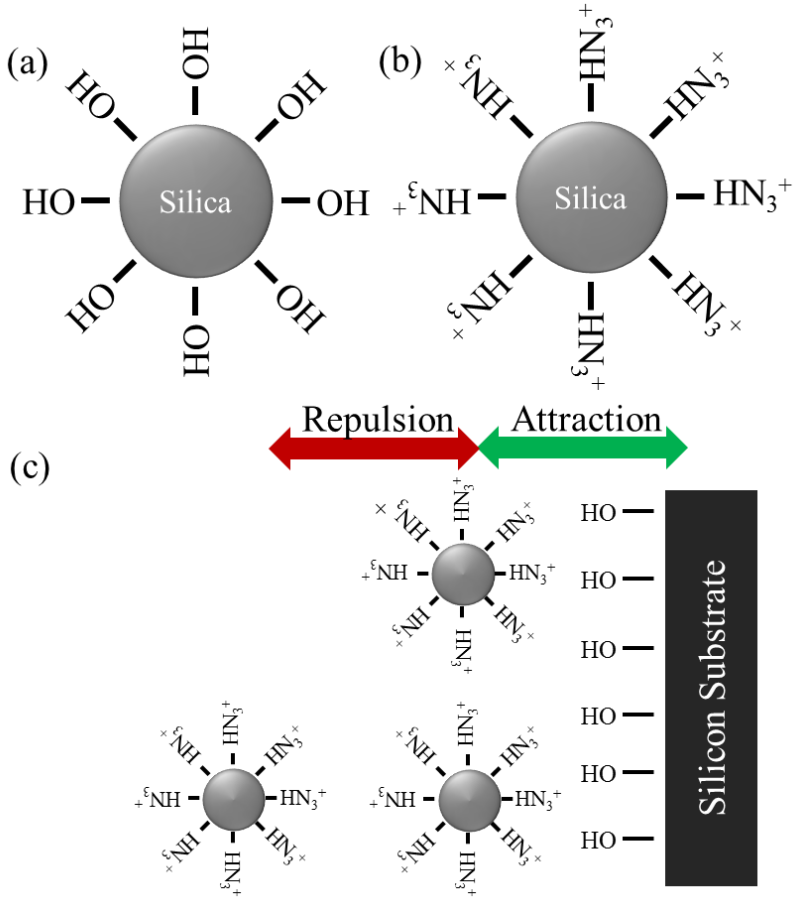


Figure 2-9. Schematic of (a) as formed hydroxyl terminated silica spheres, (b) amino group terminated silica spheres after functionalization in APTES and (c) attraction and

repulsion of silica spheres to a hydroxyl terminated substrate and functionalized silica spheres, respectively.

2.3. Metal-Assisted Chemical Etching

Metal-Assisted Chemical Etching (MACE) is relative new and appealing method to form high aspect ratio SiNW arrays for several reasons. First, the etching mechanism is very similar to that of porous Si but with an etching direction selectivity that surpasses that of DRIE to form SiNWs with high aspect ratios. Second, MACE is a simple, fast and low cost method that can be done in a lab without expensive or time consuming equipment. Third, the etching mechanism forms SiNW arrays regardless of the wafer doping type or concentration. Fourth, the SiNWs can be patterned to vary their shape, size, area and density. There is no clear limitation of the achievable SiNW diameter; however, straight SiNWs can be formed with diameters ranging a low as 5 nm up to 1 um [73]. Fifth, the etching condition and catalyst can be tuned to produce SiNWs that range from almost non-porous to highly porous. Electochemical etching of Si occurs anisotropically along the <100> direction and therefore a (100) substrate is preferred to form vertically aligned SiNW. However, researchers have developed methods to form vertically aligned SiNWs on non-(100) substrates or form slanted, zig-zagged, or spiral shaped NWs or pores [120-122]. The above reasons are why MACE has become a very promising SiNW fabrication method in the past decade in efforts to take a step forward in realizing the practicality of SiNW arrays in functional devices.

The first documented MACE experiment was reported in 1997 when a thin Al film was deposited on a Si wafer prior to stain etching in a solution containing HF, HNO_3 and H_2O [123]. It was determined that the reaction between the Al and HNO_3 injected the holes into the Si at a faster rate without an incubation period [123]. It was not until 2000 when Li and Bohn first demonstrated the catalytic properties of noble metals to produce selective porous Si etching in a solution containing HF, H_2O_2 and ethanol [124]. This opened the door for researchers to investigate the use of patterned noble metal films coated on Si substrates to selectively etch Si in the presence of HF and an oxidizing agent to form controlled nanostructures.

2.3.1. Etching Mechanism Theory

The etching mechanism in MACE is very similar to that of stain etching. However, instead of using HNO_3 as a chemical oxidizer, H_2O_2 is used with the assistance of a noble metal catalyst to oxidize the Si. Although the electrochemical potential of H_2O_2 is much larger than the Si valence band (Figure 2-10a), making it energetically favorable for H_2O_2 to oxidize Si, the etch rate is very low, less than 10 nm per hour [73]. When a noble metal catalyst is used to assist in the oxidation of Si by H_2O_2, the etch rate is significantly enhanced leading to etch rates up to 1 μm per minute. The etching mechanism can be divided into a redox reaction couple occurring at an anode and a cathode (Figure 2-10b). The first reaction takes place at the interface of the cathode metal surface (Ag in this example) and the solution. Here, Ag is oxidized by the H_2O_2 to form Ag^+ ions in the close vicinity of the Ag film. The second reaction occurs at the interface of the anode Si film and metal surface where the Si is oxidized through the

reduction of the Ag^+ ions back onto the Ag. The Si is preferentially oxidized along the <100> due to the (100) plane having two of the four Si bonds symmetrically exposed to the surface compared to only one bond in the other common surface planes, which is typically not strong enough to weaken the other three bonds (Figure 2-10c) [84, 85]. While the exact diffusion process of how the HF accesses the oxidized Si is not known, the most plausible explanation involves the formation of a thin porous layer around the metal during the etch which allows for the exchange of reactants beneath the metal film [125]. The process will allow the metallic layer to continuously drill a hole forming SiNWs with aspect ratios up to or even greater than 1000, due to the anisotropic oxidation.

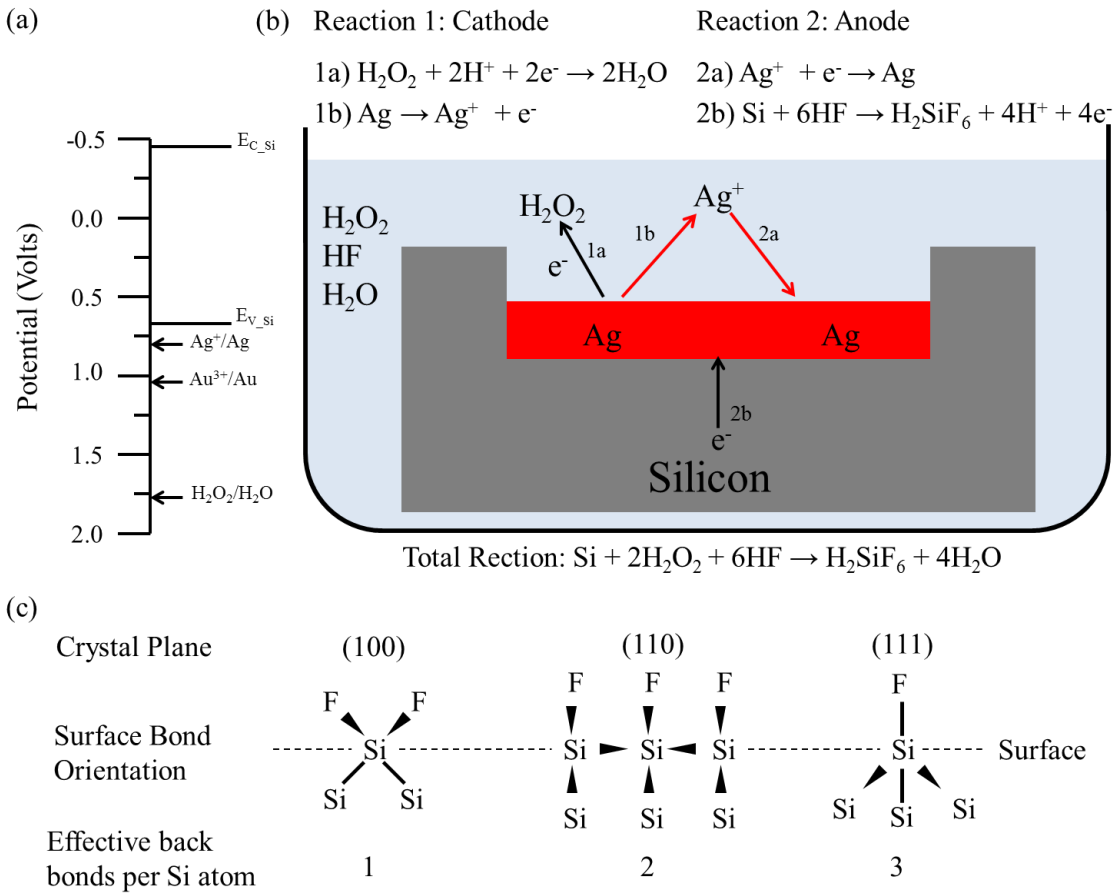


Figure 2-10. (a) Comparison of the electrochemical potential of the Si valence band to H_2O_2 and typical metal catalysts used in MACE. (b) Schematic of the reactions occurring during MACE. (c) Bond orientation for the three common crystal planes in Si. The (100) plane has the most favorable geometry and least number of effective back-bonds per Si surface atom for the dissolution of Si.

2.3.2. Catalyst Patterning Methods

The SiNW diameter, shape, and density are determined by the catalyst geometry which can be controlled by a variety of patterning and deposition conditions. The

simplest and cheapest method to pattern the SiNWs is through the electrodeposition of silver salts ($AgNO_3$) on a Si wafer. This is accomplished by first cleaning a Si substrate in a 3:1 (v/v) H_2SO_4:H_2O_2 for 10 minutes, followed by a 10 minute 2% HF dip. The silver is then deposited by gentlely mixing the substrate in a solution composed with 4.8 M HF and 0.005 M $AgNO_3$ for 45 seconds. The residual silver is thoroughly rinsed off with DI water, leaving the Si substrate coated with a silver film in a pattern based around the nucleation of the Ag particles (Figure 2-11a). The subsequent etching of the SiNW array takes place in a MACE solution composed of 4.8 M HF and 0.3 M H_2O_2. Typical SiNWs formed using this method (Figure 2-11 b,c) have diameters ranging from 20-300 nm with an average around 100 nm across a single sample due to the non-uniform nucleation of the silver particles. In addition, the random nucleation of the silver particles will result in variations of the SiNW profile shape, from independent circular nanowires to interconnected walls.

A variety of template-based patterning methods have been used to improve the control over the SiNW uniformity, size, density and shape. Some of these common patterning methods include nanosphere lithography [98, 100, 112], interference lithography [126], anodic aluminum oxide (AAO) [85, 122] and block-copolymer masking layers [127]. While interference lithography appears to be the most promising for fabricating highly aligned patterns with feature sizes as low as 65 nm, the initial setup is relatively complex [126]. Most of the SiNWs fabricated in this dissertation use MACE where the metal is patterned with nanosphere lithography. Using the methods described earlier in this chapter, silica spheres are deposited on a Si wafer via Langmuir Blodgett

and reduced by reactive ions to the desired SiNW diameter. The Si wafer is then exposed to oxygen plasma, to improve the wafer's wetting properties, immediately before the e-beam evaporation of the metal catalyst. The metallized film typically ranges from 15 to 50 nm. After the deposition, the spheres are easily lifted off from the substrate via sonication leaving a honeycomb shaped metallic pattern on the Si surface (Figure 2-11d). It is important that the thickness of the metallic layer be less than half of the sphere height to prevent bridging the metal from the wafer and to the spheres. Once all the spheres are removed, the wafer is slowly dipped into a 2% HF solution for 2 minutes to remove any oxide layer between the metal and Si prior to immerging the wafer in the MACE etching solution. As shown in Figure 2-11e,f, the SiNWs formed by this method have superior uniformity in the size, alignment and geometry compared to the SiNWs etched with electrodeposited silver salts.

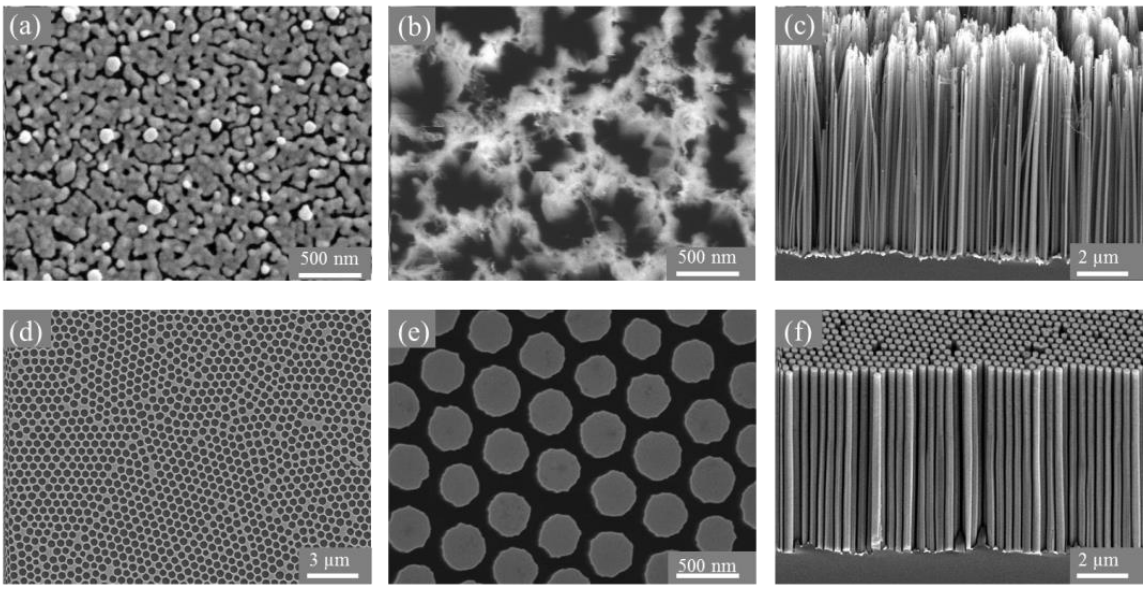


Figure 2-11. SEM images of SiNWs formed with MACE when the silver is patterned (a-c) with silver salts and (d-f) with nanosphere lithography. The SEM images show (a,d)

the patterned catalyst before etching, (b,e) a top view and (c,f) a 45 degree view of the as etched SiNWs.

2.3.3. Control Over The SiNW Morphology and Geometry

The resulting SiNW morphology and geometry closely depend on the metal catalyst, solution and Si used during MACE. Slight variations in any of these parameters can affect SiNW etching conditions. Let's first investigate the effect of the metal catalyst. This includes the metal type, thickness, deposition conditions and coverage area. The common metals used in MACE include Ag, Au, Pt and Pd. While there is no literature comparing the catalytic activity for the H_2O_2 reduction using these different metals, Ag seems to have the best etching performance with Au being the second best; making them the most popular metals [73]. Although, Ag has the best catalytic performance, it undergoes structural dissolution during the etching process, resulting in the thinning of the Ag film and deposition of Ag particles along the SiNW sidewall, increasing surface roughness [85]. Gold on the other hand does not undergo structural dissolution and is therefore more stable as a catalyst. The benefits of the high catalytic activity in Ag and inert structural dissolution properties of Au can be combined in a bilayer structure, eliminating the drawback from Ag's structural dissolution [85]. This is achieved by first depositing the silver layer on the Si wafer followed by a thin Au capping layer. The thickness of the metal is also crucial to the final structure. As mentioned above, the metallic layer can change during the etching process and become thinner so if the metal is only a few nanometers thick it can become non-continuous and result in porous Si formation rather than SiNWs. On the other hand, if the metal is too

thick, it can restrict the reactants from reaching the Si surface and result in a slower, non-uniform etch [128]. While these metals can be deposited by a variety of methods, the etching dependence on the metal thickness favors thermal evaporation, sputtering and e-beam evaporation due to their ability to deposit controlled uniform layers over a large area [73]. The coverage area and feature size are the final considerations that are dependent on the metal. The larger the coverage area, the larger the reaction interface becomes. This will typically slow down the rate or etching since more reactive species are required. However, features with larger cross-sections will actually have a faster etch rates than small pores. This can be contributed to the slower diffusion of reactants in the solution in the smaller pore sizes. Gentle agitation or stirring of the solution can help alleviate this issue and regenerate the solution concentration at the etch front [129].

The second significant parameter is the solution concentration and temperature. The solution, typically composed of HF, H_2O_2 and H_2O, has a large role in the etch rate and the resulting morphology. The solution effect can be broken up into two groups; the H_2O_2 composition and the ratio of the HF to H_2O_2. As mentioned above, the H_2O_2 is the driving force for the oxidation of Si. Therefore the stronger the H_2O_2 concentration, the faster the rate of etching. When the oxidation rate is too fast, the holes can diffuse out from the area beneath the metallized film (process 4 in Figure 2-12a) and excess Ag^+ ion can nucleate directly on the Si surface (process 5 in Figure 2-12a), resulting in an increase in the SiNW surface roughness and porosity (Figure 2-12b-c). Typically a concentration of 0.3 M H_2O_2 is used, resulting in a fast (0.5-1 μm/min) but controlled etch. The other key component of the solution is the ratio of HF to H_2O_2. This parameter

was carefully investigated by Chartier *et al.*[130]. They correlated the different etch structures to the parameter ρ, defined as [HF]/([HF]+[H_2O_2]). When 100% > ρ > 70%, meaning the solution is highly HF concentrated, MACE forms straight pores with diameters equal to the metal pattern (Figure 2-12b). Under these conditions the oxidation of Si by H_2O_2 is the limiting step with sufficient HF to remove the oxidized Si as soon as it is formed, therefore reducing the number of holes and Ag^+ ions that lead to sidewall etching and porous Si formation. If the ratio is reduced to 70% > ρ > 20%, then the HF removal rate cannot keep up with the oxidized Si formation rate. Etching under these conditions will result in an inverted cone shaped structure, where the diameter at the cone tip is similar to the metal particle size and the opening at the surface is much larger due to the sidewall etching (Figure 2-12c). Most of the MACE solutions used in this dissertation used 4.8 M HF along with the 0.3 M H_2O_2 (ρ: ~94%). Standard etching is conducted at room temperature; however, the activation energy for the formation of SiNWs is dependent on temperature. As the temperature is increased, the reaction and therefore etch rate is also increased [131].

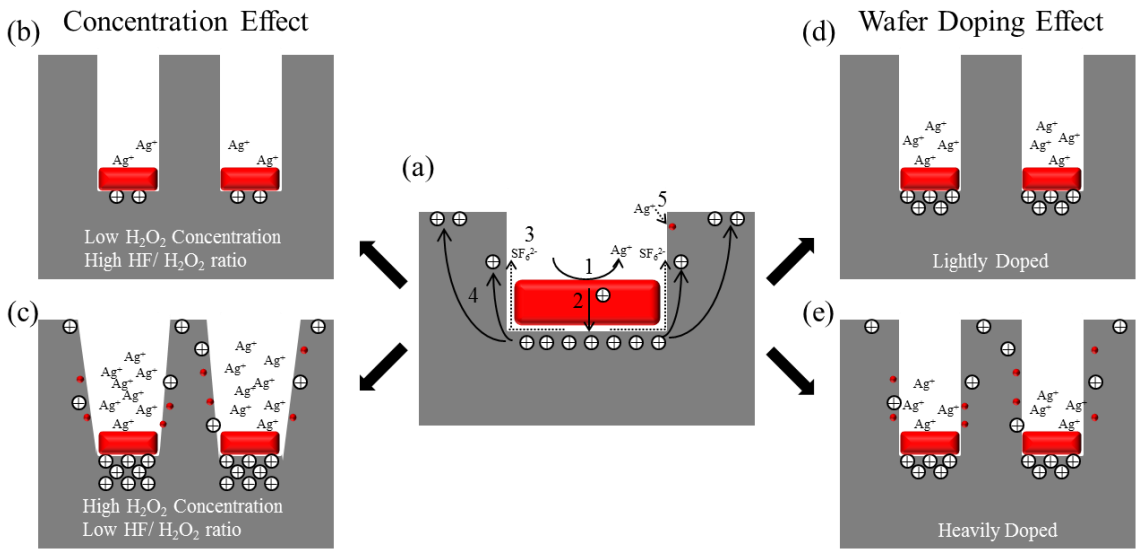


Figure 2-12. Schematic demonstrating the SiNW formation process under a variety of parameters that affect the SiNW porous morphology. (a) Charge carrier transport starting from (1) the oxidation of Ag to form Ag^+ ions, (2) oxidation of Si in the vicinity of the metal catalyst, (3) dissociation of Si by HF removal of the oxidized Si, (4) excess hole migration from the area under the metal catalyst to the SiNW sidewalls and tips, (5) excess Ag^+ ion deposition on the SiNW sidewalls, forming new etching pathways. Illustration of the electronic hole migration and Ag^+ ion concentration in SiNWs formed with (b) low, high (c) high, low H_2O_2 concentration and HF/H_2O_2 ratio, respectively and (d) lightly and (e) heavily doped Si wafers.

The third significant parameter is the intrinsic properties of the wafer, including wafer doping type, concentration and orientation. Although there has been little reported on the effect of doping type on the SiNW etch rate; most believe its effect is minor. However, some researchers have reported slightly faster etch rate in n-type Si compared

to p-type [132]. Doping level on the other hand has a significant effect on the resulting SiNWs. Typically, as the doping level increases, the porosity of the SiNWs also increases due to two factors. First the higher doping level allows the most susceptible holes embedded in the Si valence band to leave the close proximity of the metal and diffuse towards the SiNW sidewalls or tips (process 4 in Figure 2-12a). Second, the defective sites in the higher doping concentrations are preferred nucleation sites for the Ag^+ ions. Thus, the Ag^+ ions are more inclined to diffuse away from the metal film and redeposit along the SiNW sidewalls, leading to increased sidewall etching (process 5 in Figure 2-12a). Therefore lightly doped substrates (Figure 2-12d) tend to form only mildly or non-porous SiNWs while heavily doped substrates (Figure 2-12e) tend to form highly porous SiNWs. The wafer orientation also has a substantial impact of the resulting SiNWs. As mentioned earlier the (100) Si plane has the least number of Si back-bonds, making it the most susceptible for the dissolution of Si. Hence, a (100) wafer is typically used to form vertical SiNW arrays. It was originally reported that the SiNWs etched perpendicular to the substrate form vertical SiNWs in non-(100) substrates [133, 134]. It was later demonstrated that the non-(100) substrates form slanted, aligned SiNWs along the [100] direction when formed by MACE [112, 129, 135, 136]. The contradicting non-(100) etching results led researchers to investigate the parameters and their effect on the resulting etching direction. It was determined that in solutions containing a low concentration of H_2O_2, the SiNWs produced along the (100) direction when the H_2O_2 concentration was high formed perpendicular to the wafer surface regardless of the wafer orientation [137]. It was believed the reason for the vertical formation at higher H_2O_2 concentrations is due to the faster oxidation rate allowing –OH

bonds to form, reducing the anisotropy of the etching direction and proceeding in the vertical direction [137]. I tend to believe the vertical etching at higher H_2O_2 concentrations is due to the increased electric field strength driving the charge carriers in the direction perpendicular to the metal film which can overcome the preferential [100] etching direction. Either way, one can form orientated-modulated zig-zagged SiNWs that change between the [100] and the vertical direction by controlling the oxidation rate by varying the solution composition or producing vertical gradients in the solution composition [120-122]. When a (100) wafer is used this change in solution composition during the etching process will result in vertical but porosity modulated SiNW arrays [122, 138].

2.4. Top-down Silicon Nanowire Diameter Reduction

While top-down SiNW etching methods overcome the controllability and uniformity challenges associated with bottom-up SiNWs; they struggle to form nanoscale feature sizes comparable to bottom-up grown SiNWs. Therefore post processing steps that can further reduce the critical feature size of top-down SiNWs are highly desirable. Figure 2-13 shows two techniques, one dry and one wet, that can be used to reduce the SiNW diameters. The first one (Figure 2-13a) is fairly straightforward and uses an isotropic dry etch to uniformly reduce the SiNWs diameter. This is accomplished in a reaction ion etcher with 10 sccm of O_2 and 100 sccm CF_4 at 300 mT with 200W, resulting in an estimated etch rate of ~25 nm/min. An example is shown below where an as-formed ~300 nm MACE SiNW (Figure 2-13b) is etched for 4 minutes and reduced to a ~100 nm diameter (Figure 2-13c). The second SiNW reduction method, has the

benefits of both reducing the SiNW diameter while also smoothing the surface, mimizing scalloping, surface roughness and surface defects from the etching process [139-142]. This is achieved though the oxidation of the Si surface, which converts the Si on the surface to SiO_2 and can be subsequently removed in HF. While the Si surface can be oxidized by vapors [139] or liquids [141] at room temperature, a thermally grown oxide produces the best oxide layer [140, 142]. During thermal oxidation, for every 1 μm of oxide formed, 0.44 μm of Si is consumed [143]. The thermal oxidation is carried out at 900 °C for 28 min, which is the maximum growth time before the oxide layers from neighboring SiNWs overlapped, followed by the removal in 10% HF for 10 minutes (Figure 2-13d). An example is shown below where the as-formed 300 nm SiNWs (Figure 2-13e) are reduced to roughly 175 nm after the oxidation and removal step (Figure 2-13f). This process can be repeated to further reduce the SiNW diameter and improve the surface roughness.

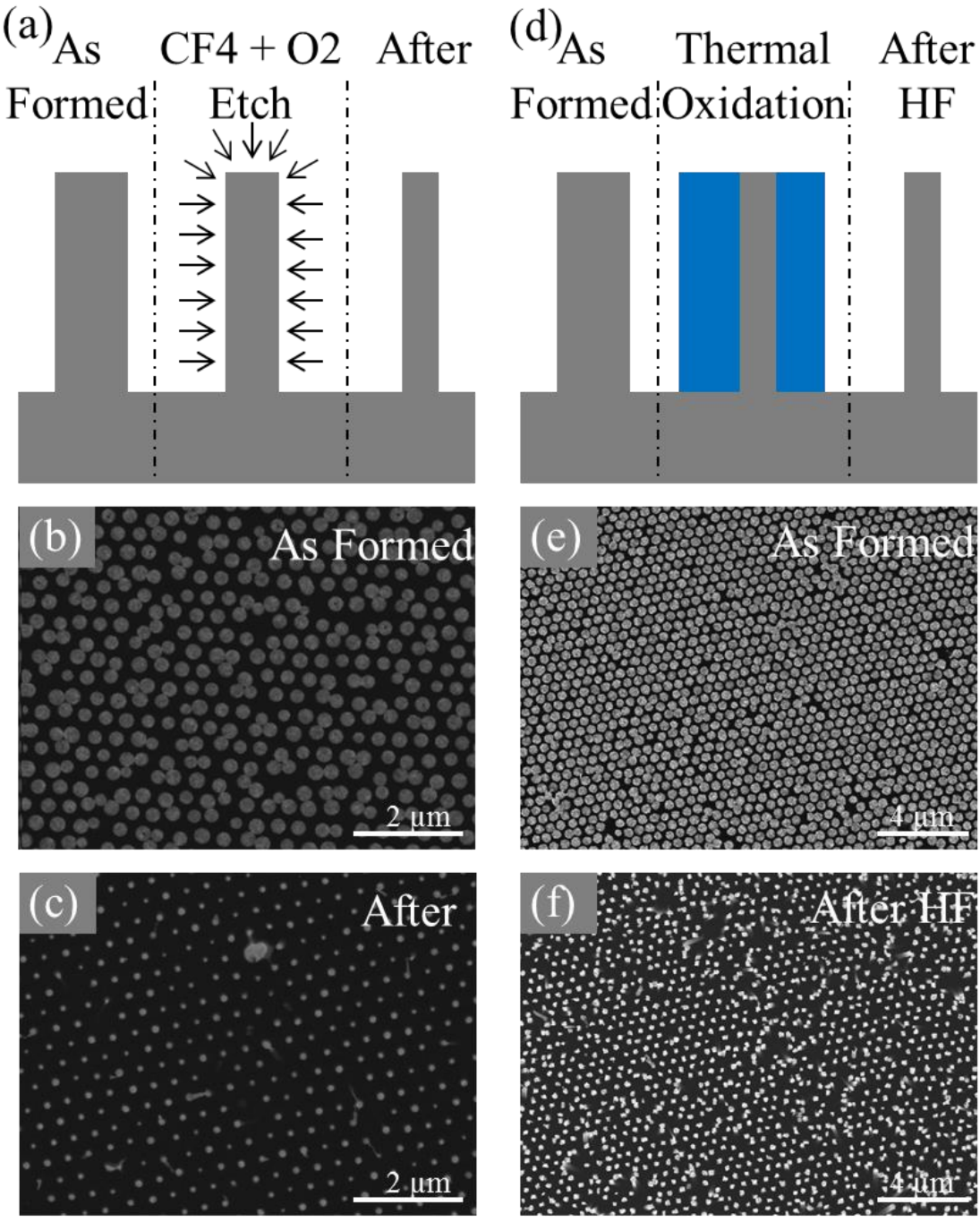


Figure 2-13. Top-down SiNW diameter reduction methods. (a) Schematic of process in which SiNWs are reduced by isotropic reactive ion etching in a CF_4 + O_2 gas. Top view SEM images show the SiNW diameters (b) before and (c) after the dry etching step. (d) Schematic of the process in which the SiNWs are reduced by thermal oxidation and

subsequent removal of the grown oxide layer in HF. Top view SEM images show the SiNW diameter (e) before and (f) after the oxide growth and removal process.

2.5. Section Conclusion

A range of top-down Si nanostucturing methods are described to pattern, etch and modify bulk Si into desired nanostructures with characteristic dimensions ranging from a few nanometer to a few microns. At one end of the spectrum, porous Si can be formed with extremely high surface area to volume ratios by either standard anodization or stain etching which is useful for a variety of drug delivery systems, optoelectronics, sacrificial materials, energy storage and harvesting devices. Moving to the other end of the spectrum, non-porous Si nanowires and microwires that share properties of both bulk and nanostructured Si are formed using DRIE with nanosphere lithography and photolithography, respectively. Bridging the gap between the two above methods is MACE, which has the advantages of being able to form SiNWs where the porosity can be tuned but also provide a cheap, fast, scalable method to form SiNW arrays. Although it is a challenge to form SiNWs with similar characteristic dimensions as bottom up methods, techniques are being developed to post-modify the SiNWs, bringing their diameters closer to that of bottom-up synthesis. As technology moves towards the future, I feel top-down Si nanostructures will have a large role as fundamental building blocks in a large range of future applications.

Chapter 3. Thermal Conductivity Trends in SiNW Arrays

3.1. Background

Silicon with a high density of nanoscale features such as interfaces, porosity, and impurities can have thermal conductivities (κ) up to three orders of magnitude lower than that of bulk Si through enhanced phonon scattering [13, 19, 22, 24-28, 36-38, 40-42, 144-146]. For example, the thermal conductivity of nanoporous bulk Si generally decreases with increasing porosity and decreasing pore size [22, 24-28, 144-146] and, with high porosity, approaches the amorphous limit (0.2 to 0.5 W/m/K) [25, 144, 145]. Similarly, SiNWs with diameters significantly smaller than the bulk phonon mean free path ($\Lambda \approx$ 300 nm at 300 K) were reported to have thermal conductivity values as low as 0.76 W/m/K due to strong phonon scattering at the SiNW boundary [36, 37]. Introducing surface roughness to the SiNWs leads to additional phonon scattering at length scales even smaller than the NW diameter [19, 38, 40-42]. However, there have been few investigations on the combined effects of external dimensions and internal porosity on the thermal conductivity values of SiNWs. In this chapter, we report the effects of internal porosity on the thermal conductivity of SiNWs of two different diameters that allow the phonon propagation to span the range from ballistic to diffusive thermal transport ($d_{avg} \approx$ 350 and 130 nm) by measuring the thermal conductivity of vertically aligned SiNW arrays using nanosecond transient thermoreflectance (TTR). As opposed to measurements of individual SiNWs, measurements of arrays of SiNWs offer the advantage of averaging

out the inherent thermal conductivity variations that are caused by differences in SiNW diameter, surface roughness, and defects within the arrays.

3.2. Fabrication Methodology

The vertically aligned SiNW arrays are fabricated using a four-step preparation process illustrated in Figure 3-1. Two sets of vertically aligned SiNW arrays with different diameters are fabricated (Figure 3-1a,e) using top-down etching techniques to achieve a range of porosities (Table 1, additional details can be found in Appendix E). For the first set, the diameter (d_{avg} ≈ 300 to 350 nm) and density of the SiNWs are controlled by nanosphere lithography [147]. Specifically, a monolayer of SiO_2 spheres is deposited using the Langmuir-Blodgett method onto Si wafers (p-type with boron dopant atoms, (100)) and used as a mask for the subsequent etching steps. The internal porosity of the SiNWs is varied from non-porous to highly porous by changing the etching methods and conditions [148-150]. Non-porous SiNWs are formed by DRIE, and the resulting SiNWs have slightly smaller diameters (d_{avg} ≈ 300 nm) than the spheres used as the etch mask [53]. Porous SiNW arrays are fabricated by MACE in a solution of 4.8 M HF and 0.3 M H_2O_2, and the porosity is controlled by varying the metal catalyst and wafer doping concentrations [85, 148-152]. For low-porosity nanowires, the catalyst layer consists of a 15-nm Ag film covered by 5-nm Au, while for the moderate to highly porous nanowires, a 50-nm Ag film is used as the catalyst and the initial wafer doping concentration is varied. The second set of SiNWs, with generally smaller diameters, is fabricated using a two-step MACE process with silver salts [132, 138, 148, 149, 151]. First, the Ag film is deposited using a solution of 0.005 M $AgNO_3$ and 4.8 M HF for 1

min. Then the SiNWs are formed by etching in a solution of 4.8 M HF with various concentrations of H_2O_2 (0.15, 0.30, 0.60, and 1.20 M) to adjust the SiNW porosity [132, 138, 148, 149, 151]. The resulting SiNWs have an average diameter of 130 nm, but there is significant diameter variation within the SiNW array ($d \approx$ 20 to 300 nm). For all the samples, the SiNW length is approximately 10 μm.

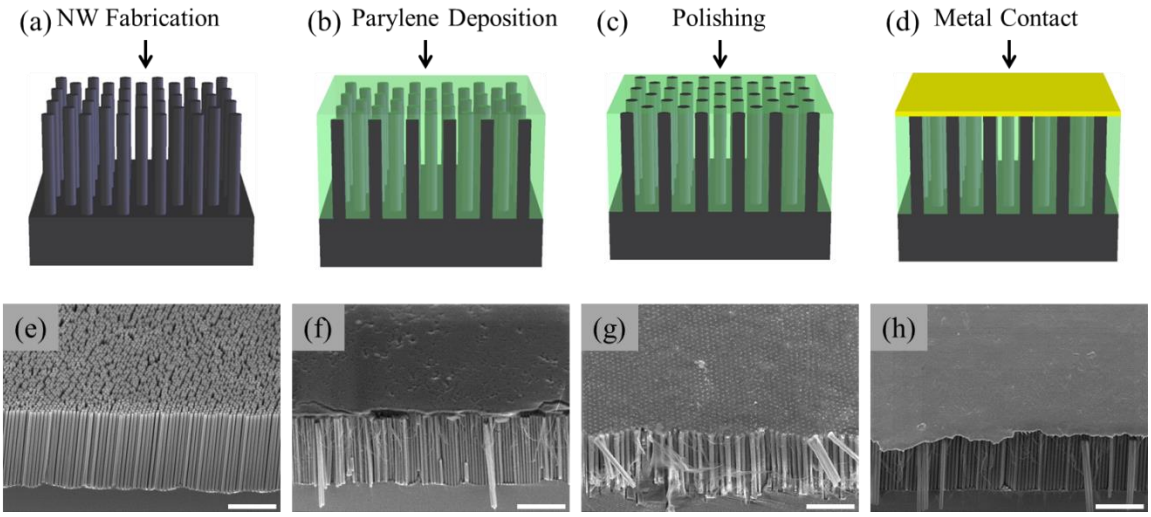


Figure 3-1. Fabrication of the vertically aligned SiNW arrays for the nanosecond thermoreflectance measurements. (a,e) SiNW arrays are formed using the top-down etching. (b,f) Parylene is conformally deposited in between NWs and acts as a mechanical scaffold for the top metal transducer layer. (c,g) The SiNW tips are exposed by chemical mechanical polishing to ensure good thermal contact between the SiNWs and the metal film, and (d,h) a metal film is deposited over the SiNW array. The scale bars on the SEM images are 5 μm.

	Diameter Control	Porosity Control
Set 1:	*Nanosphere Lithography*	*Etching Method and Doping Concentration*
	d_{avg} ~ 300 to 350 nm VF_{DRIE} = 21-23% VF_{MACE} = 45-60%	Non-Porous: DRIE Low Porosity: Ag/Au MACE Moderate Porosity: Ag MACE, Lightly Doped High Porosity: Ag MACE, Heavily Doped
Set 2:	*Silver Salts*	*MACE Etchant Solution*
	d_{avg} ~ 130 nm VF = 26-35%	Low Porosity: 0.15 M H_2O_2 High Porosity: 1.2 M H_2O_2

Table 1. Summary of SiNW arrays with varied diameters and porosities

Following the formation of the SiNW arrays, the gaps between SiNWs are completely filled with parylene N (poly-para-xylylene; Figure 3-1b,f), which has a thermal conductivity significantly lower than the SiNWs (K_{parylene} = 0.125 W/m/K) and a high melting temperature ($T_{\text{m}} \approx 410$ °C). The parylene filling quality is inspected by examining multiple freshly cut cross sections under a scanning electron microscope (SEM), and no parylene voids are observed. The SiNW tips are subsequently exposed via chemical-mechanical polishing to remove the parylene covering the SiNWs (Figure 3-1c,g) that facilitates the SiNWs to form a good thermal contact with the top metal film. Finally, a 15-nm Cr layer (for adhesion) and a 500-nm Cu layer are deposited by electron beam evaporation on top of the SiNW tips to form a flat, reflective transducer layer for the thermoreflectance measurements (Figure 3-1d,h).

3.3. Nanosecond Transient Thermoreflectance (TTR)

The setup and contents of this measurement were carried out by Dr. Amy Marconnet and Dr. Matthew Panzer from Prof. Ken Goodson's Lab.

The thermal conductivity of the vertical SiNW arrays is measured at room temperature by nanosecond TTR (Figure 3-2); the details of which can be found in Panzer et al. [153]. Briefly, the metal transducer layer that is deposited on the parylene-filled SiNW array is heated by a 3-mm diameter, 532-nm wavelength, 6-ns pulse from a Nd:YAG laser at a frequency of 10 Hz (Figure 3-2a). The reflected intensity of the probe laser ($d \approx 20$ μm, 10 mW, 658 nm, continuous wave) is directly correlated to the temperature of the metal layer that is affected by the thermal conductivity of the SiNW/parylene composite through the following relation:

$$\frac{\Delta R}{R_0} = C_{th}\Delta T \qquad 3\text{-}1$$

where R_0 is the reference reflectivity detected by the photodiode, C_{tr} is the thermoreflectance coefficient and ΔT is the normalized metal temperature [153].

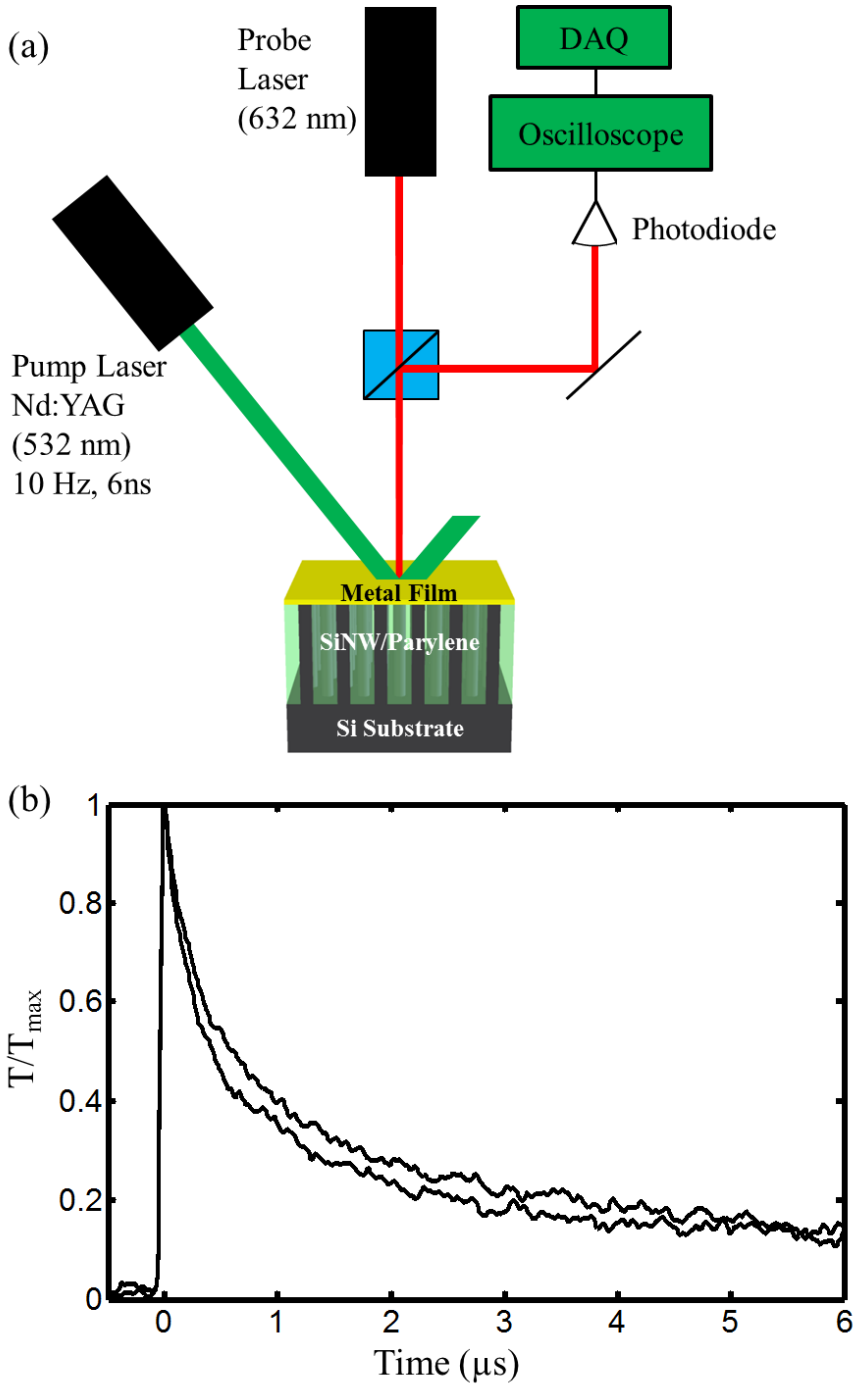


Figure 3-2. Representative illustration of nanosecond transient thermoreflectance. (a) A pump laser causes temporal heating on the surface of a transducer layer with a 6 nm pulse at 10 Hz while a photodiode detects a change in reflectance from a continuous probe

laser. (b) The normalized change in reflectance is converted to a normalized temperature decay and plotted against time, and fitted to a 1-D solution to the heat diffusion equation.

The thermal conductivity of the SiNW/parylene composite and its interfacail thermal resistance at the top metal layer are extracted using a two-parameter fit of the measured temperature decay trace (normalized by the maximum temperature) (Figure 3-2b) to the solution of a one-dimensional heat diffusion equation for a multilayer stack with surface heating. The volumetric heat capacity of the film ($C_{\mathrm{v,composite}}$) is assumed to be the volumetric average of the heat capacity of parylene ($C_{\mathrm{v,parylene}}$) and bulk Si ($C_{\mathrm{v,Si}}$): $C_{\mathrm{v,composite}} = VF \cdot C_{\mathrm{v,Si}} + (1 - VF) \cdot C_{\mathrm{v,parylene}}$, where *VF* is the volume fraction of SiNWs within the composite. The *VF* of SiNWs within each array is measured directly from top-view SEM images of the film by setting a brightness threshold to define the edge of SiNWs (Appendix G). The average thermal conductivity of an individual SiNW within the array is calculated from the extracted film thermal conductivity ($k_{\mathrm{composite}}$) using an effective medium model: $\kappa_{\mathrm{SiNW}} = \left[\kappa_{\mathrm{composite}} - (1 - VF)\kappa_{\mathrm{parylene}}\right]/VF$, where k_{SiNW} and k_{parylene} are the thermal conductivities of the SiNWs and parylene, respectively. In this model, SiNW arrays are treated as thermal resistors in parallel with the parylene matrix. The uncertainty of the extracted k_{SiNW} is calculated through an error propagation analysis given by the following equation:

$$\Delta k_{SiNW} = \sqrt{\left(\frac{\partial k_{SiNW}}{\partial k_{film}}\Delta k_{film}\right)^2 + \left(\frac{\partial k_{SiNW}}{\partial VF}\Delta VF\right)^2 + \left(\frac{\partial k_{SiNW}}{\partial k_{parylene}}\Delta k_{parylene}\right)^2} \qquad 3\text{-}2$$

where $\Delta k_{parylene}$ is the thermal conductivity variation from the literature. Δk_{film} and ΔVF are the measured spot-spot variation in the same type of samples. More details on the measured values, calculated values and error analysis can be found in Appendix F.

3.4. Results

3.4.1. Large Diameter SiNW Trends ($d > \lambda_{bulk\_Si}$)

The thermal conductivity for the SiNWs with large diameters ($d_{avg} \approx 300$ to 350 nm) demonstrates a clear decrease with increasing porosity (Figure 3-3). The thermal conductivity of non-porous SiNWs, though with rough surfaces, is 142 ± 13 W/m/K, which is very close to that of bulk Si ($\kappa \approx 150$ W/m/K). This suggests that for large-diameter SiNWs, surface roughness at this depth and periodicity does not cause effective phonon-external boundary scattering and therefore has little effect on the thermal conductivity. On the other hand, the internal porosity of SiNWs significantly reduces the thermal conductivity from 142 W/m/K for the non-porous SiNWs to 98 W/m/K (Au/Ag-MACE) and 51 W/m/K (Ag-MACE) for the increasingly porous SiNWs.

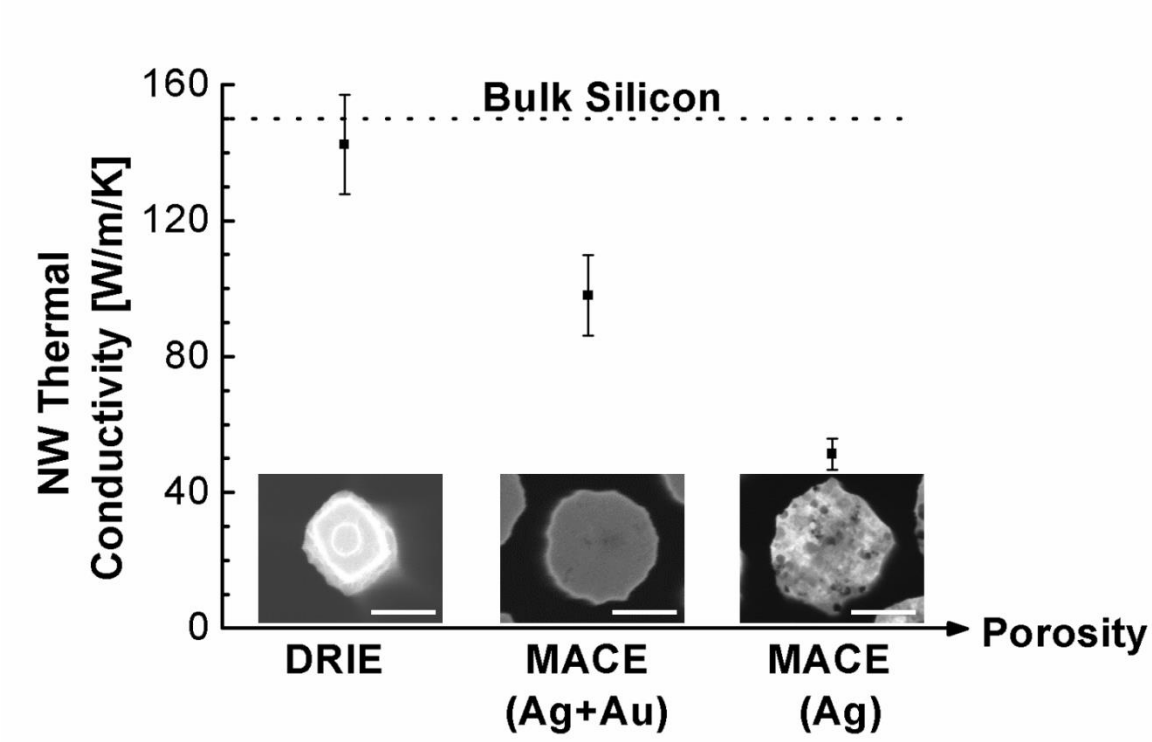


Figure 3-3. Thermal conductivity of large-diameter SiNWs (approximately 350 nm; 10^{14} cm^{-3} p-type doping). The thermal conductivity with three levels of porosity, corresponding to different etching conditions, is shown. The thermal conductivity decreases significantly with increasing porosity. The inset images show the top view of the SiNWs, and the scale bars are 200nm.

The thermal conductivity of large-diameter SiNW arrays ($d_{avg} \approx 350$ nm) with three different p-type boron dopant atom concentrations (10^{14}, 10^{16}, and 10^{19} cm^{-3}) is further investigated for both non-porous and porous NWs (Figure 3-4). The thermal conductivity of non-porous SiNWs decreases slightly with increasing doping concentration due to the increased phonon-impurity scattering, similar to bulk Si [154, 155]. Conversely, the thermal conductivity of porous SiNWs drops to about 1 W/m/K

when the doping concentration is increased from 10^{16} to 10^{19} cm^{-3}. It should be noted that the main reason for the dramatic drop in conductivity with doping concentration is that higher doping concentrations leads to increased porosity in SiNWs fabricated with MACE (Figure 3-4b,c,d). The dopant atom sites act as preferred locations for pore formation [132, 138, 148, 151]. In comparison to the internal NW porosity, the phonon-impurity scattering at higher doping concentration has a much smaller impact on the thermal conductivity [19, 25].

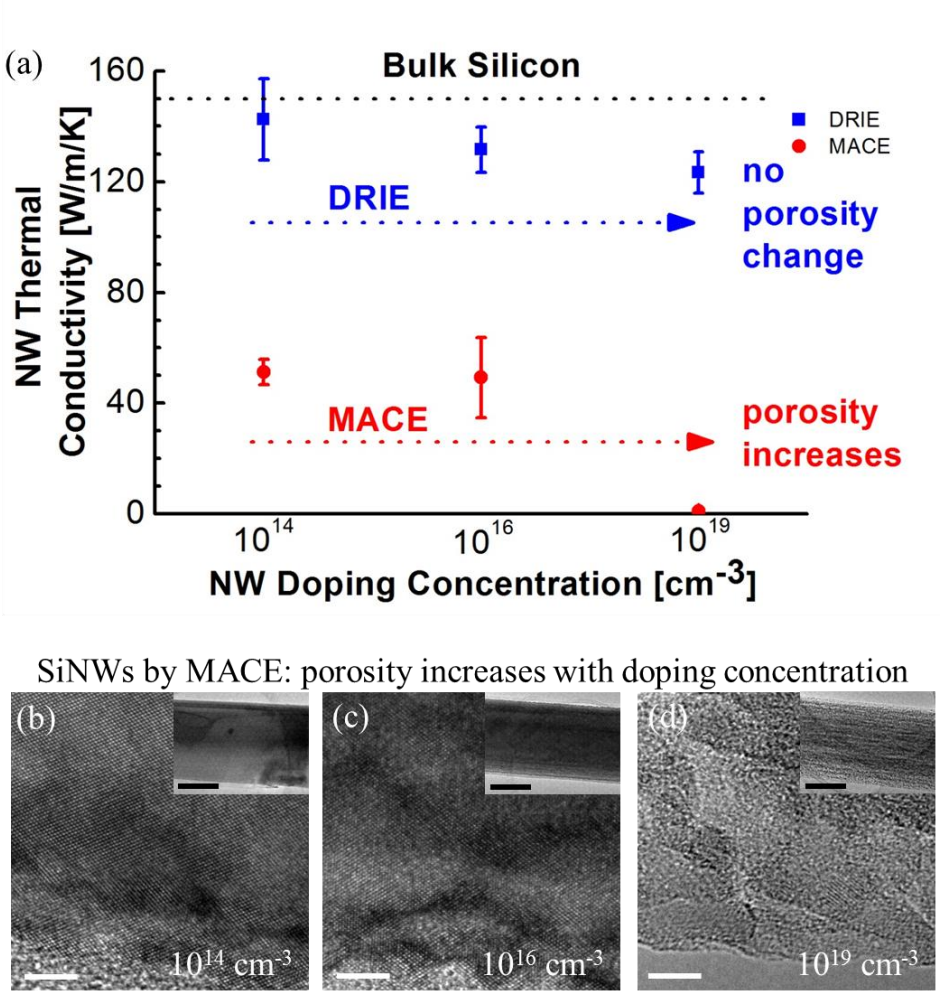


Figure 3-4. Thermal conductivity of large-diameter non-porous and porous SiNW arrays. (a) Thermal conductivity of non-porous and porous SiNW arrays of large diameters as a

function of doping concentrations. TEM images show the relative porosity for Ag-MACE SiNW arrays fabricated with doping concentrations of (b) $10^{14,}$ (c) 10^{16}, and (d) 10^{19} cm^{-3}. The scale bars on the TEM and inset TEM images are 5 and 200 nm, respectively. The uncertainty bar for the MACE nanowires with a doping concentration of 10^{19} cm^{-3} is on the order of the data point marker size (see Appendix F for more details).

3.4.2. Small Diameter SiNW Trends ($d < \lambda_{bulk\_Si}$)

The thermal conductivities of SiNWs with small diameters ($d_{avg} \approx 130$ nm) also decrease with increasing porosity (Figure 3-5), similar to the large-diameter SiNWs. However, the thermal conductivity of these SiNWs is much smaller than that of large-diameter SiNWs of similar porosities (i.e., the same etchant solution, 0.3 M H_2O_2). Specifically, the thermal conductivity is reduced from 51 W/m/K for the large-diameter ($d_{avg} \approx 350$ nm) SiNWs to 28 W/m/K for the smaller-diameter SiNWs ($d_{avg} \approx 130$ nm). This highlights the significant impact of phonon-external boundary scattering on the thermal conductivity at length scales that are smaller than the phonon mean free path. The additional reduction in thermal conductivity (to 17 W/m/K) with increasing H_2O_2 concentration for the smaller-diameter SiNWs indicates that the increasing internal porosity also has a significant impact on the thermal conductivity.

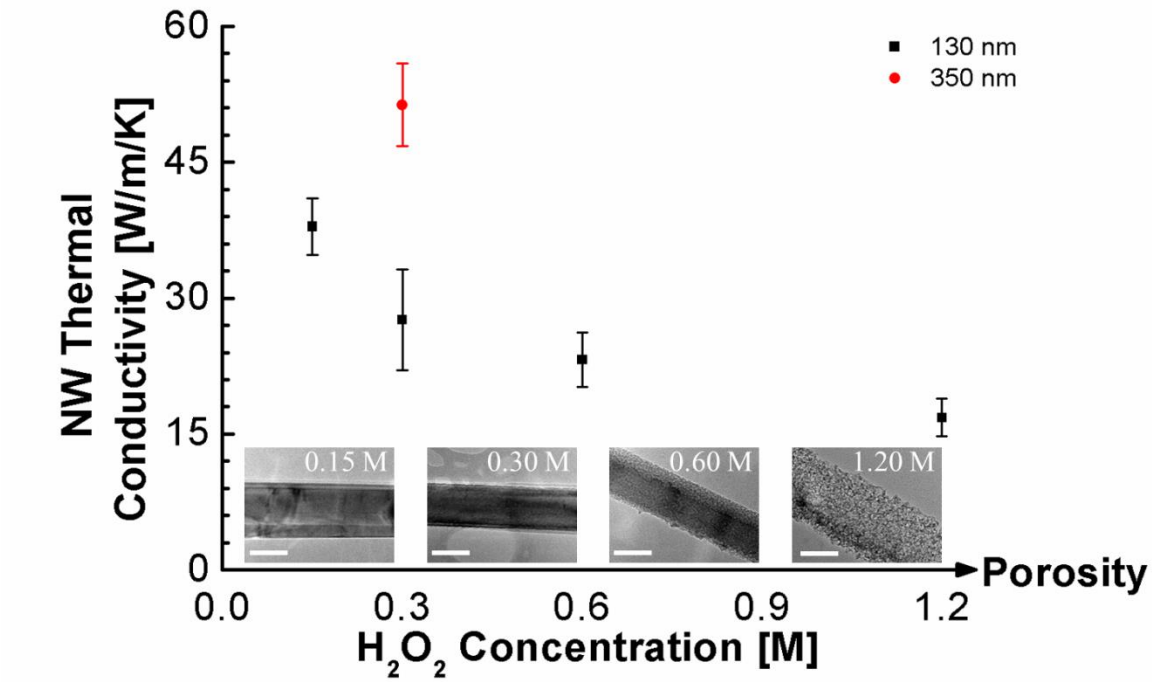


Figure 3-5. Thermal conductivity of small-diameter (approximately 130 nm) SiNWs (10^{14} cm^{-3}) as a function of porosity. For comparison, the thermal conductivity of the large-diameter SiNW etched at the same condition is shown as the red circle. Increasing nanowire porosity is realized by increasing the H_2O_2 concentration during MACE, as evidenced by the inset TEM images. The scale bars on all the TEM images are 100 nm.

3.4.3. Estimated Electrical Performance

While many of the SiNW arrays fabricated in this chapter show a reduced thermal conductivity, the key to improve zT is to achieve a reduction in κ without substantially reducing $\alpha^2\sigma$. As shown above, the addition of porosity to SiNWs can substantially help reduce κ, but if the porosity becomes too high it will also start to interfere with the electrical conductivity. A measurement capable of obtaining both the thermal and

electrical data at the same time would be ideal; however, due to the following fabrication challenges, the measurement was not achieved: 1) fabricating ohmic electrical contacts on polymer embedded SiNW arrays (significantly more challenging than forming measurable thermal contacts) and 2) backing out the SiNW array electrical conductivity from that of the substrate. Initial attempts to further expose the SiNW tips for electrical contact after chemical mechanical polishing were performed via dry etching. While the SiNW tips appeared to be exposed, the surface was no longer flat which prevented the metal transducer layer from having the reflective surface required for the TTR measurement.

The effect on the electrical conductivity can be roughly approximated if the porosity within the SiNWs can be measured. Porous Si formed by electrochemical etching can range in pore size, shape, anisotropy, uniformity and density which prevent an accurate and detailed correlation between porosity and the electrical conductivity. Only a rough approximation to determine if the electrical properties are slightly affected or severely deteriorated can be concluded from the porosity. In porous Si, the electrical conductivity has two main contributions: 1) conductivity from the crystalline matrix and 2) conductivity from hopping between Si crystallites [32]. As the Si becomes more porous, the main contribution of the conductivity transitions from the former to the latter. All of the Si crystalline clusters become isolated once the Si porosity reaches around 57%, known as the percolation threshold (χ_c) [32]. Unfortunately for thermoelectric materials, the electrical conductivity from hopping between crystallites is roughly five orders of magnitude lower than crystalline Si [30, 31, 79, 156, 157]. Noticeable

reductions (1-2 orders of magnitude) in the electrical conductivity start to occur as the porosity approaches 25-30%. Therefore, the SiNW porosity should be less than 25-30% to potentially benefit from the reduction in the thermal conductivity.

In order to roughly approximate if there is a reduction in the electrical conductivity, a qualitative approximation of the porosity within the SiNWs is measured using the gravimetric method. The SiNWs used to determine the porosity were fabricated under the same conditions as the ones used in the TTR measurement. The Si wafer pieces are patterned with the Ag or Ag/Au catalyst (two for each method), weighed (m_1) with an analytical balance (resolution: 0.01mg), and measured for length (L) and width (W) with vernier calipers. After the SiNW arrays are etched, the samples are weighted again (m_2) and measured to determine the VF and array thickness (T) using an SEM. The SiNW porosity for each sample is determined by

$$P = \left(1 - \frac{m_{SiNW}}{m_{Ideal}}\right) \cdot 100\% \quad 3\text{-}3$$

$$m_{SiNW} = V \cdot VF - (m_2 - m_1) \quad 3\text{-}4$$

$$m_{Ideal} = V \cdot VF \cdot \rho \quad 3\text{-}5$$

$$V = L \cdot W \cdot T \quad 3\text{-}6$$

where P is the porosity, m_{SiNW} is the measured SiNW mass, m_{Ideal} is the ideal non-porous SiNW mass, V is the volume, and ρ is the density of Si. An error propagation analysis was carried out for each samples based on the estimated error for each parameter. Unfortunately, an accurate porosity was not able to be determined for the small diameter

SiNWs due to 1) etching on all exposed Si surface at different rates and 2) larger uncertainty in *VF*. The large diameter MACE SiNW array sample porosities are measured and the resulting average values of two samples are shown in Table 2 (additional details can be found in Appendix H). While the Ag-MACE sample with doping concentration of 10^{19} cm^{-3} has a drastic reduction of κ down to 1.0 W/m/K, the high porosity will most likely result in an even more substantial reduction in σ. The Au/Ag-MACE sample with doping concentration of 10^{14} cm^{-3} had a very minor amount of porosity which was capable of reducing κ by ~45 W/m/K will mostly likely have insignificant effects on the electrical conductivity. The Ag-MACE samples with doping concentration of 10^{14} and 10^{16} cm^{-3} achieved a larger reduction in κ; however, the measured porosity is boarding the range for substantial reductions in σ.

Sample	Au/Ag-MACE 10^{14} cm^{-3}	Ag-MACE 10^{14} cm^{-3}	Ag-MACE 10^{16} cm^{-3}	Ag-MACE 10^{19} cm^{-3}
Porosity (%)	3.8	19.0	16.7	74.0
Error (%)	±11.8	±20.1	±15.6	±7.3
K (W/m/K)	98.0	51.3	49.3	1.0
Error (W/m/K)	±11.9	±4.6	±14.4	±0.2

Table 2. Average porosities and thermal conductivities for large diameter MACE samples.

3.5. Section Conclusion

In summary, we measured the thermal conductivity of SiNW arrays with various nanowire diameters, doping concentrations, surface roughness and internal porosities using a nanosecond transient thermoreflectance method. When the SiNW diameter ($d_{avg} \approx$ 350 nm) is larger than the phonon mean free path in the bulk Si, the thermal conductivity shows little dependence on the doping concentration and surface roughness but decreases with increasing porosity due to phonon scattering at the pore interfaces. In contrast, when the SiNW diameter ($d_{avg} \approx$ 130 nm) is smaller than the phonon mean free path, the thermal conductivity strongly depends on both the external boundary-phonon scattering and the internal pore interface-phonon scattering, leading to a reduction in the thermal conductivity for small-diameter SiNWs. A more detail investigation on the electrical conductivity needs to be carried out to determine if the SiNWs will have reduced σ/κ or will lead to an improvement in zT.

Chapter 4. Transfer of Uniform Silicon Nanowire Arrays via Crack Formation

4.1. Background

A major fabrication challenge arises in characterizing the electronic conductivity of vertical SiNW arrays to determine the effect on zT, since Si wire arrays with lengths of a few to tens of micrometers are usually formed by the deposition of vapor onto a Si wafer that is about 500 microns thick, rigid, and opaque, or by the chemical etching of such a wafer. Hence it is a challenge to express and utilize the inherent material properties of the SiNW arrays for devices because the SiNW array properties are typically overshadowed by the properties of the much thicker bulk silicon wafers. Efforts have been made to distinguish the properties of the SiNWs from that of the substrate while maintaining the vertical structure of SiNW arrays. One approach used a heavily doped Si wafer and a thin lightly doped Si layer that was epitaxially grown on top in which the SiNWs were formed by etching [53]. However, growing an epitaxial layer is a time-consuming, expensive process, and this technique is only suitable for investigating lightly doped SiNW arrays. Another approach fabricated SiNW arrays on a SOI wafer and used KOH to selectively removed the backside Si, and as such the optical properties of the SiNW arrays were characterized [54]. It is more desirable to remove vertical NW arrays from their growth substrate and attach the removed array to a different substrate

for vertical devices. One method embedded a Si wire array inside Polydimethylsiloxane (PDMS), which was further peeled off from the substrate, however this method has only been demonstrated for ultra-long wires with large inter wire spacing [158]. The other approach cemented the SiNWs into a 290 nm thick Poly(methyl methacrylate) (PMMA) layer, and fractured the SiNWs from the silicon substrate by applying a shear force while maintaining their vertical alignment in the PMMA [159]. Nevertheless, an extremely high insertion pressure of 55 kg/cm^2 was required to push the array into the PMMA, which resulted in the SiNW tips bundling within the PMMA and damage of the vertical alignment [159]. More importantly, the SiNWs fracture at random locations, which cause the transferred SiNWs to have non-uniform lengths. In this chapter an alternative and yet simple method is introduced that does not rely on mechanical force but rather on chemically weakening the SiNW/Si wafer adhesion by using Ag-assisted electroless etching [124] to form a localized horizontal porous crack, which enables the controlled transfer of uniform, vertically aligned SiNWs to foreign substrates with high quality.

4.2. Controlled Separation of Uniform Length SiNW Arrays

A well-controlled horizontal crack parallel to the wafer surface is formed over a large area through an array of vertically aligned SiNWs. The formation process of the crack is illustrated in Figure 4-1. The SiNW array is fabricated by the well-established Ag-assisted electroless wet etching technique [124]. Silica (SiO_2) spheres are synthesized by a modified stöber synthesis method [115], deposited as a monolayer on a Si(100) wafer via Langmuir-Blodgett assembly, etched by reactive ions to a desired diameter in a gas mixture of O_2 and CHF_3 [72], and followed by e-beam evaporation of a 50 nm thick

silver film (see Appendix E for more details). The SiO_2 spheres are then removed ultrasonically in isopropyl alcohol (IPA), resulting in a honeycomb-pattern silver film, as shown in Figure 2-1a [112, 160, 161]. SiNWs are then formed by immersing the Si wafer in an etchant solution of 4.6 M hydrofluoric acid (HF) and 0.3 M hydrogen peroxide (H_2O_2) [112, 132, 136], where directional etching of Si occurs along the [100] direction [129, 137, 162]. Once the desired SiNW length is achieved by the timed etch, the wafer is rinsed in deionized (DI) water and dried by N_2. Subsequently, the Si wafer is soaked in a 75°C DI water bath for about three hours, which delaminated the Ag film (Figure 4-1c and Figure 4-2e) [163, 164]. Afterwards, the Si wafer is promptly dried by N_2 and immediately returned back into the etching solution. A horizontal crack is formed at the start of the second etch while the etching continued to elongate the SiNWs (Figure 4-1d). Scanning electron microscopy (SEM) images show that the vertically aligned SiNW array has a uniform length (about 5 μm) after the first etch (Figure 4-1e), and is separated into two uniform length layers of 5 μm each after the second etch (Figure 4-1f). A zoomed-in SEM image shows that the Si is partially etched away at the crack location of the SiNWs, which weakens the connection between the top and bottom SiNW array layers (Figure 4-1g).

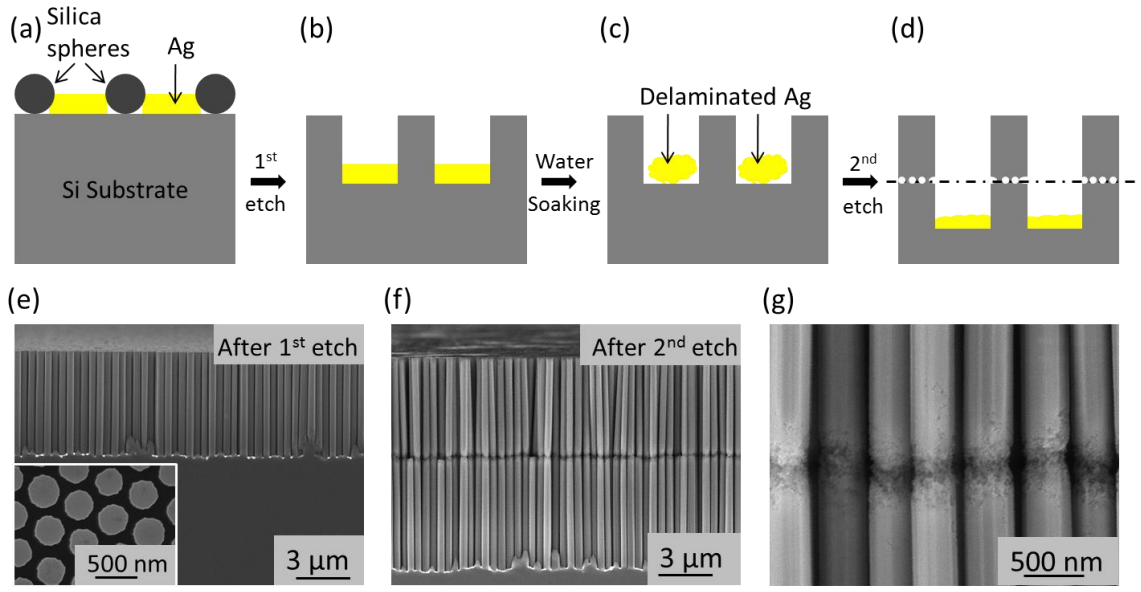


Figure 4-1. Schematic of the fabrication procedure for the cracked SiNW array. (a) Ag film is patterned by using silica spheres, (b) a SiNW array is formed after the first etch, (c) Ag is delaminated from Si after soaking the wafer in 75°C DI water for 3 hours, (d) a horizontal crack is formed after the second etch, along with the elongation of the SiNWs. SEM images of SiNWs (e) after the first etch, (f) after the second etch, and (g) with a zoom-in view of the crack.

4.3. Crack Formation Theory

The formation of the horizontal crack in the SiNWs is closely related to the delamination of the Ag film, and the electrochemical reactions during the etching process. The etching process of the SiNWs consists of two pairs of redox reactions: one occurs at the interface between the Ag film and the etching solution (R1) and the other occurs at the Ag/Si interface (R2) [130, 132, 136].

$$H_2O_2 + 2H^+ + 2e^- \rightarrow 2H_2O \qquad E^0 = 1.77V/SHE \qquad (R1a)$$

$$Ag \rightarrow Ag^+ + e^- \qquad E^0 = -0.79V/SHE \qquad (R1b)$$

$$Ag^+ + e^- \rightarrow Ag \qquad E^0 = 0.79V/SHE \qquad (R2a)$$

$$Si + 6HF \rightarrow H_2SiF_6 + 4H^+ + 4e^- \qquad E^0 = 1.2V/SHE \qquad (R2b)$$

At the Ag/etchant interface, Ag is oxidized by H_2O_2 (R1a and 1b), forming Ag^+ ions in the vicinity of the Ag film (Figure 4-2a) [130, 136, 151]. The formed Ag^+ ions are subsequently reduced back to Ag by (R2a) preferably onto the surface of Ag instead of Si, since Ag is more electronegative than Si [130, 165, 166]. Meanwhile, the Si is oxidized by (R2b) and further dissolved by HF, resulting in the formation of SiNWs [130, 134, 165, 166]. Normally, when the Ag film has good contact with the Si, the production of the Ag^+ ions by R1 is balanced by the consumption of the Ag^+ ions by R2, so the Ag film remains mostly intact. However, when the Ag film is delaminated (Figure 4-2b), the Ag/etchant interfacial area is increased (Figure 4-2b), which speeds up the production rate of Ag^+ ions by R1. Meanwhile, the Ag/Si interfacial contact area is reduced, decreasing the amount of electrons transferred from Si to Ag, which consequently reduces the consumption rate of the Ag^+ ions by R2 [129]. The combination of a faster R1 and a slower R2 results in a surplus of Ag^+ ions in the solution near the Ag film. This buildup of Ag^+ ions allows some of the Ag^+ ions to be reduced and deposited on the Si surface as new Ag particles, particularly in the proximity of the Ag film where the Ag^+ ion concentration is highest. The Ag particles deposited on the sidewalls of the SiNWs will etch horizontally through the SiNWs, leading to the formation of the crack (Figure

4-2b,c). Other Ag particles are deposited underneath the delaminated silver area, leading to the reattachment or "healing" of the Ag film to the Si wafer (Figure 4-2b,c) [129, 132]. The healing process occurs quickly as the second etching step progresses, so the sidewalls of the SiNWs formed during the second etching become smooth again (Figure 4-1g and Figure 4-2c). To confirm this effect, the as-deposited Ag film which has a well-defined pattern and good adhesion to the Si wafer (Figure 4-2d) is soaked in DI water for 3 hours at 75^{o}C, and the Ag film clearly became delaminated afterwards (Figure 4-2e). When we use this delaminated Ag film to etch SiNWs, the top and sidewalls of the SiNWs are very corrugated and some Ag particles could be found on top of and inside of the SiNWs throughout the sample after 1 minute of etching (Figure 4-2f). However after 5 minutes of etching, the sidewalls of the SiNWs became much smoother (Figure 4-2g), indicating that the Ag film is healed. In addition, it can be seen in Figure 4-2g that some Ag particles on top of the SiNWs caused some channel formations inside the SiNWs.

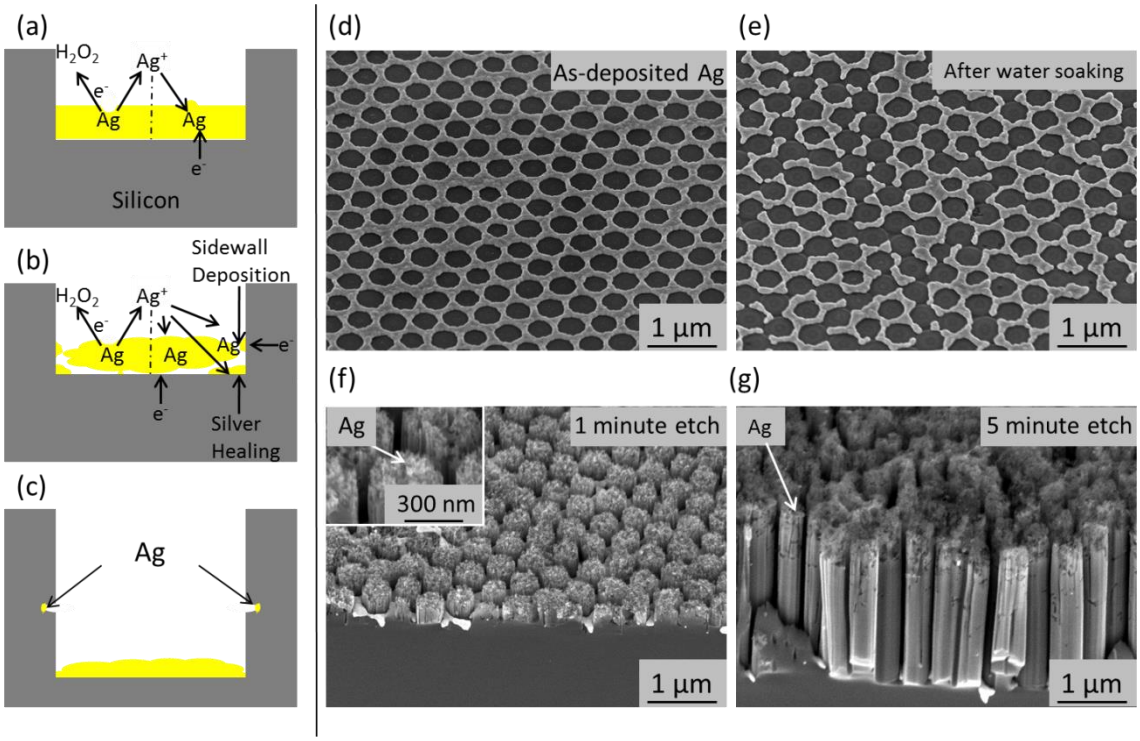


Figure 4-2. The crack formation mechanism. Schematic of (a) the reactions occuring at the etchant/Ag (left) and Ag/Si (right) interface when the Ag has good adhesion with Si, (b) when the Ag is delaminated from the Si, a surplus of Ag^+ ions is formed in the solution, leading to Ag particle deposition on the sidewalls of the SiNWs and on the Si wafer beneath the Ag film, (c) the delaminated Ag film is healed and reattached to the Si wafer while the SiNWs continue to elongate. SEM images of the patterned Ag film (d) as deposited, (e) after soaking in 75°C DI water for 3 hours, and subsequently etched in HF/H_2O_2 mixture for (f) 1 minute and (g) 5 minutes.

4.4. Basic Functionalities

Cracked SiNW arrays can be formed over a broad range of Si wafers, varying in both doping types and doping concentrations. As show in Figure 4-3, cracked SiNW

arrays are successfully formed with both lightly (Figure 4-3a,c) and heavily (Figure 4-3b,d) doped P or N-type Si wafers. It should be noted that the heavily doped SiNWs appear to be somewhat etched during the water soaking step, so their water soaking time is decreased to 30 minutes. Interestingly, as shown in Figure 4-3e, multiple cracks can be created at the desired axial locations along the SiNWs by adding multiple water-soaking steps between the time-controlled etching steps. In addition, the crack formation technique also applies to electrolessly deposited Ag [133]. Figure 4-3f shows that a crack is also formed in a SiNW array fabricated by the steps outlined in Figure 4-1b-d, for which the Ag is electrolessly deposited by soaking the Si wafer in a 0.005 M $AgNO_3$ and 4.6 M HF solution for 1 minute. Finally, it should be noted that the Ag^+ ion diffusion is not entirely localized, which roughens the surface of SiNWs above the crack, as shown in Figure 4-3b,e. Rough surfaces increase the scattering of electrons and phonons in SiNWs, which will reduce the thermal conductivity and the electron mobility. The surface roughness of SiNWs, when undesired, can be reduced by an oxidation process followed by a wet etching step to remove the surface oxide [139, 141].

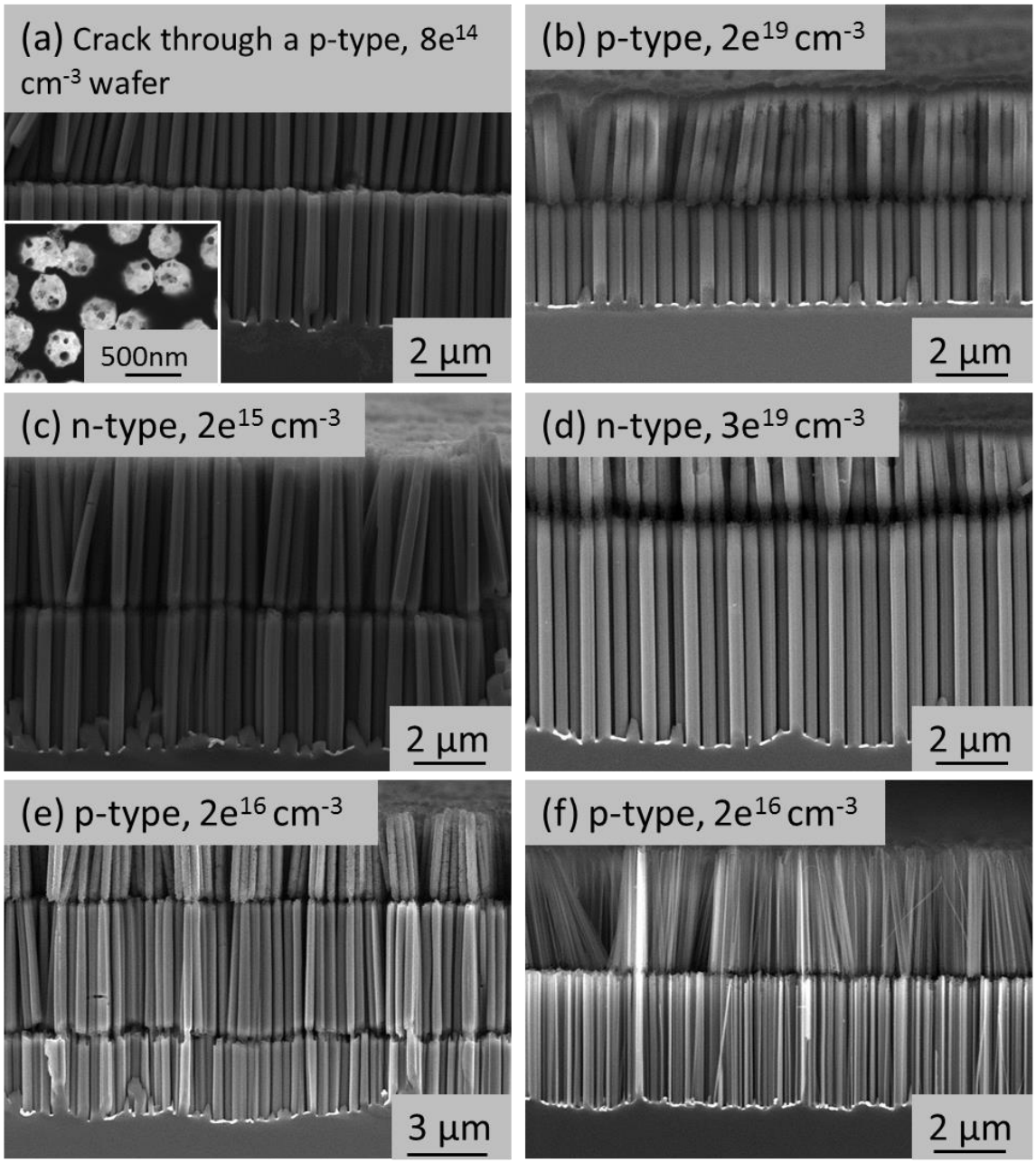


Figure 4-3. Generality of the crack formation. SEM images of cracked SiNWs fabricated using Si substrates that are (a) lightly doped p-type (inset, top view), (b) heavily doped p-type, (c) lightly doped n-type, and (d) heavily doped n-type. (e) SEM image of a SiNW array with two horizontal cracks. (f) SEM image of cracked SiNWs for which the Ag is deposited electrolessly in $AgNO_3$/HF.

Creation of a horizontal crack through SiNW arrays enables the controlled breakage of the SiNWs at specified locations and facilitates their transfer to other substrates. Vertical transfer of the cracked SiNWs is achieved simply by attaching an adhesive surface to the top of the SiNW array and peeling off the adhesive receiver substrate, which fractures the NWs at the crack. The left column of Figure 4-4a demonstrates an example of using a thin spin-coated PMMA film as an adhesive on a receiver substrate [159]. A cracked SiNW array is inserted into the PMMA by hand. The PMMA is then cured on a hotplate at 210°C, which is above the glass transition temperature of the PMMA. This curing step cemented the SiNWs to the receiver substrate. Upon cooling, the Si substrate is easily removed by fracturing the SiNWs at the crack, resulting in the transfer of vertically aligned, uniform length SiNWs to the receiver substrate over a relatively large area as shown in Figure 4-4b. Although a similar PMMA-assisted vertical transfer method has been demonstrated before [159], the presence of the crack greatly facilitates the separation of SiNWs from the donor Si wafer and improves the homogeneity of the transferred SiNW array. Furthermore, the cracked SiNWs can be easily peeled off from their fabrication substrate with adhesive tape, enabling the vertical transfer of SiNW arrays to flexible substrates. For example, Figure 4-4c shows that a SiNW array is transferred to blue tape over a large area, with a high degree of vertical alignment. Finally, horizontal transfer of SiNWs to receiver substrates can be realized by the dry transfer method [167]. The SiNWs easily fracture at the crack during the transfer process, resulting uniform length SiNWs depositing on the substrate with some degree of alignment (Figure 4-4d), which is important for reducing variations

in the performance of NW-based devices. Although fractured SiNWs of uniform length have been demonstrated by using a "knocking-down" approach with an elastomer-covered rigid-roller, this method only applies to pattern planar NW devices on their growth substrate [168]. Our transfer methods, with the presence of a crack through the SiNW array, greatly facilitate the removal of uniform length SiNWs from their original substrates with the option of maintaining their vertical alignment. The transfer methods presented above demonstrate that the presence of a crack through the SiNW array greatly facilities the removal of uniform length SiNWs from their fabrication substrates.

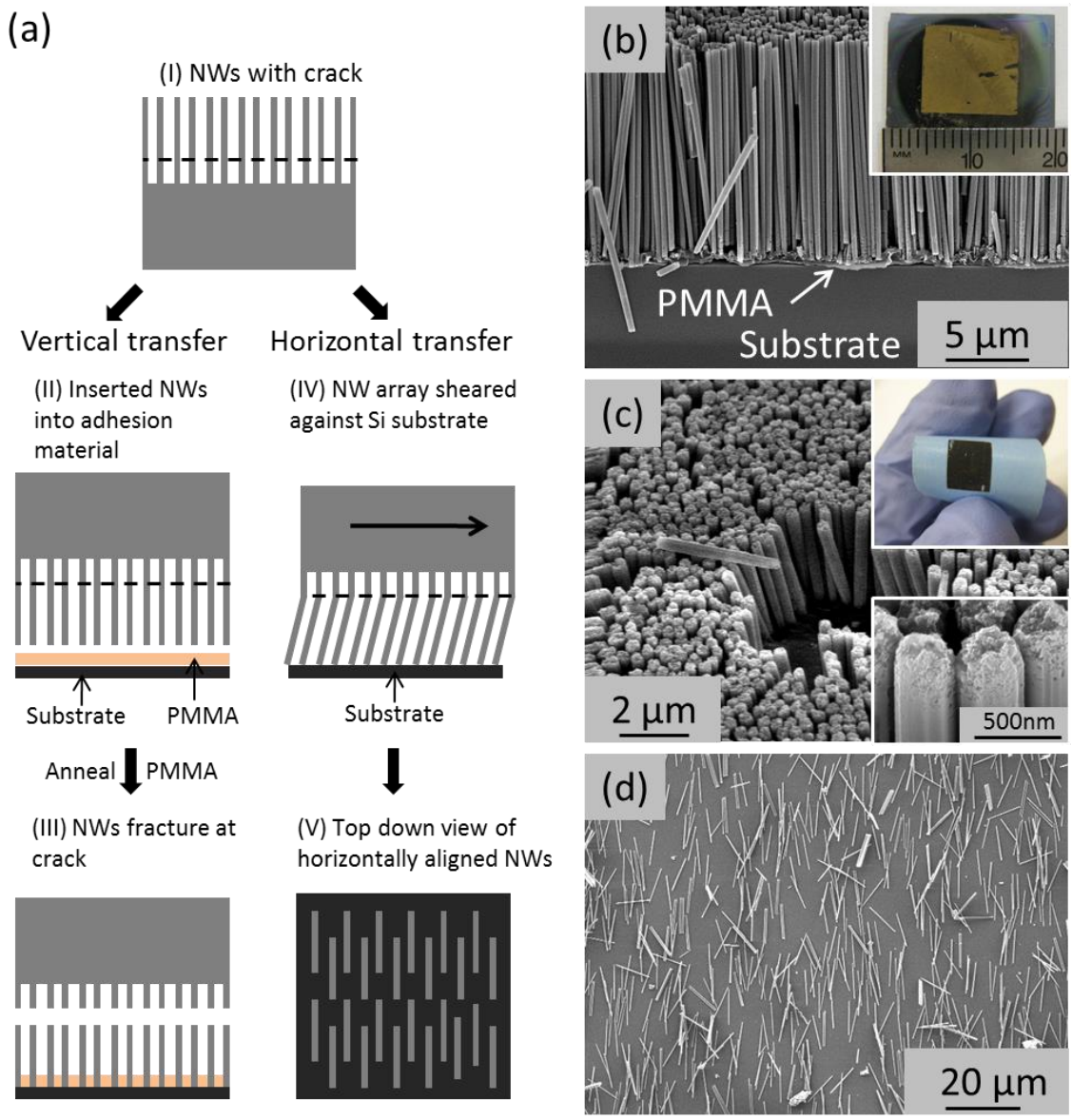


Figure 4-4. Transfer of the cracked SiNWs. (a) Schematic of vertical and horizontal transfers of the cracked SiNWs to foreign substrates. Left column: Vertical transfer of SiNWs by inserting the cracked SiNW array into PMMA, followed by curing of the PMMA, and fracturing of the SiNWs. Right column: Horizontal transfer of SiNWs by applying a shear force on the cracked SiNWs over a receiver substrate. SEM and optical(inset) images of (b) the vertical NWs tranfered to a Si wafer coated with PMMA,

(c) the vertical SiNW array on a blue tape and a zoomed-in view (lower inset) of the rough tips of NWs, and (d) horizontal NWs with uniform length on a Si wafer.

In addition, the formation of the cracked SiNW array enables two other functionalities, i.e., embedding the SiNWs within PDMS and integrating the SiNWs into channels. Embedding NWs within polymer is needed to provide mechanical support and electrical and thermal insulations for NW-based flexible displays and energy harvesting devices [169, 170]. This is typically realized by spin coating hexane-diluted PDMS [158, 171], for which the spinning speed, duration and the dilution of the PDMS need to be varied for NW arrays of different densities and dimensions. For our cracked SiNWs, we simply pour liquid PDMS into a pre-cracked SiNW array. Upon degassing and curing, the PDMS can be peeled off along the cracked interface, forming a receiver and a donor substrate (Figure 4-5a). The receiver substrate (Figure 4-5c) is a flexible piece of PDMS with vertically aligned SiNWs embedded in one side. The donor substrate (Figure 4-5d) consists of the bottom SiNW layer embedded in the PDMS, for which a metal contact can be easily deposited on top to form vertical SiNW devices. This is a simpler and more uniform technique to create polymer filled SiNW arrays over a large area compared to the spin coating method [170]. The other opportunity facilitated by the crack is the formation of a silicon trench with vertically aligned NWs at the bottom, which can increase the surface area or promote mixing of a microfluidic channel without generating a significant pressure drop [172]. As shown in Figure 4-5b, the trench is formed by patterning the Ag film at selected areas, forming a cracked SiNW array, and removing the top SiNW layer

with an adhesive material, such as tape. The SEM image in Figure 4-5e shows that uniform SiNWs are formed at the floor of the Si trench.

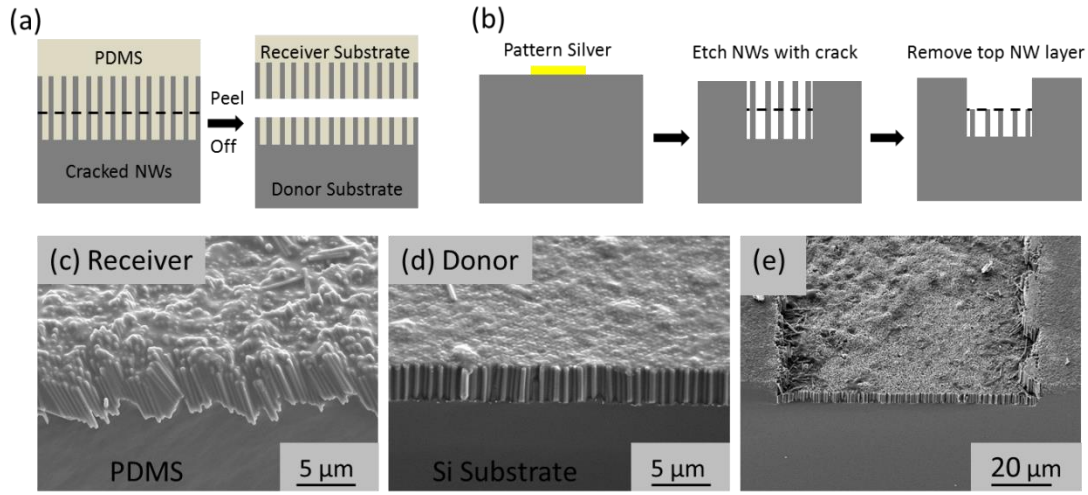


Figure 4-5. (a) Schematic of embedding vertically aligned SiNWs in PDMS, SEM images of (c) the corresponding receiver and (d) the donor substrates after peeling off the PDMS. (b) Schematic and (e) SEM image of the fabricated vertical SiNWs along the base of a trench.

4.5. Section Conclusion

In summary, we present a simple water soaking technique to form horizontal cracks through Ag-assisted top-down SiNW arrays. The formation of the crack is caused by the delamination of the Ag film during the water soaking step, and redistribution and reattachment of the Ag film during the subsequent wet etching step. Some of the Ag is redistributed as particles to the sidewalls of SiNWs close to the Ag film, which leads to a localized horizontal etch of the SiNWs forming the crack thereby weakening the SiNW/Si wafer adhesion. Single or multiple cracks can be formed over various Si wafers

with different doping types and doping concentrations. Furthermore, the crack enables the breakage of SiNWs with uniform lengths and greatly facilitates the vertical transfer of uniform SiNW arrays to other adhesive substrates, such as tape and PMMA coated substrates. In addition, the crack enables embedding the SiNWs within PDMS and integrating the SiNWs into channels. We believe that all the functionalities enabled by the crack may help facilitate the realization of vertical SiNW devices capable of characterizing and utilizing the electronic conductivity for thermoelectric devices.

Chapter 5. Fabrication of Flexible and Vertical Silicon Nanowire Electronics

5.1. Background

In addition to characterizing thermoelectric devices, the anisotropic electronic and optical properties, large surface to volume ratios, resistance to Li-ion pulverization and abilities to orthogonalize light absorption and carrier transport directions make vertical SiNW arrays important building blocks for various applications, ranging from vertical surround-gate field-effect transistors [173-175], sensors [43, 45, 47], solar cells [53, 58, 176], and Li-ion batteries [60, 62-64]. Many of these applications desire vertical SiNW arrays to be fabricated on non-silicon based substrates in order to endow the final devices with the properties of flexibility, transparency, and light-weight [46, 159, 177]. Nevertheless, fabrication of vertical SiNW array devices on non-Si based substrates faces three significant challenges: 1) detaching SiNW arrays with uniform length from their original fabrication substrates, typically Si wafers, while maintaining their vertical orientation; 2) attaching the detached SiNW arrays to any receiving device substrates, again retaining their vertical orientation; and 3) forming metallic contacts on both ends of the SiNWs with mechanical support and electrical insulation in between. Although a number of methods, such as dry transfer [167, 178], transfer printing methods (TPMs)

[46, 179, 180], and water-assisted TPM [181], have been developed to fabricate *horizontal* NW electronics on non-Si based substrates, a methods has yet to be developed capable of fabricating *vertical* SiNW devices on non-Si based substrates that forms electrical contacts to both sides of the array [53, 177, 182]. In Chapter 4, a method capable of forming a horizontal crack through a metal-assisted etched SiNW array was introduced. In this chapter a new crack-assisted vertical-transfer printing method (V-TPM) will be used to fabricate vertically aligned SiNW electronic devices with metallic contacts on both ends on arbitrary substrates, such as plastic sheets, metal foils, and glass slides will be introduced that utilizes the crack formation method.

5.2. Fabrication Methodology

Our method essentially relies on the formation of a horizontal crack across the SiNW arrays, resulting in easy detachment of the NW arrays with uniform length from their fabrication substrates [152]. The fabrication process of the vertical SiNW array devices with this crack-assisted V-TPM is illustrated in Figure 5-1. First, vertically aligned SiNWs are formed on top of a (100) p-type Si wafer (dopant concentration of ~10^{14} cm^{-3}) by Ag-assisted electroless etching [53, 177, 182] and a horizontal crack across the SiNWs is formed by inserting a water soaking step between two consecutive etching steps (Figure 5-1a) [152]. The water soaking step causes the delamination and redistribution of Ag, leading to new horizontal etching pathways to form the crack [152]. Next, the SiNW array is filled with hexane diluted PDMS (2:1) by spin coating, for mechanical support and electrical insulation purposes (Figure 5-1b). Then the PDMS is further dry etched by a plasma reactive ion etcher (Stanford's SNF MRC etcher) with 15

sccm CHF_3, 5 sccm O_2, 150 W plasma power, 50 mtorr chamber pressure to expose the SiNW tips (Figure 5-1c). The etch time varied from sample to sample due to variations in the PDMS thickness. Then, a metal contact consisting of the sequential deposition of Ti, Pd, and Al with respective thicknesses of 5, 200, and 500 nm are deposited on the exposed SiNW tips with an electron beam evaporator after a brief HF etching to remove the native oxide on the surface (Figure 5-1d). Subsequently, the sample is flipped over and attached to any arbitrary receiver substrate coated with a thin conductive silver epoxy (Ted Pella, part number: 16043) layer (~50 μm) (Figure 5-1e). Once the silver epoxy is fully cured, the Si substrate is detached from the SiNW array at the horizontal crack line with the assistance of a gentle shear force, leaving behind the SiNW array embedded in PDMS on the receiver substrate (Figure 5-1f). The other metal contact (Ti/Pd/Al 5/200/500 nm) is deposited through a shadow mask with ~300 μm diameter holes (machined from stainless steel) on top of the SiNW tips after dry etching of PDMS for NW tip exposure and HF etching for native oxide removal. Finally, vertical SiNW arrays with metal contacts on both ends are fabricated on arbitrary substrates (Figure 5-1h).

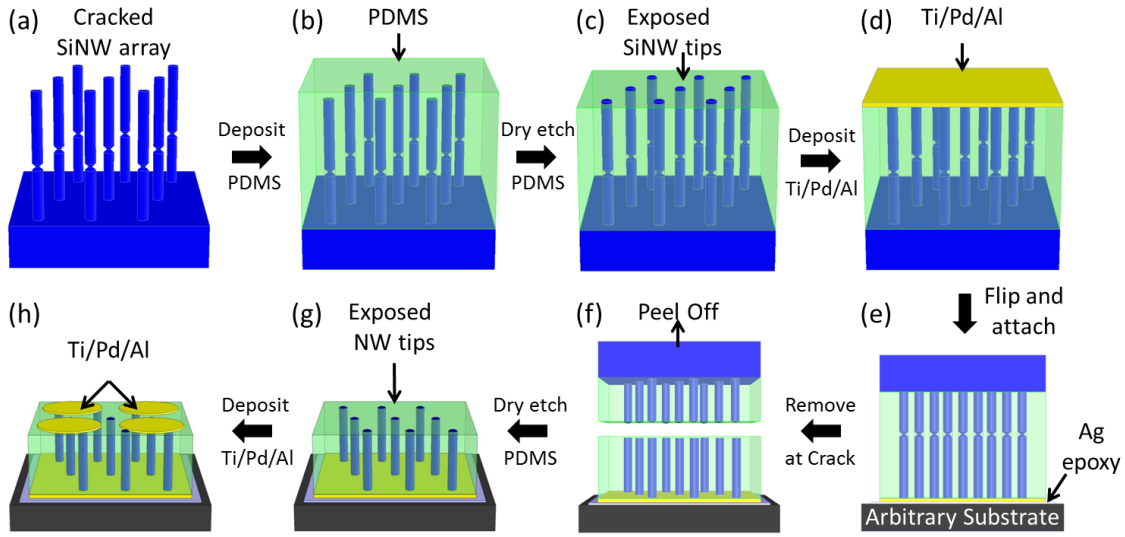


Figure 5-1. Schematic of the fabrication procedure for vertical SiNW array electronic devices on non-Si based substrates with the crack-assisted V-TPM. (a) Cracked vertical SiNW arrays are formed by inserting a water soaking step between two consecutive Ag-assisted chemical etching steps; (b) SiNWs are filled with hexane-diluted PDMS for mechanical support and electrical insulation; (c) SiNW tips are exposed after dry etching of PDMS; (d) metal contact is deposited over the exposed SiNW tips; (e) the metal contact side of the Si wafer is attached to an arbitrary substrate with a thin layer of silver epoxy in between. (f) The vertical SiNW array is separated from the donor Si wafer at the crack location by peeling off; (g) the other side of SiNW tips is exposed after dry etching of PDMS; (h) the other metal contact is deposited on the exposed SiNW tips over a shadow mask with 300 μm diameter holes to complete the vertical SiNW array device.

Figure 5-2 shows representative SEM images of SiNWs at different stages of the fabrication process as illustrated in Figure 5-1. Figure 5-2a shows that vertical SiNW arrays of uniform length (tens of μm) are etched on top of a Si wafer with a horizontal

crack formed close to the base of the array (corresponding to Figure 5-1a). Figure 5-2b shows that after PDMS infiltration and reactive ion etching (corresponding to Figure 5-1c), the SiNWs tips are fully exposed and ready for metal contact deposition and that PDMS nicely filled in between SiNWs, providing good mechanical support and electrical insulation. Figure 5-2c shows that the cracked end of the SiNW array, right after separating from the Si substrate, is covered by a thin layer of PDMS. Figure 5-2d shows the cross section of a final device that is composed of uniform and vertical SiNW arrays sandwiched between two metal contacts and attached to an arbitrary substrate by a conductive Ag epoxy layer (corresponding to Figure 5-1h).

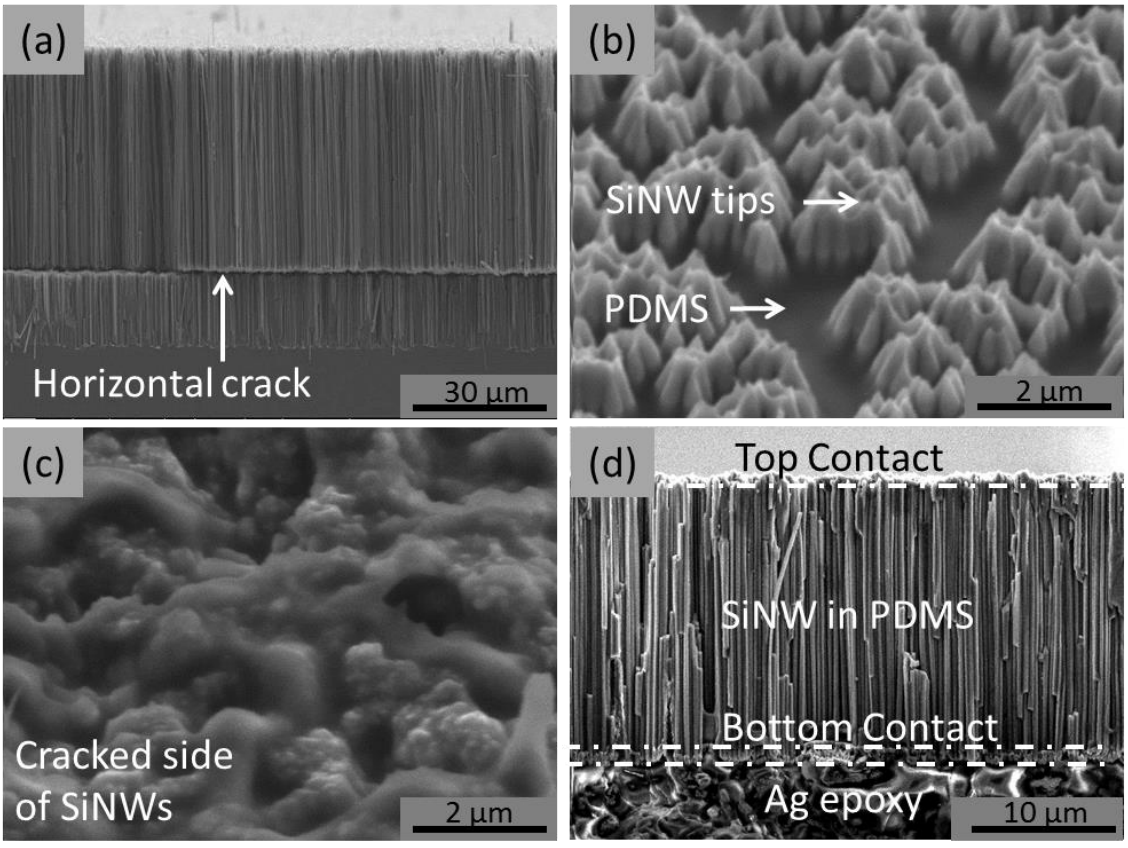


Figure 5-2. SEM images of (a) as-fabricated cracked SiNW array, (b) the exposed SiNW tips after the first PDMS etching, (c) the cracked end of the SiNWs embedded in PDMS

right after separation from the donor Si wafer, and (d) the completed vertical SiNW array with metal contacts on both ends that are attached to an arbitrary receiver substrate by the Ag epoxy.

5.3. Marginally-porous SiNW Devices

With our crack-assisted V-TPM, vertical SiNW array devices are successfully fabricated over a range of non-Si based substrates, including conductive and flexible metal foils (Figure 5-3a), transparent glass slides (Figure 5-3b), and transparent and flexible plastic sheets (inset of Figure 5-4b). The current-voltage (I-V) curves of the final devices exhibit characteristics that are similar among the various receiver substrates but different depending on the SiNW morphology. The SiNW morphology can be tuned by varying a few parameters during the etching process to reduce the excess Ag^+ ions in the etchant solution from depositing along the NW surface that generates porosity inside SiNWs. For example, marginally-porous SiNWs with relatively rough surfaces are fabricated by maintaining a low excess Ag^+ ion concentration in the solution throughout the etching process (*e.g.,* adding Au on top of Ag to increase the metal's stability [85], reducing the H_2O_2 concentration [148, 151], decreasing the etching time [148, 151], reducing the Ag thickness [148], using a low wafer doping concentration [148, 149], and optimizing the Ag delamination step to reduce the SiNW sidewall etching). These marginally-porous SiNWs, as shown in Figure 5-3c, have linear I-V curves with an average electrical conductivity value around $2.9 \cdot 10^{-3}$ S/cm, demonstrating that our crack-assisted V-TPM forms good quality metal-Si contacts during the device fabrication process; however, still sustained two order or magnitude reduction in electrical

conductivity compared to bulk. This reduction could be contributed to several factors such as a surface depletion layer, preferential etching of dopant atoms, or slight porosity around the crack location interfering with the electronic transport.

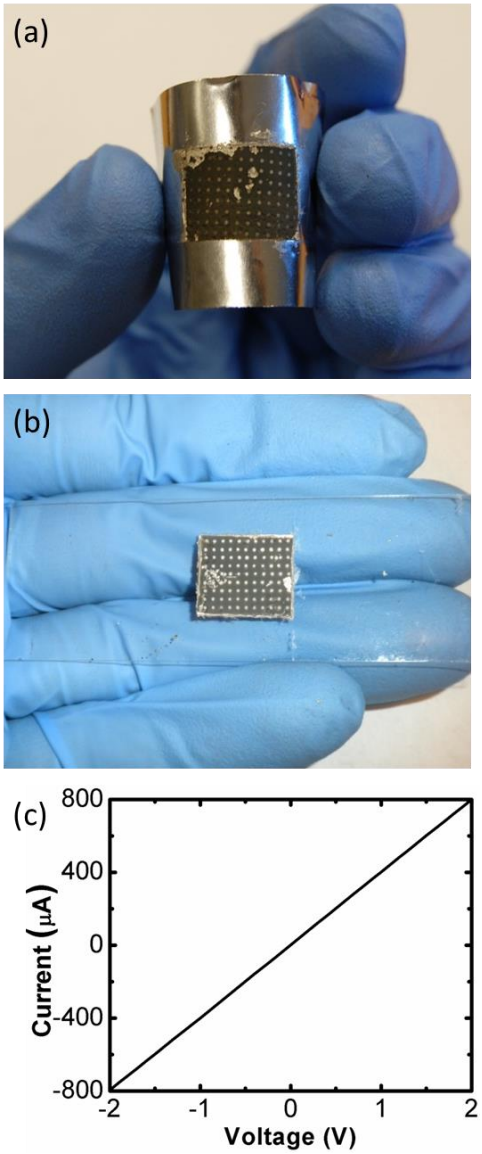


Figure 5-3. Optical images of vertical maginally-porous SiNW devices fabricated on (a) a stainless steel foil and (b) a transparent glass slide with the (c) I-V curve of a typical vertical marginally-porous SiNW device. The linear I-V characteristics demonstrate that

the crack-assisted V-TPM forms ohmic contact to the SiNW tips on both sides of the array.

5.4. Porous SiNW Devices

On the other hand, porous SiNWs are frequently formed during the Ag-assisted electroless etching process if the Ag^+ ion concentration in the etchant solution is not well controlled by the above mentioned methods [73, 124, 148, 149, 151, 183]. The porosity of these SiNWs is clearly shown throughout the length of the NW array in the cross-sectional SEM images in Figure 5-4a, where the porosity is particularly increased where an etching step is initiated (*i.e.*, around both the NW tips), due to the initial local increase in the Ag^+ ion concentration. These porous vertical SiNW arrays fabricated by this crack-assisted V-TPM exhibit quasi-linear I-V curves at low voltages (-2 to 2 volts) but nonlinear I-V curves at higher voltages (inset of Figure 5-4b). We believe that the nonlinear behavior under relative high voltages originates from the electron transport properties in the porous SiNWs. Porous Si has been shown to have nonlinear I-V characteristics [156, 184-189] and resistivity values five orders of magnitude larger than crystalline silicon due to the depletion of free charge carriers [79, 156]. Upon closer investigation of the porous SiNW device I-V curves, it is found that at higher voltages the conductance (I/V) shows an exponential dependence on the square-root of applied voltage as shown in Figure 5-4c, and such dependence is best described by the Poole-Frenkel relationship shown in Equations (5-1) and (5-2).

$$G(V,T) = G_o exp\left[\frac{-E_A}{k_B T}\right] exp\left[\frac{V}{V^*}\right]^{1/2} \quad 5\text{-}1$$

$$\sqrt{V^*} = \frac{k_B T}{e} \Big/ \left[\frac{e}{\pi \epsilon d}\right]^{1/2} \quad 5\text{-}2$$

Here, G is the conductance of porous Si, G_o is the conductance prefactor, E_A is the activation energy to release a trapped charge carrier from coulombic traps, k_B is the Boltzmann's constant, T is the device temperature, V is the applied voltage, V^* is a parameter reflecting the material characteristic, e is the elementary electron charge, ε is the dielectric constant, and d is the length of the porous channel. The Poole-Frenkel relationship attributes the nonlinear I-V characteristics to an electric-field-enhanced thermal excitation of charge carriers from coulombic traps, for which the activation energy to release a trapped carrier is reduced with increasing electric fields, leading to the non-linear voltage dependence [156, 184, 190-192]. At low voltages, the metal-porous Si contacts will exhibit a quasi-ohmic contact, corresponding to the low voltage quasi-linear I-V curves (inset of Figure 5-4b). The average conductivity values extracted from the I-V curves between -2V to 2V, is $2.1 \cdot 10^{-6}$ S/cm, which is roughly three orders of magnitude lower than the average sample in Figure 5-3 and five orders of magnitude lower than the conductivity calculated on the basis of the wafer property, indicating the porous nature of the SiNWs. The marginally-porous NWs are believed to have lower conductivity than the initial bulk wafer due to the increased surface charge carrier depletion from the rough surface inherently formed by the Ag-assisted chemical etching process [151]. Nevertheless, as the voltage is increased in the porous SiNWs, the electric field enhances the thermal excitation of charge carriers from coulombic traps, causing the conductance (G) to increase with V in the form of $\exp(V^{1/2})$ [184, 191]. To confirm this behavior

associated with porous SiNWs, we calculated the activation energy associated with releasing trapped carriers by the slope of the zero-field conductance values vs. 1/T curve (Figure 5-4d) using the Arrhenius relation according to Eq. 1, where the zero-field conductances at any specified temperature are obtained by extrapolating the conductances measured under different bias to zero bias (Figure 5-4c, marked by the open red circles) at that temperature. As a result, the obtained activation energy is about 0.25 eV from Figure 5-4d, and generally in the range of 0.23 – 0.32 eV, which is comparable to the 0.14 to 0.5 eV activation energies for bulk porous Si films formed by anodization using the same Poole-Frenkel relation [156, 184, 192, 193].

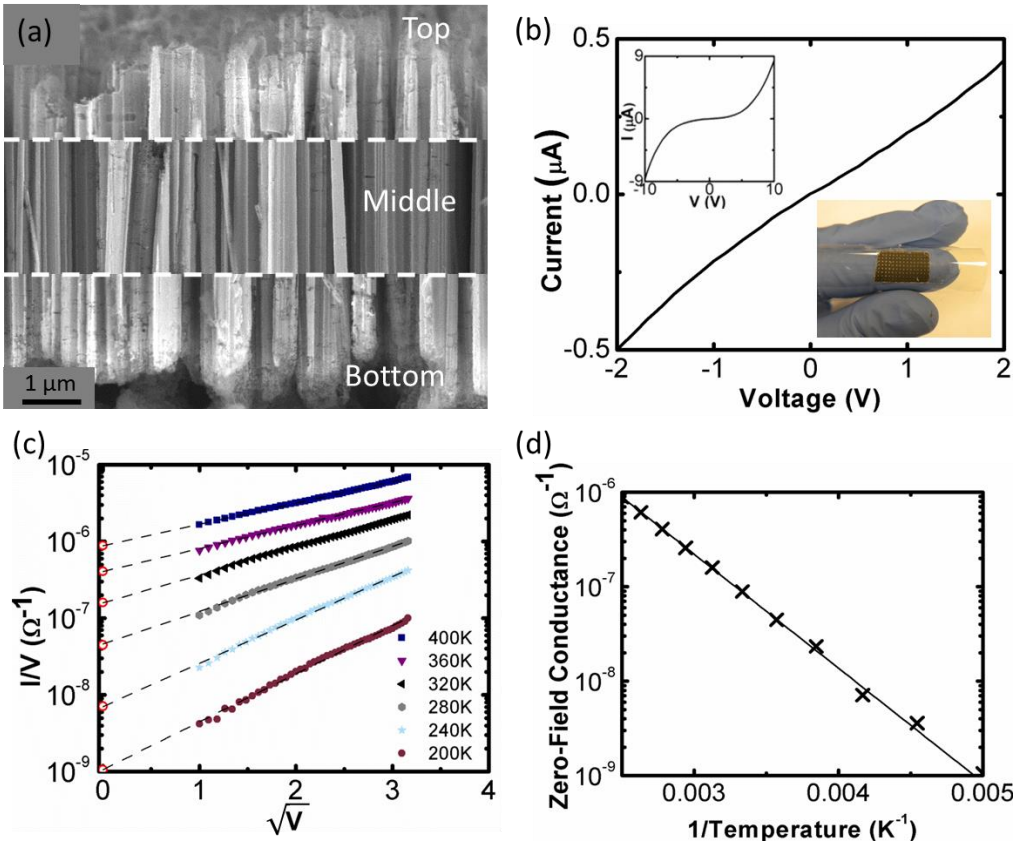


Figure 5-4. (a) Cross sectional SEM images of the top, middle and bottom sections of an Ag-assisted electroless etched SiNW array clearly show that the SiNWs are porous. (b)

I-V curve of a vertical porous SiNW device fabricated on a plastic sheet. Insets show the device optical image and the I-V curve over a large voltage range. (c) Measured conductance (I/V) of a SiNW array vs. the square root of the applied voltage measured at various temperatures (symbols), which shows good agreement with the Poole-Frenkel transport relation in Eq. 1. The zero-field conductances (open red circles) are obtained by linearly extrapolating the measured conductance values to zero volt. (d) The zero-field conduction is plotted as a function of 1/Temperature, where the slope is used to calculate the activation energy associated with releasing trapped carriers from coulombic trap sites.

5.5. Axially-Modulated SiNW Devices

Our crack-assisted V-TPM can be also applied to axially modulated p-n SiNWs (Figure 5-5). The axial p-n SiNWs are fabricated by etching a p-n wafer with approximately a 10 μm thick n-type layer (dopant concentration of ~10^{18} cm^{-3}) on top of a p-type wafer (dopant concentration of ~10^{16} cm^{-3}). The location of the crack is controlled such that both the p and n segments exist above the crack. The axially modulated p-n SiNW array device is successfully transferred on a Kapton sheet (Figure 5-5b) and showed a clear rectifying behavior (Figure 5-5c), indicating the formation of a diode. Importantly, the rectifying I-V curve remains almost the same under different bending radii (8 – 68 mm) of the Kapton sheet, demonstrating the good flexibility of the final vertical SiNW devices.

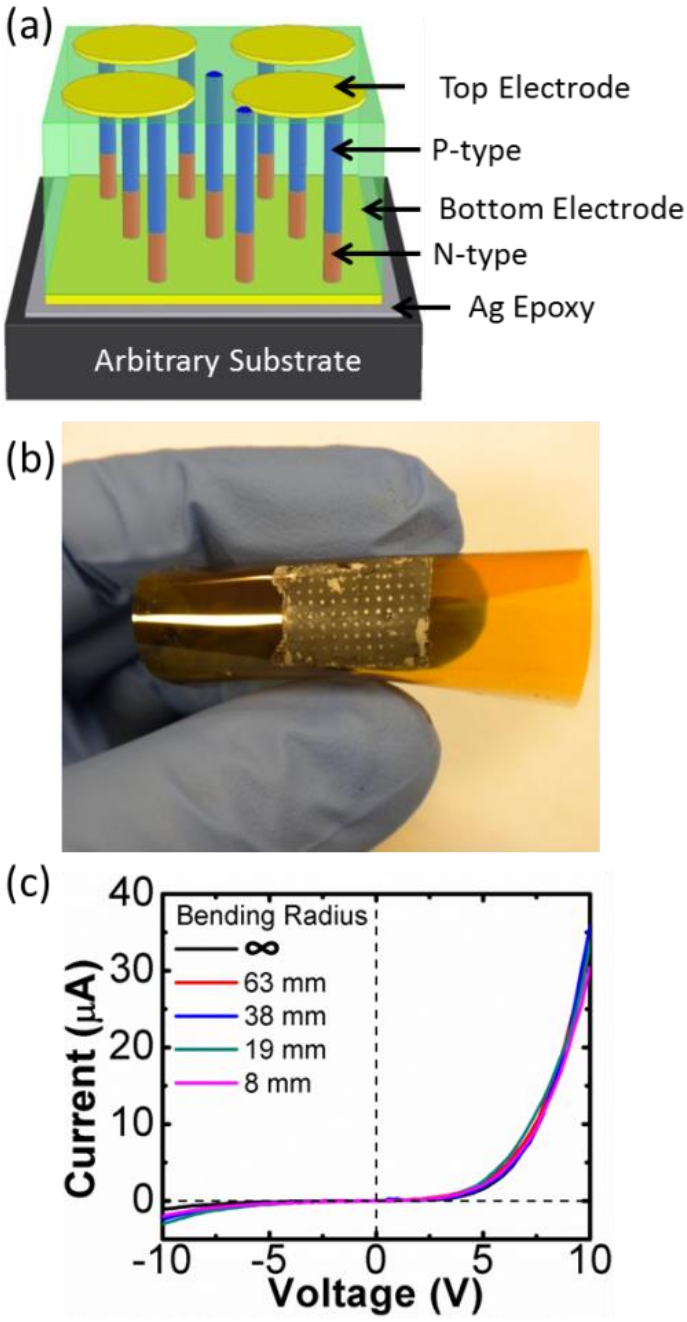


Figure 5-5. (a) Schematic and (b) optical image of axially-modulated vertical p-n SiNW array devices fabricated on a Kapton sheet. (c) The corresponding I-V curve shows nearly identical rectifying behavior under various bending radii.

5.6. Section Conclusion

In summary, we demonstrated a new crack-assisted V-TPM to fabricate vertically aligned SiNW array electronic devices on arbitrary substrates, including plastic sheets, metal foils, and glass slides. The crack-assisted V-TPM overcomes three major challenges of fabricating vertical SiNW devices: 1) detachment of vertically aligned SiNW arrays from Si substrates by forming horizontal cracks, 2) attachment of the vertical SiNW arrays to arbitrary substrates by using conductive Ag epoxy, and 3) formation of metallic contacts on both sides of the SiNW array by infiltrating PDMS in between SiNWs and etching the top PDMS layer to expose the SiNW tips. The I-V curve characteristics of the completed vertical SiNW arrays are independent of the substrate materials, but mainly depend on the porosity of the SiNWs. Marginally-porous SiNWs exhibit linear I-V curves, demonstrating the good fabrication quality by the crack-assisted V-TPM. Porous SiNWs have quasi-linear I-V curves at low voltages and evolve to an $\exp(V^{1/2})$ dependence at higher voltages due to the Poole-Frankel effect in porous Si. The I-V curves of the axially modulated p-n SiNWs exhibit clear rectifying behavior indicating the excellent control of the crack location and generality of this method. Future work will require expanding on the crack-assisted V-TPM to develop the next generation of V-TPMs that can eliminate the reduction in electrical conductivity for devices that require peak electrical performance such as thermoelectrics. We believe that our crack-assisted V-TPM will still greatly facilitate the fabrication of large area, high density vertical SiNW devices on non-silicon based substrates for various applications while initiating the development of new V-TPMs capable of transferring non-porous SiNWs for thermoelectric devices.

Chapter 6. Electro-assisted Transfer for Vertical Silicon Wire Arrays

6.1. Background

Separation of the Si wire arrays from the parent Si wafer allows the electrical, thermal, optical and mechanical properties of the Si wire arrays to be isolated and harnessed in devices without being overshadowed by the properties of the thick parent Si wafer, and enables the transfer of the Si wire arrays to other flexible, lightweight, low cost or transparent substrates for enhanced device functionality. A key requirement for the separation and transfer of Si wire arrays is the preservation of their original properties and orientation. A range of methods have been developed for the separation of Si wire arrays from their parent Si wafers, which rely on the mechanical breakage of the Si wires by the application of peeling forces [158, 194, 195], direct shear forces [159, 177, 196], or the creation of a horizontal porous crack within the Si wires [150, 152]. However, these methods require that the Si wires are held together during the mechanical breaking process by encapsulation in a polymer host, the existence of which makes it difficult to use the separated Si wires for applications that require an exposed Si surface, such as for ohmic contacts to metal electrodes, sensors or catalysts. In addition, some of these methods are only compatible with Si wires of certain geometries [158, 159, 177, 194-196] or those made by particular methods [150, 152]. To address these shortcomings, we have developed, and report herein, a new electro-assisted transfer printing method for the transfer of vertical Si wire arrays from their parent Si wafers to other substrates without modification to the properties and orientation of the Si wires, without constraints on the

Si wire geometry or fabrication method, and without the need for polymer encapsulation. The fundamental understanding gained from this new electro-assisted transfer method also enabled us to develop a current-induced metal-assisted chemical etching method for the facile and rapid synthesis of Si nanowires with axially modulated porosity.

6.2. Fabrication Methodology

Our electro-assisted transfer method relies on a sacrificial porous Si layer [197, 198] for the separation of vertical Si wire arrays (both nanowires and microwires) from their parent Si wafers by the general procedure illustrated in Figure 6-1. Si wires are first formed by either deep reactive ion etching (DRIE) or metal-assisted chemical etching (MACE) of a p-type Si wafer (boron dopant concentration of 10^{14} cm^{-3}) (Figure 6-1a for schematic and 1f for scanning electron microscopy (SEM) image). An aluminum (Al) film is then deposited on the back of the Si wafer to serve as an electrode for the following electro-etching process. Then the parent Si wafer with the Si wire array on top is placed in a Teflon anodization cell filled with an ethanolic HF electrolyte solution (1:1 v/v mixture of 48% HF and 100% ethanol) (Figure 2-1). A constant current of 50 mA/cm^2 is applied for 20 minutes between the Al electrode on the back of the Si wafer and a platinum (Pt) counter electrode submerged in the ethanolic HF solution, which leads to formation of a porous Si layer of about 15 μm thickness beneath the Si wire array (Figure 6-1b). The porous Si layer, together with the Si wire array on top, is subsequently separated from the parent Si wafer by the standard electropolishing method (Figure 6-1c) [77, 78, 90-92]. The electropolishing is achieved by applying 50 mA/cm^2 between the Al and Pt electrodes in a 1:4 v/v mixture of 48% HF and 100% ethanol for

15 seconds (Figure 2-1) [92, 199]. The electropolishing process has lower HF concentration (25% vol.) than that of the electro-etching process (50% vol.). The smaller concentration of HF in the etchant reduces the diffusional flux of F^- ions to the Si surface. As such, the Si surface is oxidized to form a continuous oxide layer (instead of individual pores) and the entire oxide layer is subsequently removed as a "lift-off". Figure 6-1g and h are the SEM and optical images of the Si nanowires on top of the porous Si layer after the electropolishing step, and both images show that the porous Si layer, together with the top Si nanowires, is separated from the parent Si wafer. Figure 6-1h shows a case where the porous Si layer (white dotted circle showing the size of the Si area exposed in the anodization cell) is already lifted off from the parent Si wafer by electropolishing. The degree of electropolishing can be tuned from slightly weakened to severely weakened by changing the electropolishing time and applied current. Next, the entire Si wafer is gently removed from the anodization cell and dried in a critical point drier to prevent the porous Si layer from cracking. Subsequently, the porous Si layer with the top Si wire array is easily removed from the Si parent wafer, flipped over and attached to an arbitrary flat substrate by an adhesive (e.g., polyvinyl alcohol, Ag epoxy) (Figure 6-1d). The porous Si layer is then etched away in a 0.03 M KOH solution containing 10% ethanol for 30 minutes, which is capable of removing the porous Si layer without causing much damage to the Si wires due to the low concentration of KOH (Figure 6-1e) [77, 197, 198].

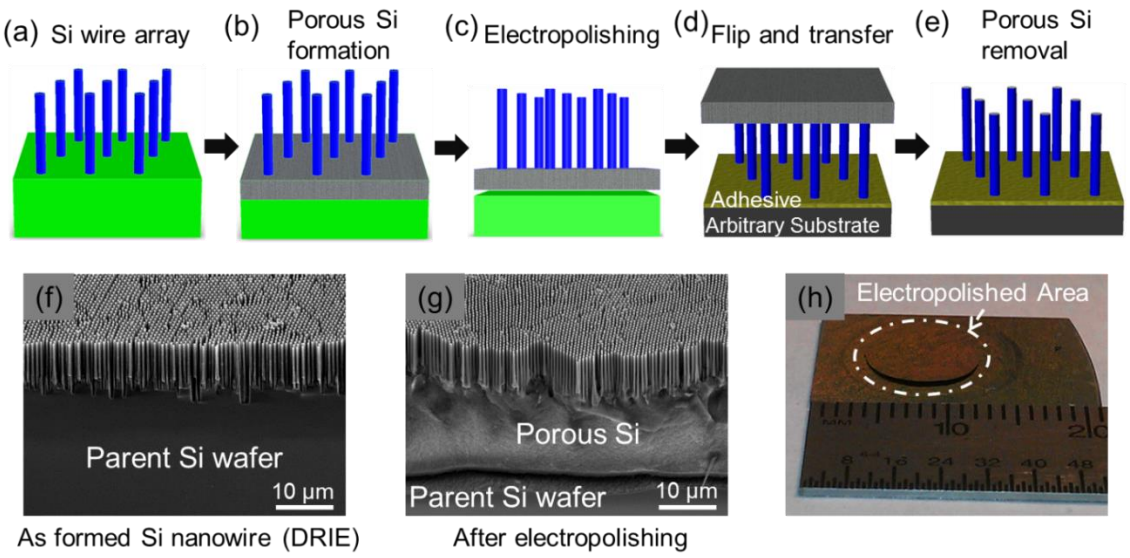


Figure 6-1. Schematic of the electro-assisted transfer of vertical Si wire arrays. (a) A vertical Si wire array is fabricated on a parent Si wafer, (b) a sacrificial porous Si layer is formed beneath the Si wire array by electro-etching the parent Si wafer, (c) the porous Si layer, together with the top Si wire array, is detached from the parent Si wafer by electropolishing, (d) the Si wire array supported by the porous Si is flipped over, attached and transferred to any flat substrate coated with an adhesive, (e) the porous Si layer is etched away. SEM images of the Si nanowires (formed by DRIE) (f) before and (g) after the porous Si layer is electropolished from the Si wafer. (h) An optical image showing that the Si nanowire array held together by the porous Si layer is lifted off from the parent Si wafer after the electropolishing step.

6.3. Controlled Location for Porous Silicon Formation

One key requirement for our electro-assisted transfer method is that the formation of porous Si should be restricted to the Si underneath the Si wires, not within the Si wires, in order to preserve the original properties of the Si wires. Porous Si is formed

only when holes (h^+), reach a Si surface that is exposed to hydrofluoric acid [200]. Therefore, in order to prevent the Si wires from becoming porous, the holes should be directed away from the Si wire surface. This can be accomplished by controlling the width of the space-charge region (SCR) at the Si surface that is in direct contact with the electrolyte. The SCR is depleted of mobile charge carriers, behaving as a nearly insulating region. Since the porous Si is formed under a forward bias conditions, the current of holes has to pass the SCR region first and then reach to the Si surface; naturally the holes will select the least resistive pathway. When the width of the SCR (W_{SCR}) is larger than the radius of the Si wires ($r_{Si\ wire}$) (Figure 6-2a) and the conductivity of the ethanolic HF etchant solution (estimated to be ~1 S/cm) [199, 201] is much larger than the conductivity of the depleted Si wires [202], the least resistive pathway for holes is through the gaps between the Si wires, not through the Si wires, leading to little porosity formation within the Si wires (Figure 6-2b) [202-204]. On the other hand, when W_{SCR} is smaller than $r_{Si\ wire}$, the holes can go through the inside of Si wires (Figure 6-2c), leading to porosity inside the Si wires and in the Si underneath the wires (Figure 6-2d).

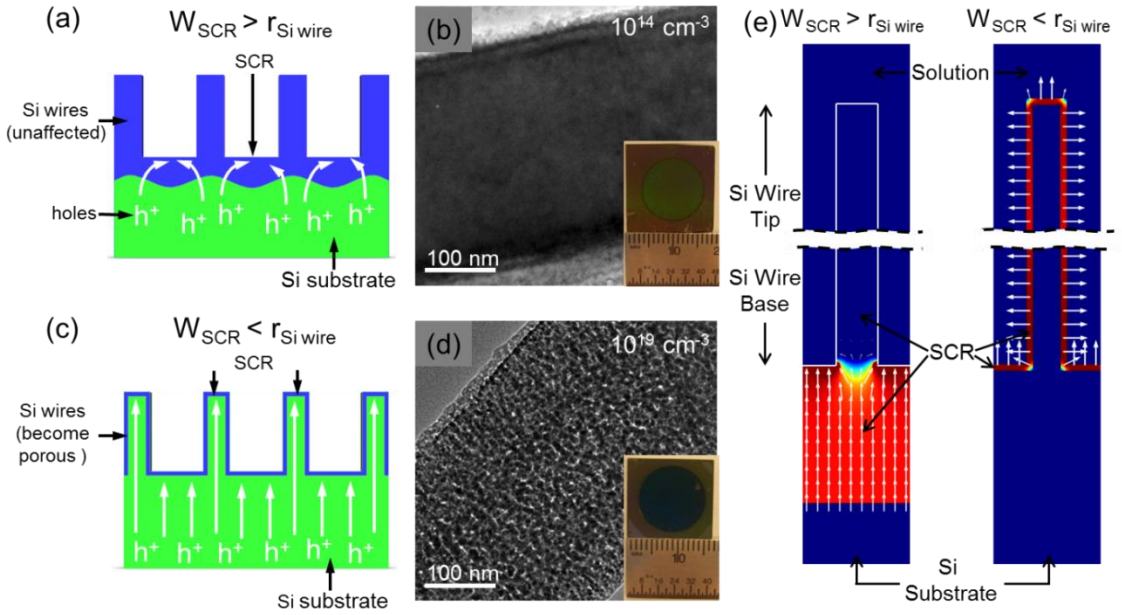


Figure 6-2. The location of the space-charge region determines the distribution of the electric field and therefore the location of the porous Si formation. Porous Si forms underneath the Si wires when the space-charge region (blue) width (W_{SCR}) is greater than the Si wire radius ($r_{Si\ wire}$) (a, b) and inside the Si wires when $W_{SCR} < r_{Si\ wire}$ (c, d). TEM and optical images (insets) show that the p-type Si nanowires with doping concentrations of (b) 10^{14} cm^{-3} and (d) 10^{19} cm^{-3} have different internal porosity after the porous Si layer formation step, supporting the schematics in (a) and (c), respectively. (e) The calculated electric field by COMSOL around a Si wire shows that the electric field directs holes away from the Si wire when $W_{SCR} > r_{Si\ wire}$ and through the Si wire $W_{SCR} < r_{Si\ wire}$.

To illustrate the importance of the relative width of the SCR to the radius of the Si wires, the electric field around Si wires is simulated using COMSOL Multiphysics™ software (Comsol; Stockholm, Sweden). As shown in Figure 6-2e, when W_{SCR} is greater

than $r_{Si\ wire}$, the electric field directs the holes to flow between the Si wire gap into the solution, not through the Si wires. When W_{SCR} is smaller than $r_{Si\ wire}$, the SCR only exists near the surface of the Si wires and the holes can readily reach to the surface of the Si wires. Experimentally, we vary the ratio of W_{SCR} to $r_{Si\ wire}$ by changing the doping concentration of the parent Si wafer. The W_{SCR} can be estimated from

$$W_{SCR} = \left(\frac{2\varepsilon_r \varepsilon_0 V}{eN_A}\right)^{1/2} \quad 6\text{-}1$$

, where ε_r is the relative dielectric permittivity, ε_0 is the permittivity of vacuum, V is the applied bias, e is the electron charge and N_A is the number of ionized acceptors. When the Si wires are lightly doped with a boron concentration of 10^{14} cm^{-3}, the estimated W_{SCR} is about 3 μm, which is much larger than $r_{Si\ wire}$ (~280 nm). In this case, the Si wire does not show signs of porosity in the transmission electron microscope (TEM) image in Figure 6-2b, taken after the porous Si formation step. On the other hand, when the Si wires are heavily doped with a boron concentration of 10^{19} cm^{-3}, the estimated W_{SCR} is about 10 nm, much smaller than $r_{Si\ wire}$ (~280 nm). In this case, the Si wire is clearly porous after the porous Si formation step, as seen in Figure 6-2d and the inset optical image showing that the Si wires are much darker after the porous Si formation step. Therefore, application of our electro-assisted transfer method requires W_{SCR} to be greater than $r_{Si\ wire}$ to limit the porosity formation inside the Si wires.

6.4. Generality of Electro-assisted Transfer Method

Our electro-assisted transfer method has four key merits. The *first* merit is its generality for transferring Si wire arrays, regardless of their dimensions and the methods by which they are fabricated. The transfer of Si nanowires (diameter: 280 nm, length: 12

μm, spacing: 650 nm) formed by the DRIE method has already been demonstrated in Figure 6-1. Figure 6-3a and 3b show that this transfer method is equally applicable to Si nanowire arrays (diameter: 300 nm, length: 10 μm, spacing: 400 nm) fabricated by the MACE method and Si microwires (diameter: 3μm, length: 18 μm, spacing: 7 μm) formed by the DRIE method. The left SEM images in Figure 6-3a and 3b show the Si wires before the transfer step but after electropolishing (equivalent to Figure 6-1c). The porous Si layer is clearly visible below the Si wire array and has been separated from the parent Si wafer below. The right SEM images in Figure 6-3a and 3b show the Si wires after they are removed from the parent Si wafer and transferred to a receiver substrate. The Si wires look identical to those before the transfer. The porous Si layer can be removed after the transfer step by etching in a 0.03 M KOH solution containing 10% ethanol for 30 minutes. After the porous Si layer removal, the SEM images in Figure 6-3c and d show the remaining Si nanowire arrays formed by MACE and DRIE, respectively. There are still some porous Si strips on the ends of Si nanowires, which is consistent with the simulation results in Figure 6-2e in that a narrow strip of Si right underneath the Si wires is less porous due to the local electrical field. The *second* merit of this transfer method is that the alignment and structure of the Si wires are kept intact by the porous Si layer during the transfer. As such, even patterned Si wire arrays can be transferred with high fidelity. Figure 6-3e that shows a pre-patterned Si nanowire array (number: 15) is transferred to a different Si substrate while maintaining the patterned shape. The *third* merit of the electro-assisted transfer method is that Si wires can be transferred to any substrate, such as stainless steel sheets (Figure 6-3f), as long as the substrates are kept flat during the attachment of the Si wire array. The *fourth* merit is that Si wafers can be

repeatedly used to form vertical Si wire arrays by etching and transferring Si wires to different substrates. Since the electropolishing step creates a new and relatively flat polished Si surface underneath the porous Si layer, it allows new Si wires to be etched on the same parent Si wafer. The recycling ability of the Si wafer is demonstrated in Figure 6-4 by forming Si nanowire arrays by MACE and transferring them five consecutive times. As shown in Figure 6-4a, new Si nanowire arrays can be formed after each transfer, though the uniformity decreases since the freshly exposed Si surface is not perfectly flat after electropolishing. The surface roughness of the Si can be improved by adding an intermediate surface polishing step. Even though there is some global surface roughness, the morphology of the first array of Si nanowires (Figure 6-4b) is similar to that of the fifth wire array (Figure 6-4c), showing the ability to recycle the parent Si wafer.

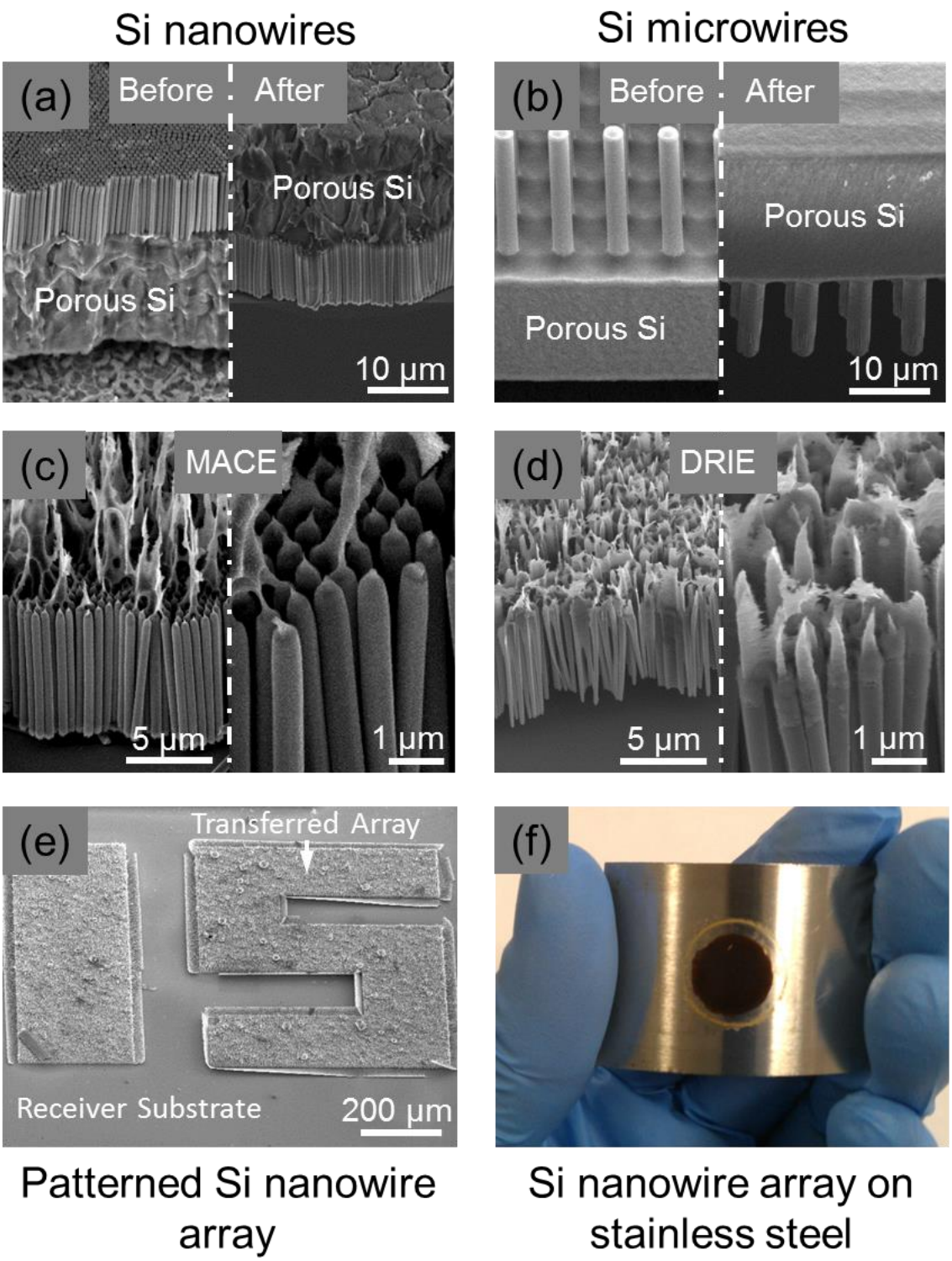


Figure 6-3. Generality of the electro-assisted transfer method in transferring different Si wires to other substrates. SEM images of (a) Si nanowires and (b) Si microwires before

(left images) and after (right images) the electropolishing and transfer step. Low (left images) and high magnification (right images) SEM images of transferred (c) MACE and (d) DRIE Si nanowire arrays after the sacrificial porous Si layer is etched away. (e) SEM image shows that a patterned Si nanowire array (in letter 15) is well preserved after being transferred to a different Si substrate and removal of the porous Si layer. (f) Optical image of a Si nanowire array transferred to a flexible stainless steel sheet.

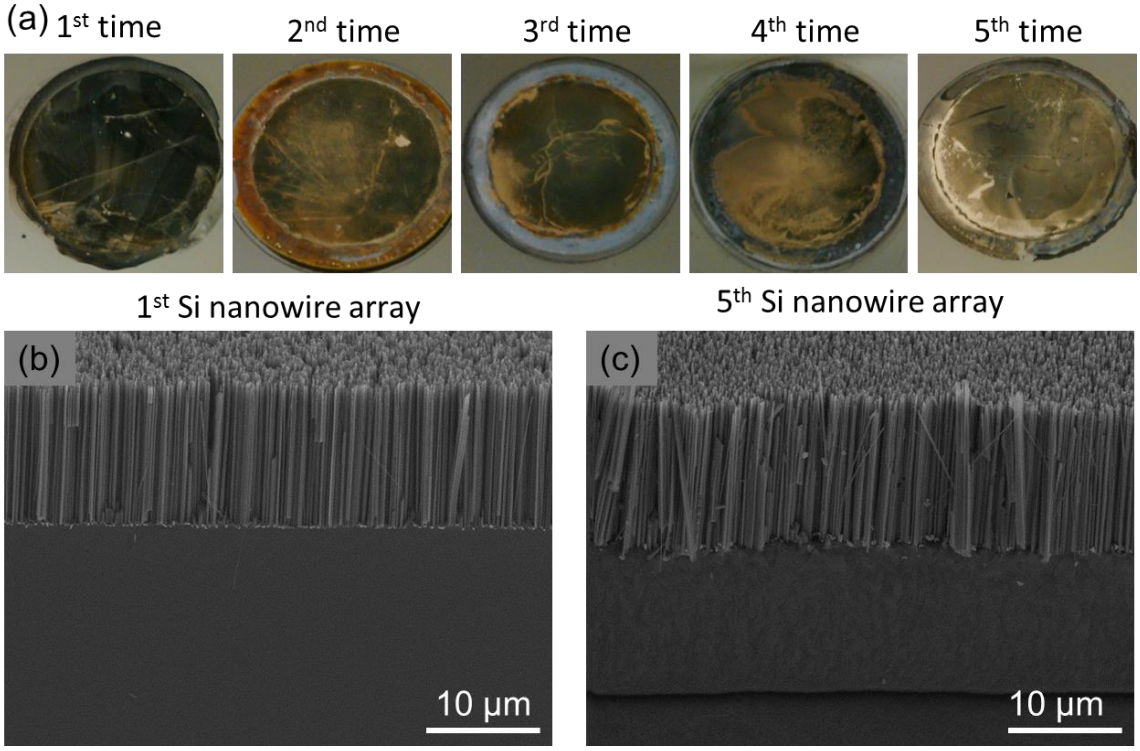


Figure 6-4. Recyclability of the parent Si wafer to form and transfer multiple Si wire arrays from a single substrate. (a) Optical images of five Si nanowire arrays that are consecutively formed by MACE and transferred. SEM images show that Si nanowires of similar morphology are formed by the electro-assisted transfer method before the (b) first and (b) fifth time transfer.

6.5. Fabrication of Electronic Devices

In order to further demonstrate that there is little porosity formation within the Si wires, the electrical conductivity of Si nanowires from the same wafer is measured before and after the porous Si formation process. The Si nanowires (DRIE) are ultrasonicated in IPA to separate from the substrate prior to being drop-casted onto a Si wafer patterned with metal electrodes. Pt metal contacts are deposited on both ends of the Si nanowires and connected to the patterned electrodes using a focused ion beam (FIB). As shown in (Figure 6-5) the Si nanowires have comparable electrical conductivities (within the measurement and sample tolerance) and similar linear current-voltage characteristics.

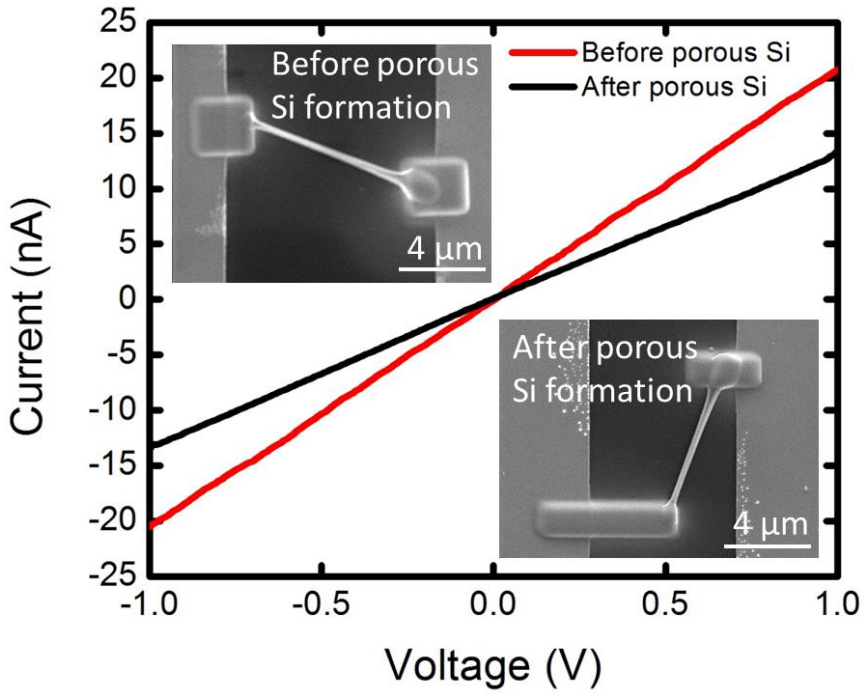


Figure 6-5. Comparison of the electrical conductivity of Si nanowires before (as-etched) and after the porous Si layer is formed underneath the Si nanowire array. In this case, the conductivity of the Si nanowires is lower than the conductivity of the etchant solution, so

the Si nanowires show similar conductivities (~0.02 S/cm), indicating little porosity formation within the Si nanowires.

Device scale electrical characterization (Figure 6-6) is carried out using a similar fabrication method to the one in Chapter 5. Si nanowires are formed and electropolished with a porous Si layer beneath the wires and filled with a polymer. In this case parylene is used instead of PDMS for two main reasons: 1) the porous Si layer is too fragile for a liquid based polymer and 2) the porous Si layer preserved the Si nanowire spacing better than the crack formation method allowing parylene to be used, which is much easier to etch than PDMS. The Si nanowire tips are exposed with oxygen plasma (100 sccm O_2, 150 mTorr, 150 W, estimated etch rate ~35 nm/min) (Figure 6-6a). An SEM image with exposed Si nanowire tips is shown in Figure 6-6f. Then, metal contacts (Ti/Pd: 5/200 nm) are deposited on the exposed SiNW tips with an electron beam evaporator after a brief HF etching to remove the native oxide on the surface (Figure 6-6b). Subsequently, the sample is flipped over and attached to any arbitrary receiver substrate coated with a thin conductive silver epoxy (Ted Pella) layer (~50 μm). Once the silver epoxy is fully cured, the Si substrate is detached from the porous Si layer with the Si nanowires on top, leaving behind the Si nanowire array embedded in parylene topped with the porous Si layer on the receiver substrate (Figure 6-6c). The majority of the porous Si layer is removed in a 0.03 M KOH solution containing 10% ethanol for 30 minutes. The thin parylene layer near the SiNW tips/porous Si interface is removed with oxygen plasma followed by a brief 2% HF etch. The Si nanowire tips are then reactive ion etched (15 sccm SF6, 5 sccm O2, 50 mTorr 100 W) to remove any residual porous layer/parylene composite (Figure 6-6d,g). The other metal contact (Ti/Pd 5/200 nm) is deposited through a shadow

mask with ~300 μm diameter holes (machined from stainless steel) on top of the Si nanowire tips after HF etching to remove the native oxide, completing the vertical Si nanowire array device (Figure 6-6e). Representative linear I-V curves with an average electrical conductivity similar to the single Si nanowire measurements are an order of magnitude higher than our MACE Si nanowire formed via crack formation, demonstrating that our electro-assisted V-TPM forms good quality metal-Si contacts during the device fabrication process and maintains the original Si nanowire properties.

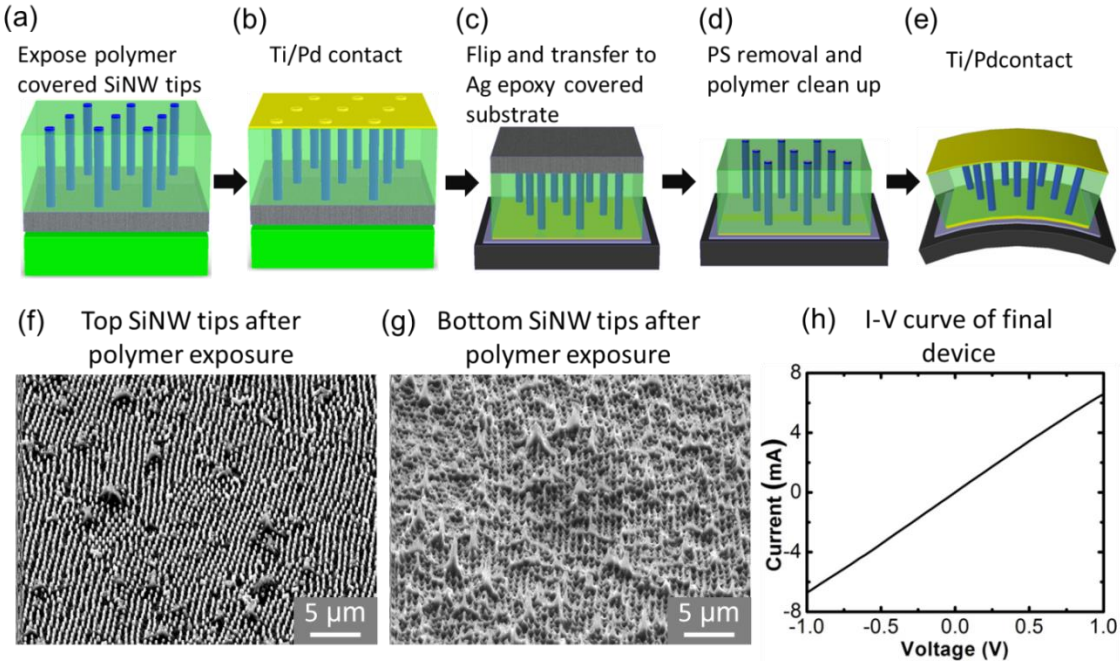


Figure 6-6. Schematic of the fabrication procedure for the electro-assisted transfer for Si nanowire for integration into electrical devices. (a) Porous Si containing Si nanowires (DRIE) are electropolished form a Si wafer, filled with parylene, and etched to expose the Si nanowire tips; (b) metal contact is deposited over the exposed Si nanowire tips after the native oxide it removed; (c) the metal contact on the Si nanowire and attached to silver epoxy as the Si wafer is released from the porous Si layer; (d) the porous Si layer is

removed and the backside of the Si nanowire tips are exposed, (e) the other metal contact is deposited on the exposed SiNW tips over a shadow mask with 300 μm diameter holes to complete the vertical SiNW array device. SEM image of the exposed (f) front and (g) backside Si nanowire tips. (h) Typical linear IV curve demonstrating the Si nanowires maintain the original as formed properties.

6.6. Current-Induced Metal-Assisted Chemical Etching

In our electro-assisted transfer method, the holes are the oxidizing species, and are supplied from inside the parent Si wafer. The local concentration of holes controls the local oxidation rate of the Si and its removal rate in HF. Holes play the same oxidizer role as the H_2O_2 commonly used in the MACE method, so we can replace H_2O_2 in the MACE method with an electrical current (equivalently a flow of holes) to synthesize Si nanowires. To illustrate this, we follow the same preparation steps of the MACE method by first patterning the Ag/Au catalyst on top of a Si wafer. Next, we place the Ag/Au coated Si wafer in a Teflon anodization cell fill with a modified MACE etchant (4.8 M HF solution but without H_2O_2). Then, we pass a current between the Al contact on the back of the Si wafer and a Pt counter electrode immersed in the etchant to supply holes that mimic the role of H_2O_2. The holes move towards the top Ag/Au film (Figure 6-7a), where the Si underneath the Ag/Au is subsequently oxidized and removed by HF, leading to the formation of Si nanowire arrays (Figure 6-7b, etching conditions: 15 mA/cm^2 for 20 minutes). The benefits of using current, instead of H_2O_2, for MACE are most pronounced when synthesizing Si nanowires with 1) long lengths for which the poor transport of H_2O_2 onto Si nanowire surface leads to etching nonuniformity or 2) axially

modulated porosity or zigzag shapes. With conventional MACE, the Si wafer needs to be switched between etchants of different concentrations of H_2O_2 to vary the porosity or control the etching direction [73, 149, 205]. In our current-induced MACE, the Si wafer stays in the same etchant but the applied current is varied to instantaneously control the etching porosity or direction. For example, when the applied current is modulated between 7 mA/cm^2 and 23 mA/cm^2 periodically, the oxidation rates of Si are changed correspondingly, leading to the formation of Si nanowire arrays with axially modulated porosity as highlighted by the SEM and TEM images in Figure 6-7c and d. Specifically, the high current density (23 mA/cm^2) results in porous Si nanowire segments (Figure 6-7d, sections 1 and 3) and the low current density (7 mA/cm^2) results in non-porous/porous core/shell Si nanowire segments (Figure 6-7d, sections 2 and 4).

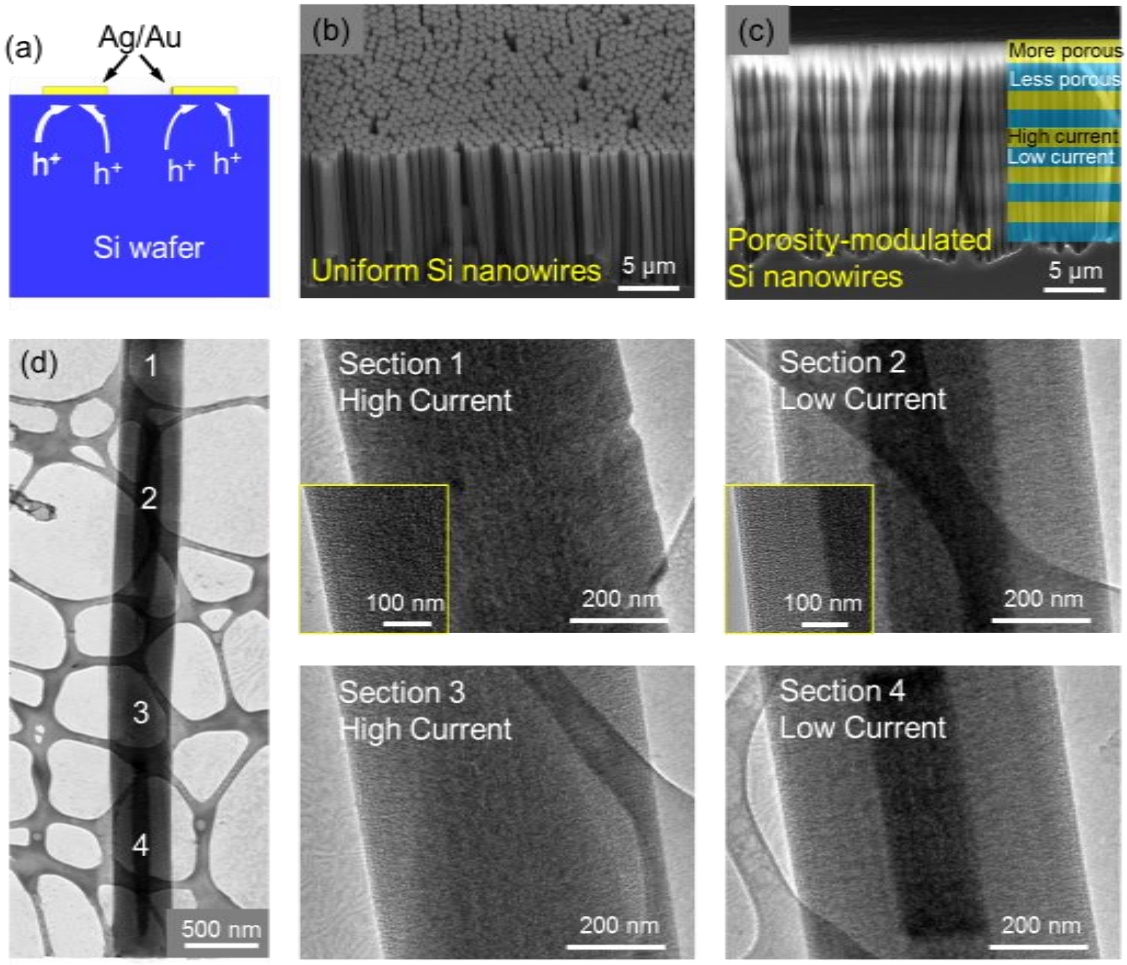


Figure 6-7. Synthesis of Si nanowires by the current-induced MACE for which the oxidizer, H_2O_2 is replaced by an applied current. (a) Schematic shows that the holes within the Si substrate preferentially oxidize Si beneath the patterned Ag/Au catalyst. (b) SEM image of an axial uniform Si nanowire array etched in a 4.8M HF solution with a constant 15 mA/cm^2 applied current. (c) SEM and (d) TEM images of a Si nanowire array with axially modulated porosity etched in a 4.8M HF solution by switching the applied current between 7 and 23 mA/cm^2 periodically in a 4.8 M HF solution. High magnification TEM images show that the high current density (23 mA/cm^2) results in porous Si nanowire segments (center images, sections 1 and 3) and the low current

density (7 mA/cm^2) results in non-porous/porous core/shell Si nanowire segments (right images, sections 2 and 4)

6.7. Section Conclusion

In summary, we have developed a general electro-assisted transfer method for transferring Si wire arrays, regardless of their dimensions and fabrication methods, to any other flat substrates while maintaining their original properties and vertical alignment. This transfer method relies on the formation of a sacrificial porous Si layer underneath the Si wire array. The porous Si layer, together with the Si wire array on top, is subsequently separated from the parent Si wafer by the electropolishing method, and the Si wire array is then be transferred to other substrates. The key to this transfer method is to prevent the formation of porosity in the Si wires by controlling the electric field around the Si wire arrays through the formation of a space-charge region with greater width than the radius of the Si wire. The electrical conductivity of the Si nanowires is maintained in single Si nanowire measurement before and after the porous Si formation and when scaled up to an array measurement. We believe that this new transfer method can be applied to transfer other nanostructures fabricated or deposited on Si wafers as well. Finally, we extend the concept of controlling the oxidation location of Si and develop a current-induced MACE technique. The current-induced MACE technique replaces H_2O_2 with an applied current and allows easy and rapid control of the Si oxidation rate by variation of the current, providing a convenient means by which to form Si nanowires with axially modulated porosity, potentially valuable for thermoelectric devices.

Chapter 7. Conclusion

7.1. Concluding Remarks

Silicon, the second most abundant element on earth with years of research and development, is a promising material for cost-effective thermoelectric devices. Silicon nanostructures have received substantial attention due to the unique and promising material properties and combination of properties not naturally available in bulk silicon. In particular, the ability to independently reduce the lattice component of the thermal conductivity without negatively reducing the electrical conductivity allows SiNWs to be fabricated towards the ideal phonon glass, electron crystal material. However, three major challenges need to be addressed to help bring SiNW arrays towards a practical thermoelectric material: 1) improve the fundamental understanding and fabrication of nanostructured silicon, 2) utilize and understand the effect of various nanostructring methods on the reduction of the lattice component of the thermal conductivity without reducing the electronic conductivity and 3) fabricate highly dense, vertically aligned SiNW array electronic devices on arbitrary substrates to remove the bulk Si substrate effects.

This dissertation focuses on addressing the above three challenges to help realize the potential of SiNW arrays as thermoelectric materials. First, in Chapter 2, a range of top-down fabrication methods are introduced for use in nanostructuring silicon. Using these methods, different structures are fabricated ranging from nano-porous silicon to non-porous and porous SiNWs. A variety of methods are used to pattern and post-

modify Si wires, expanding the possibilities of top-down nanostructured silicon. Chapter 3 utilizes methods discussed in Chapter 2 to characterize the reduction in thermal conductivity of SiNW arrays with external dimensions comparable and smaller than the average bulk Si phonon mean free path ($\lambda_{Si\text{-}bulk}$) and with a range of internal porosities. It was determined that SiNWs with dimensions comparable or larger than $\lambda_{Si\text{-}bulk}$ only saw a reduction in thermal conductivity when internal porosity was introduced. On the other hand, when the SiNW diameter was decreased to below $\lambda_{Si\text{-}bulk,}$ there was a reduction in the thermal conductivity from both the SiNW diameter and the internal porosity. Although, over a two order magnitude reduction in the thermal conductivity was measured, the high porosity of the SiNWs would negate the benefit of the thermal conductivity reduction with a more substantial reduction in the electrical conductivity. The remaining SiNW arrays that had a less substantial reduction in the thermal conductivity had porosities that required electrical characterization to determine if the electrical conductivity is severely reduced. Therefore, a method to measure the electrical conductivity of the SiNW arrays needs to be developed while also removing the poor performing bulk Si wafer.

A method to transfer the SiNW arrays from that of the Si wafer is required since the Si wafer is substantially larger than the SiNWs and would overshadow the unique benefits of the SiNW array properties. However, finding a method to separate and maintain the highly dense, vertically aligned SiNW arrays from the Si wafer poses a challenge due to the strong adhesion between the SiNWs and the Si wafer. Prior methods are based around using shear force to fracture the SiNWs from the base; however, the

SiNW transfer area, density, reproducibility, and quality are limited with these brute force methods. Chapter 4 introduces a new method to chemically weaken the SiNW arrays from the Si wafer by inserting a water soaking step between two consecutive MACE steps. The creation of the chemical crack eliminates the need for large shearing forces and therefore the limitations in transfer area and density while preserving the high degree of vertically alignment and uniform length of the SiNW array. Chapter 5 utilizes the crack formation method introduced in Chapter 4 to develop a new vertical-transfer printing method (V-TPM). With this method, vertical SiNW array electronic devices are fabricated by: 1) removing the SiNW array from the substrate, 2) reattaching the SiNW array to an arbitrary substrate and 3) forming metal contacts on both side of the SiNW array with a polymer layer in between for structural support and electrical characterization. Electrical characterization showed that the MACE SiNW arrays can be tailored to show non-linear I-V curves consistent with porous silicon to linear I-V curves when the porosity was improved. However, even when steps are taken to minimize the SiNW porosity, the electrical conductivity was reduced relative to the original bulk Si wafer value. While the crack-assisted V-TPM is very promising for SiNW array applications, the reduction in the electrical conductivity is too detrimental to the thermoelectric performance to benefit from the reduction in thermal conductivity.

With the crack-assisted V-TPM limited to MACE SiNW arrays, a new V-TPM needs to be developed that is capable of transferring and preserving the SiNW array properties before and after the transfer process independent of method of SiNW array fabrication. Chapter 6 introduces a new electro-assisted V-TPM based around the

formation of a sacrificial porous silicon layer beneath the SiNW array that is subsequently electropolished, allowing the SiNWs to be easily transferred. The electric field within the Si wafer is controlled by depleting the SiNWs of mobile charge carriers during the porous silicon formation process to prevent the SiNWs from becoming porous. Since the transfer process is not linked to the SiNW formation, the SiNW arrays can be fabricated by any method. The SiNW arrays transferred with this method showed comparable electrical conductivity between: 1) a single SiNW before the porous silicon layer is formed, 2) a single SiNW after the porous layer is formed beneath the SiNW and 3) a transferred SiNW array on an arbitrary substrate. In addition, the electrical conductivity was an order of magnitude larger than the SiNW array with minimal porosity demonstrated in Chapter 5 but still lower than bulk Si due to possible contact resistance and surface issues. With optimization, it is believed the electrical conductivity of the SiNW array can match the bulk value; however, the SiNWs also need to show a significant reduction in the thermal conductivity to open up opportunities for future work based on the research in this thesis.

Using the porosity and thermal characterization data in Chapter 3 and a combination of original wafer values, literature values and electrical conductivity data from Chapter 5 and 6, a range of room temperature zT values can be estimated based on the SiNW arrays used in this work (Figure 7-1). In all of the samples, bulk Si Seebeck Coefficient values are used at their corresponding doping concentrations since phonon drag is not expected to have a major role due to 1) nanoscale features significantly contribute to the phonon scattering and 2) temperatures sufficiently high so that electron-

phonon scattering is not the dominate phonon scattering mechanism [16]. The large range of zT values can be contributed to the electrical conductivity values, ranging from the ideal original bulk Si wafer electrical conductivity all the way down to the non-optimized measured electrical conductivity, which may include metal semiconductor nanostructured contact resistances and insufficient porous silicon or polymer removal along the Si nanowire tips. Estimated electrical conductivity values based on similar single SiNW data from the literature is used for a best guess zT value and labeled by the markers, since four-point probe measurements are not easily possible on the array scale samples. [19, 151, 206-208].

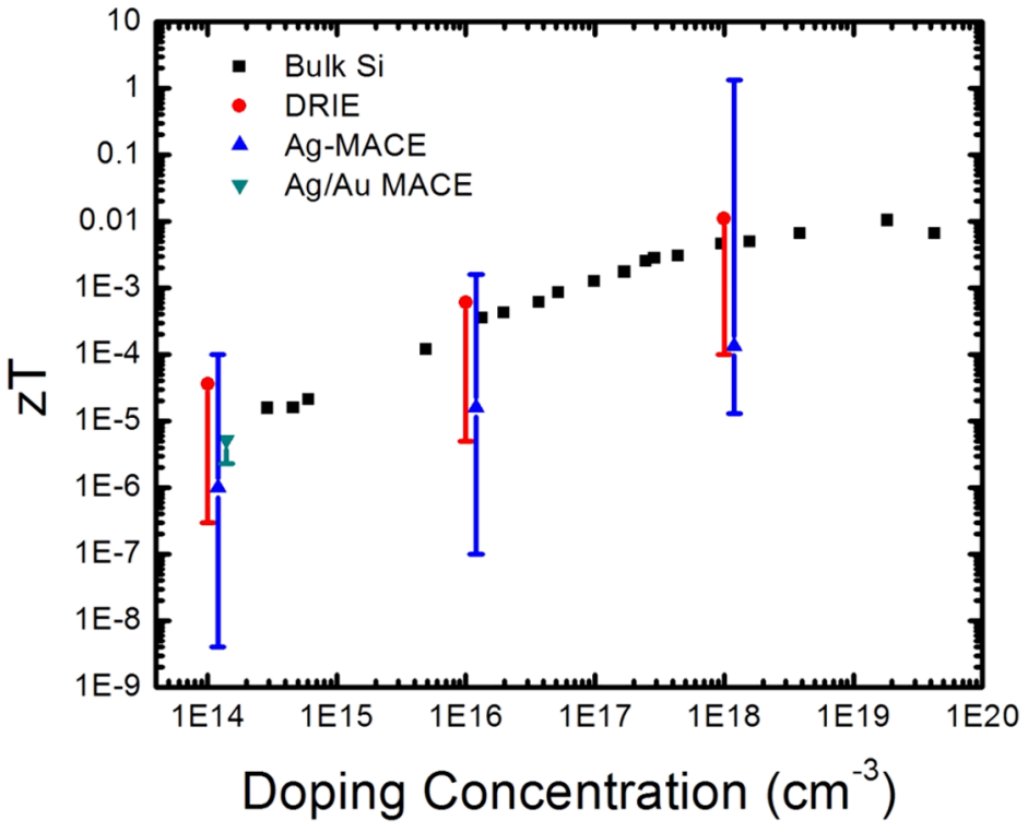


Figure 7-1. Rough estimation of zT values at room temperature based on SiNW arrays characterized in this thesis. The top of the marker error bars correspond to zT values that

assume the SiNW array electrical conductivity is the same as the bulk Si value. The marker within the error bars correspond to estimated electrical conductivity values. The bottom of the marker error bars correspond to zT values that use the SiNW electrical conductivities from electrical data that includes possible contact resistance and surface issues.

7.2. Recommendation for Future Work

7.2.1. Optimization of Electrical Contacts

Forming ohmic electrical metal contacts to semiconductor interfaces has been well researched; however, there is a significant difference between forming contacts to nanostructures and bulk materials due to unique geometries and electrostatics, rendering existing bulk models and techniques not directly applicable to nanostructured materials [209]. Further research is required in order to optimize the metal contacts to nanostructured semiconductors both in terms of the materials and methods [209]. In addition, both of the transfer methods presented in this work rely on the formation of a porous layer at the base of the SiNW array. While the V-TPMs developed in this thesis work very well for transferring Si nanowires, a concern arises that a residual porous Si layer can reside on the SiNW tips and interferes with the electrical contact. Further efforts could be utilized to ensure that all the porosity is removed from the SiNWs, which would minimize the detrimental reduction to the electrical conductivity.

7.2.2. Integrated Electrical and Thermal Conductivity Measurement

Optimization of zT in nanostructured silicon should be approached with a measurement that combines the thermal and electrical conductivity characterization simultaneously instead of performing both individually. The V-TPMs developed in this thesis enable metal contacts to be fabricated on both sides of the SiNW array, opening up opportunities for new characterization methods. Figure 7-2 shows a measurement technique that can measure the electrical conductivity as was done in this thesis but also the thermal conductivity using the 3-ω technique on the same sample [210-212]. The 3-ω method uses electrical joule-heating and thermometry in a metal bridge and parametric fitting of a heat diffusion model to extract the thermal conductivity. Typically, for the 3-ω method, a single heater is patterned on the material of interest and is electrically isolated from the sample to extract thermal properties. By integrating top and bottom electrical contacts into the measurement setup, the electrical and thermal properties can be simultaneously characterized. In addition, the 3-ω technique does not require reflective surfaces, eliminating the fabrication challenge of forming ohmic metal contacts on only partially exposed SiNW tips.

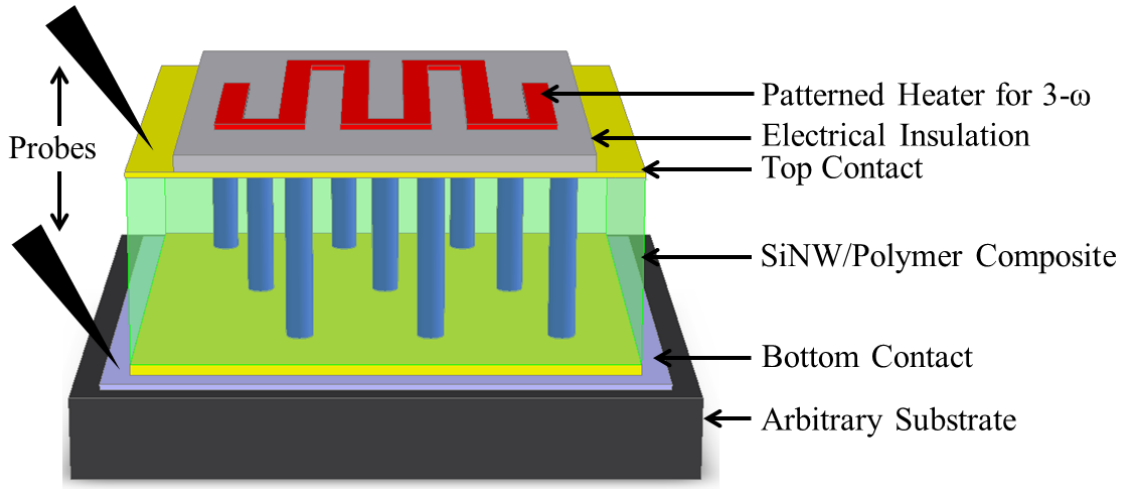


Figure 7-2. Schematic of measurement setup capable of simultaneously measuring the thermal and electrical conductivity. Electrical conductivity is measured through electrical probes on the metals films that are directly in contact with the top and bottom of the SiNW array. The thermal conductivity uses the patterned electrically-isolated heater for the 3-ω method.

7.2.3. Optimization of Nanostructured Silicon

There is a general trend that as the porosity increases with in SiNWs, the thermal conductivity decreases. However, at the same time, introducing porosity can also lead to a decrease in the electrical conductivity, which negates the benefits of porosity for improving zT. A more detailed and quantitative investigation on the porosity would be beneficial to determine the effect of pore size, pore distribution and pore uniformity. Characterization methods such as TEM, Brunauer–Emmett–Teller (BET) and Barrett-Joyner-Halenda (BJH) can be used to more precisely measure the pore location and uniformity, silicon surface area, and pore size and volume, respectively. A promising nanostructured morphology could be a non-porous/pore core/shell structure (Figure 7-3).

The non-porous core could serve as an efficient electron/hole highway for the charge carriers while the porous shell could enhance the phonon scattering. This structure could be fabricated by first forming a non-porous DRIE SiNW array. The porous shell can be formed by placing the SiNWs in an anodization cell with H_2O_2 and HF. A controllable porous shell will form along the SiNWs when a current is applied. Figure 7-3a shows the base of a SiNW array fabricated using this method. The non-porous/pore core/shell SiNW array could then be transferred and integrated for characterization as shown in Figure 7-3b.

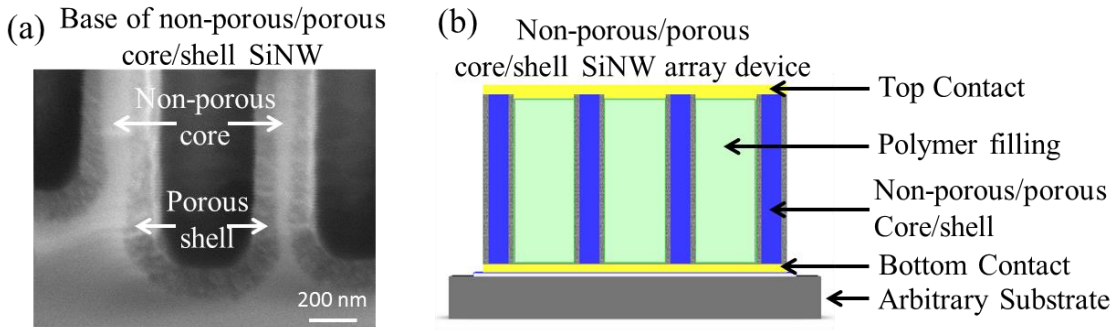


Figure 7-3. Fabrication of non-porous/porous core/shell SiNW arrays. (a) SEM image of DRIE SiNWs with a porous shell formed in a solution containing 4.0 M HF and 3.2 M H_2O_2. (b) Schematic showing a non-porous/porous core/shell SiNW array device.

7.2.4. Fabrication of a Functional Thermoelectric Device and other Relevant Applications

The research and methods developed within this thesis laid the ground work for improving a range of vertical SiNW array based devices. With further improvement and optimization in SiNW arrays as thermoelectric material, the next steps will be to integrate alternating p- and n-type SiNW arrays electrically in series and thermally in parallel

(Figure 7-4a). This configuration will rely on the efficiency from both the p- and n-type arrays and be able to directly produce an electrical output to power a practical device. In addition, alternative filler materials should be investigated that are capable of withstanding high temperatures applications such as oxides or spin-on glass. Although the primary focus of this thesis is on using SiNW arrays as a potential thermoelectric material, the methods developed can be applied to other promising applications such as photovoltaic devices, Li-ion battery anodes, or sensors. Vertical SiNW arrays are promising for photovoltaic devices (Figure 7-4b) due to their superior light trapping and ability to decouple the direction of light absorption from carrier extraction, reducing charge carrier recombination. With the above attributes and the V-TPMs developed within this thesis, SiNW arrays can be transferred from a reusable Si wafer, reducing the high quantity and quality of silicon used, and therefore the cost required in a conventional photovoltaic cell. In addition, silicon is being researched as a potential anode in Li-ion battery (Figure 7-4c) with a theoretical specific capacity of 4200 mAh/g compared to the conventional carbon with only 372 mAh/g [62, 64]. However, during cycling the Si expands to ~400% leading to pulverization. The high surface area to volume ratio of the SiNWs allows the silicon to withstand the large strain without leading to pulverization. The ability to use the V-TPMs allows the SiNW arrays to be removed from the substrate and directly contacted to a current collector, allowing silicon to be used as a promising high capacity anode material that is relative stable during Li-ion cycling. Furthermore, the vertical SiNW array based sensors (Figure 7-4d) have the ability to improve single SiNW based sensor's slow processing times, unreliable results from irreproducible nanowire dimensions and surface chemistry, size dependent noise sources and substrate

effects [49, 50]. Using a periodically porous top electrode will further improve the performance of vertical SiNW array based sensors by increasing the analyte access to the surface of the SiNWs.

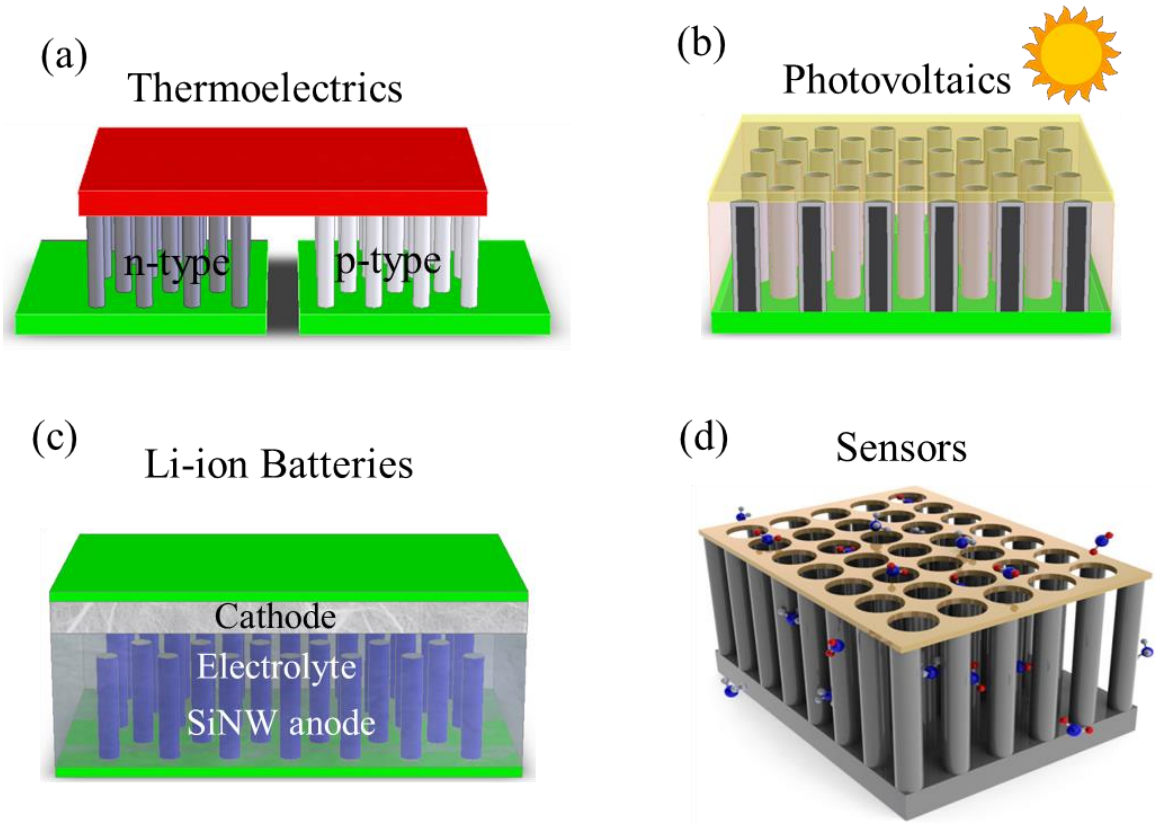


Figure 7-4. Schematic of some potential applications that could be improved with the methods developed within this thesis. (a) Completion of a thermoelectric module consisting of p- and n-type SiNW arrays connected electrically in series and thermally in parallel. (b) Photovoltaic device consisting of radial junction SiNWs that can decouple the direction of light absorption from carrier extraction, allowing photovoltaics to be fabricated with less and lower quality silicon to reduce costs. (c) Li-ion battery anodes manufactured with SiNWs have over 10x improvement in theoretical capacity compared to carbon, while being able to withstand cycling by not leading to pulverization. (d) The

high surface area to volume ratio of vertical SiNW arrays allows biological and chemical sensors to be fabricated that are capable of detecting down to less than 10 parts per billion [49].

Appendix A: Porous Si and Electropolishing Procedures

Porous Si fabrication

Porous Si can be fabricated on p-type Si wafers using the steps below.

1. Deposit an aluminum (Al) layer on the backside of the wafer using e-beam evaporation
    a. 200 nm is typically used in this work
2. Anneal the wafer at 400 °C for 30 minutes to form an ohmic contact between the Al and Si.
3. Attach a piece of conductive tape to the Al coated side of the Si wafer piece.
4. Insert the Al coated Si wafer piece into the anodization cell (Figure 2-1)
5. Fill the anodization cell with an ethanolic HF solution
    a. A 1:1 v/v of 100% ethanol and 48% HF is typically used
6. Insert a platinum (Pt) counter electrode submerged in the ethanolic HF solution and parallel to the Si wafer
7. Connect a sourcemeter to flow a current from the Si working electrode to the Pt counter electrode
8. Apply a constant current to form a porous Si layer at the Si and ethanolic HF interface
    a. 50 mA/cm^2 is typically use for 10^{14} and 10^{16} cm^{-3} wafers
    b. Etch rate is roughly ~0.8 μm/min under these conditions

9. Upon achieving a desired porous Si thickness, remove the Si wafer from the anodization cell and soak in ethanol before critical point drying.

Sides notes:

- The pore size, shape, and density can all be modified by varying the wafer doping type, concentration and orientation, solution composition, applied current and external conditions such as temperature and illumination
- n-type silicon is typically formed using front or backside illumination rather than with a sourcemeter

Electropolishing conditions

The electropolishing conditions can easily be tuned from porous Si formation to electropolishing by either increasing the current density or decreasing the concentration of HF in the solution until the Si oxidation rate exceeds the diffusion of F^- ions to the Si surface. Typical conditions for electropolishing of 10^{14} and 10^{16} cm^{-3} p-type wafers is below.

1. Follow steps 1-4 of the porous Si fabrication procedure
2. Fill the anodization cell with an ethanolic HF solution and insert the Pt counter electrode
    a. A 3:1 v/v of 100% ethanol and 48% HF is typically used
3. Apply a constant current to electropolish the Si at the Si and ethanolic HF interface

a. 50 mA/cm^2 is typically use for 10^{14} and 10^{16} cm^{-3} wafers for 10-30 seconds

4. After electropolishing is completely, remove the Si wafer from the anodization cell and soak in ethanol before critical point drying.

Appendix B: Fabrication Procedure for DRIE Si Microwires and Nanowires

DRIE Microwire Fabrication

Silicon microwires (diameter: 3μm, spacing: 7 μm) are fabricated on 500 μm thick single side polished Si (100) wafer using the procedure below.

1. The Si wafer is first cleaned in the following solutions
    a. Soaking in a 4:1 v/v mixture of sulfuric acid and hydrogen peroxide at 90°C for 10 minutes to remove any organic residue
    b. Soaking in a 5:1:1 v/v/v mixture of water, hydrogen peroxide and hydrochloric acid at 75°C for 10 minutes to remove any metal residues
    c. Soaking in 2% hydrofluoric acid solution for 1 minute to etch any chemically formed oxides from the above solutions
2. A micrometer of SPR3612 photoresist was spin coated on the wafer and backed at 90°C for 1 minute
3. The photoresist is exposed for 1.4 second using a vacuum contact mask aligner to a chrome mask
4. The photoresist is post baked at 100°C for 1 minute followed by being developed
5. Vertically aligned silicon microwires are formed using DRIE with cycles of 6 second etching with 130 sccm of SF_6 and 5 second passivation with 120 sccm of C_4F_8 and a 600 W plasma power for ~14 minutes for 10 μm long wires

6. After etching the Si wafer containing the microwire, all the by-product polymers from the etching process are removed by the following process
    a. Soaking in a 4:1 v/v mixture of sulfuric acid and hydrogen peroxide at 90°C for 10 minutes
    b. Etching in oxygen plasma with 100 sccm O_2, 150 mTorr pressure and 500 W plasma power
    c. Soaking in 2% hydrofluoric acid for 1 minute to remove any oxides from the above steps

DRIE Nanowire Fabrication

Silicon nanowire (diameter: 280-350 nm, spacing: 650 nm) are fabricated on 500 μm thick single side polished Si (100) wafer using a similar procedure which is described below.

1. The Si wafer are first cleaned using the same procedure as the microwires
2. The Si wafer is exposed to oxygen plasma (80W) for 5 minutes to clean the surface
3. The Langmuir Blodgett method is use to deposit a monolayer ~650 nm silica spheres
4. The silica spheres are reduced in diameter to ~500 nm to create a non-closed packed monolayer with 6 sccm 02, 85 sccm CHF3, 50 mTorr chamber pressure and 1200 W plasma power

5. Vertically aligned Si nanowires are formed using the same DRIE etching process as a the Si microwires but due to the reduction of the silica sphere masking layer the resulting Si nanowire are around 280 nm
6. The Si nanowire are cleaned from any by-product polymers by the same method as the microwiresAfter etching the Si wafer containing the microwire, all the by-product polymers from the etching process are removed by the following process
    a. Soaking in a 4:1 v/v mixture of sulfuric acid and hydrogen peroxide at 90°C for 10 minutes
    b. Etching in oxygen plasma with 100 sccm O_2, 150 mTorr pressure and 85 W plasma power
    c. Soaking in 2% hydrofluoric acid for 1 minute to remove any oxides from the above steps

Appendix C: General Fabrication Recipe used to synthesis 650 nm spheres

1. Synthesis of nanoparticles
    a. Create the following solutions in a 45mL plastic vial
        i. Vial #1 = 1.3mL TEOS + 5mL 200proof Ethanol + small stir bar
        ii. Vial #2 = 15mL 200proof Ethanol + 7mL 30% Ammonium Hydroxide(fume hood)
    b. Preset magnetic spinner to 500-600rpm
    c. Pour Vial #2 into Vial #1 and mix for 1 hour at room temperature in fume hood (notice the color change)
    d. After the 1 hour, remove stir bar from solution and sonicate on high power for 10 min
2. Cleaning of unfunctionalized Nanoparticles
    a. Cleaning step 1
        i. Pour in regular ethanol until vial is at 40mL
        ii. Sonicate at high power to make homogenous solution
        iii. Place in centrifuge (don't forget counter balance)
        iv. Spin at 3500rpm for 15min
        v. Remove from centrifuge and notice that the particles have settled to the bottom
        vi. Pour out clear liquid leaving only the particles behind
    b. Cleaning Step 2 – repeat cleaning step 1

c. Cleaning Step 3 – repeat cleaning step 1
d. Cleaning Step 4
    i. Pour in DI water until vial is at 40mL
    ii. Sonicate at high power to make homogenous solution
    iii. Place in centrifuge (don't forget counter balance)
    iv. Spin at 3500rpm for 15min
    v. Remove from centrifuge and notice that the particles have settled to the bottom
    vi. Pour out clear liquid leaving only the particles behind
e. Cleaning Step 5 – repeat cleaning step 4
f. Cleaning Step 6
    i. Pour in regular ethanol until vial is at 40mL
    ii. Sonicate at high power to make homogenous solution
    iii. Place in centrifuge (don't forget counter balance)
    iv. Spin at 3500rpm for 15min
    v. Remove from centrifuge and notice that the particles have settled to the bottom
    vi. Pour out clear liquid leaving only the particles behind
g. Fill vial with Ethanol until vial is up to 40mL
h. Sonicate at high power to make homogenous solution
i. Store in refrigerator until ready to functionalize

Appendix D: Functionalization of Silica Spheres with APTES

1. Functionalization of Nanospheres
    a. Do this step the night before the spheres are ready to be used
    b. In a small glass vial add
        i. 2mL of particles from vial stored in refrigerator
        ii. 15mL of 200 proof ethanol
        iii. 0.75mL of DI water
    c. Place glass vial on hot/stir plate at 600rpm and room temperature in fume hood
    d. Add 100uL of APDES (amount proportional to surface area)
    e. Cap glass vial and let stir on stir plate for 12 hours (up to 16 hours is ok) at room temperature and 600rpm
    f. After 12 hours increase temperature to 100deg C and open cap and cover with Al foil to keep isothermal
    g. Leave for 1 hour
    h. After 1 hour turn off heat but keep mixing till solution is cooled
    i. Remove from hot/spin plate and pour into a new 45mL plastic vial
2. Cleaning of functionalized Nanoparticles
    a. Cleaning step 1
        i. Pour in regular ethanol until vial is at 40mL
        ii. Sonicate at high power to make homogenous solution

iii. Place in centrifuge (don't forget counter balance)

iv. Spin at 6000rpm for 15min

v. Remove from centrifuge and notice that the particles have settled to the bottom

vi. Pour out clear liquid leaving only the particles behind

b. Cleaning Step 2 – repeat cleaning step 1

c. Cleaning Step 3

i. Pour in Methanol until vial is at 40mL

ii. Sonicate at high power to make homogenous solution

iii. Place in centrifuge (don't forget counter balance)

iv. Spin at 6000rpm for 15min

v. Remove from centrifuge and notice that the particles have settled to the bottom

vi. Pour out clear liquid leaving only the particles behind

d. Cleaning Step 4 – repeat cleaning step 4

e. Fill vial with 5mL of methanol

f. Sonicate at high power to make homogenous solution

g. Spheres are now ready to be used for LB method

Appendix E: Fabrication of SiNWs with Varied Diameter and Porosity

Non-porous DRIE SiNWs patterned with nanosphere lithography

See Appendix B for detailed fabrication procedures. The etch time is 15 minutes for all wafer doping levels.

MACE SiNWs patterned with nanosphere lithography

1. Clean the Si wafer in the following solutions
    a. Soak in a 4:1 v/v mixture of sulfuric acid and hydrogen peroxide at 90°C for 10 minutes to remove any organic residue
    b. Soak in a 5:1:1 v/v/v mixture of water, hydrogen peroxide and hydrochloric acid at 75°C for 10 minutes to remove any metal residues
    c. Soak in 2% hydrofluoric acid solution for 1 minute to etch any chemically formed oxides from the above solutions
2. Clean and active the Si wafer surface with oxygen plasma (80W) for 5 minutes
3. Deposit a monolayer of ~350-400 nm silica spheres functionalized with APTES using the Langmuir Blodgett method
4. Reduce the silica spheres diameter to ~300 nm with 6 sccm 02, 85 sccm CHF3, 50 mTorr chamber pressure and 1200 W plasma power for 3 minutes to create a non-closed packed monolayer (SNF's AMT etcher – program 3)

5. Remove any polymer by-products from the AMT etcher and oxidize the Si wafer with an O_2 plasma with 100 sccm O2, 150 mTorr chamber pressure 500 W plasma power for 3 minutes (SNF's Drytec 2 – Program 1). Note: This step is performed as close as possible to step 6
6. Deposit MACE metal catalyst using an e-beam evaporator (SNF's Innotec)
    a. Ag/Au MACE samples – deposit 15 nm of Ag at a rate of 0.5 A/sec followed by 5 nm of Au at a rate of 0.5A/sec
    b. Ag MACE samples – deposit 50nm of Ag at a rate of 0.5 A/sec
7. Store wafers in a dehumidifier until the wafers are ready to be etched
8. Remove the silica spheres by sonicating on high power in IPA until the majority of the spheres are removed (verify with an optical microscope)
    a. Residual spheres coated with metal will result in the metal being deposited in unwanted locations
9. Carefully place the metal coated Si wafer in a 2% HF solution for 1 minute to improve the direct Ag/Si adhesion. Do this step immediate before step 10
10. Carefully transport the samples directly from the 2% HF solution to a MACE solution composed of 4.8 M HF and 0.3 M H_2O_2 (typically 250 mL total volume) to etch the SiNWs at room temperature
    a. Approximate etch rates in the above solution
        i. 50 nm Ag, 10-20 Ω*cm = ~0.5 μm/min
        ii. 15/5 nm Ag/Au, 10-20 Ω*cm = ~0.5 μm/min
        iii. 15/5 nm Ag/Au, 0.1-0.9 Ω*cm = ~0.5 μm/min
        iv. 15/5 nm Ag/Au, 0.001-0.005 Ω*cm = 0.3 μm/min

11. After MACE etching, rinse the sample in DI water
12. Remove the metal layer by soaking at a 3:1 v/v solution of hydrochloric acid and nitric acid at 70°C for 10 minutes
13. Rinse the sample in DI water
14. Soak the sample in ethanol for 15 minutes or more
15. Critical point dry the samples after ethanol soaking to prevent agglomeration

MACE SiNWs patterned with silver salts

1. Clean a bare Si piece with acetone, methanol and IPA
2. Place sample in a 4:1 v/v mixture of sulfuric acid and hydrogen peroxide for 10 minutes
3. Place sample in a 2% hydrofluoric acid solution for 1 minute to etch any oxide on the Si surface
4. Bring sample straight from previous solution to a solution containing 4.8M HF and 0.002 M silver nitrate ($AgNO_3$). Gently hand mix for 45 seconds. This will deposit a porous Ag film on the sample
5. Thoroughly rinse the sample with DI water to remove any residual $AgNO_3$ on the surface
6. Place the sample in the MACE etching solution containing 4.8 M hydrofluoric acid and hydrogen peroxide H_2O_2 at room temperature
    a. Approximate etch rates in the above solution of a 10-20 Ω*cm p-type wafer as a function of H_2O_2 concentration

i. 0.15M H_2O_2 = ~0.2 μm/min

ii. 0.3M H_2O_2 = ~0.5 μm/min

iii. 0.6M H_2O_2 = ~0.7 μm/min

iv. 1.2M H_2O_2 = ~0.9 μm/min

7. After MACE etching, rinse the sample in DI water
8. Remove the metal layer by soaking at a 3:1 v/v solution of hydrochloric acid and nitric acid at 70°C for 10 minutes
9. Rinse the sample in DI water
10. Soak the sample in ethanol for 15 minutes or more
11. Critical point dry the samples after ethanol soaking to prevent agglomeration

Appendix F: Error Analysis for the Vertical SiNW Array Thermal Conductivity

The details of the thermal conductivity data presented in Chapter 3, including the description and error analysis for each data point, are presented below.

- k_{SiNW} is the thermal conductive of the SiNW array and calculated using the equation below

$$k_{SiNW} = \frac{k_{film} - (1 - VF)k_{pary}}{VF} \quad \text{F-1}$$

- k_{film} is the measured thermal conductive of the SiNW/parylene composite determined by the solution of the heat diffusion equation from the nanosecond transient thermoreflectance data
- VF is the SiNW array volume fraction determined by using top-view SEM images and the Matlab code found in Appendix G
- $k_{\_ary}$ is the parylene thermal conductivity literature value
- Δk_{film} is the measured spot to spot variation in the film thermal conductivity across a sample. Note, this was larger than the error from the noise in the measurement
- ΔVF is the estimated error in the calculated Matlab value based on varying the grey threshold value of over 5 SEM image taken at different locations on each sample.
- Δk_{pary} is the variation in the parylene thermal conductivity literature value

Figure Chapt 3-	k_{SiNW} [W/m/K]	k_{film} [W/m/K]	VF [-]	k_{pary} [W/m/K]	Δk_{film} [W/m/K]	ΔVF [-]	Δk_{pary} [W/m/K]
2, 3	142.5	31.4	0.22	0.12	2.9	0.01	0.05
2	98.0	44.0	0.45	0.12	5.0	0.02	0.05
2, 3, 4	51.3	27.0	0.53	0.12	2.2	0.02	0.05
3	131.5	29.0	0.22	0.12	1.2	0.01	0.05
3	123.4	27.3	0.22	0.12	1.1	0.01	0.05
3	49.3	25.7	0.52	0.12	7.4	0.02	0.05
3	1.02	0.67	0.60	0.12	0.12	0.02	0.05
4	37.9	16.7	0.44	0.12	0.34	0.04	0.05
4	27.6	13.1	0.47	0.12	2.4	0.04	0.05
4	23.2	9.5	0.41	0.12	0.93	0.04	0.05
4	16.8	8.2	0.48	0.12	0.81	0.04	0.05

Table 3. Values and tolerances of the measured film thermal conductivity, volume fraction, and literature value for the parylene thermal conductivity

An error propagation analysis is used to determine the overall error of the measured thermal conductivity as shown below.

$$\Delta k_{SiNW} = \sqrt{\left(A\left(\Delta k_{film}\right)\right)^2 + \left(B(\Delta VF)\right)^2 + \left(C\left(\Delta k_{pary}\right)\right)^2} \quad \text{F-2}$$

$$A\left(\Delta k_{film}\right) = \frac{\partial k_{SiNW}}{\partial k_{film}} \Delta k_{film} = \left(\frac{1}{VF}\right) \Delta k_{film} \quad \text{F-3}$$

$$B(\Delta VF) = \frac{\partial k_{SiNW}}{\partial VF} \Delta VF = \left(\frac{k_{pary} - k_{film}}{VF^2}\right) \Delta VF \quad \text{F-4}$$

$$C\left(\Delta k_{pary}\right) = \frac{\partial k_{SiNW}}{\partial k_{pary}} \Delta k_{pary} = \left(\frac{1}{VF} - 1\right) \Delta k_{pary} \quad \text{F-5}$$

Figure Chapt 3-	**k_{SiNW} [W/m/K]**	**$A(\Delta k_{film})$ [W/m/K]**	**B(ΔVF) [-]**	**$C(\Delta k_{pary})$ [W/m/K]**	**Error [W/m/K]**
2, 3	142.5	13.2	-6.5	0.18	14.7
2	98.0	11.1	-4.3	0.06	11.9
2, 3, 4	51.3	4.2	-1.9	0.04	4.6
3	131.5	5.6	-6.0	0.18	8.2
3	123.4	5.0	-5.6	0.18	7.5
3	49.3	14.3	-1.9	0.05	14.4
3	1.02	0.20	-0.03	0.03	0.21
4	37.9	0.77	-3.0	0.06	3.1
4	27.6	5.19	-2.1	0.06	5.6
4	23.2	2.27	-2.0	0.07	3.0
4	16.8	1.69	-1.2	0.05	2.09

Table 4. Error propagation analysis used to determine the overall error in the SiNW thermal conductivity values

Appendix G: Matlab Code use to Determine to SiNW Volume Fraction

```
clc
clear all

path1 = 'C:\Users\Jeff\Research040713\SEM images\Jan 2013\';
filename1 = '15jan13 - L1 top  3.tif';
I = imread(char([path1 filename1]));


I = I(1:485,15:end); %remove blurred edge, stats at bottom
figure(1), subplot(1,2,1)
imshow(I),hold all


level = graythresh(I)-0.0; % Adjust level to get best edge finding
I = im2bw(I,level);
J = ones(size(I));
ff = bwarea(I)/sum(sum(J));      %bwarea estimates the area of the objects in binary image
disp(['Fill Fraction: ',num2str(ff)]);


subplot(1,2,2)
imshow(I)
```

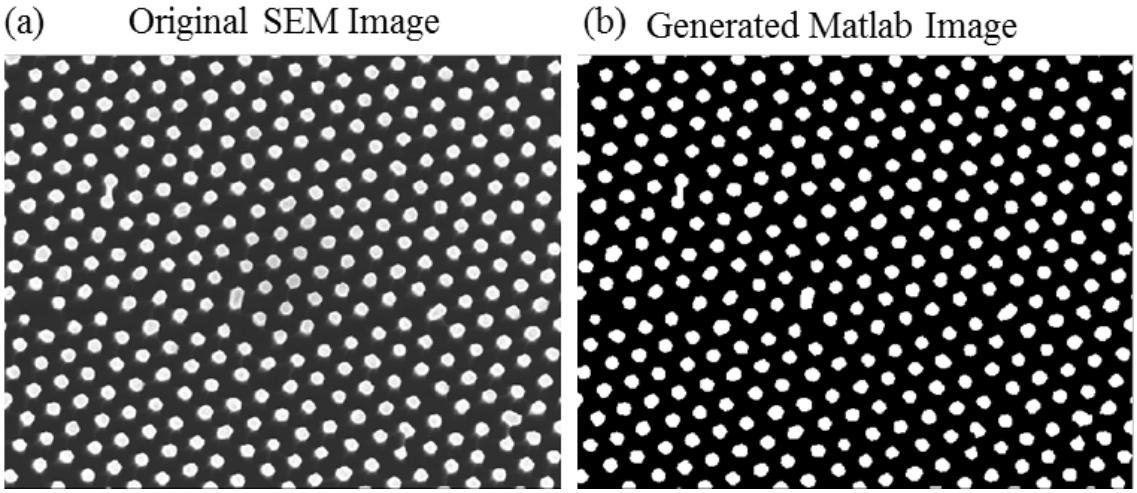


Figure G-1. Example of (a) an SEM image that is converted to (b) a Matlab generated black and white image used for determining the volume fraction.

Appendix H: Error Analysis of the Vertical SiNW Array Porosity

The details of the porosity data presented in Chapter 3, including the description and error analysis for each data point, are presented below.

- $Mass_B$ is average mass of 3 measurements of a Si wafer piece patterned with the respective metal film and with the spheres removed (0.01mg resolution)
- $Mass_A$ is average mass of 3 measurements of a Si wafer piece after the SiNWs are formed but before the metal catalyst is removed. (0.01mg resolution)
- ΔMass is the mass of etched Si and ($Mass_A$ - $Mass_B$)
- VF is the average volume fraction measured using top-view SEM images and the Matlab code found in Appendix G
- Thickness is the length of the SiNWs and determined with cross-sectional SEM images
- Length is the length of the Si wafer piece and measured with vernier caliper
- Width is the length of the Si wafer piece and measured with vernier caliper
- Volume is the of etched area (includes SiNW volume) (Thickness x Length x Width)
- $Mass_{Act}$ is the actual mass of remaining SiNWs (Volume x $density_{Si}$ – ΔMass)
- $Mass_{Ideal}$ is the theoretical mass of solid SiNWs (Volume x VF x density)
- Porosity is the determined by the ratio of actual mass to the theroritical mass of solid SiNWs ((1- $Mass_{Act}$/ $Mass_{Ideal}$) x 100%)

- $Porosity_{Avg}$ is the average porosity value of the two identically fabricated sample

Wafer	Au/Ag-MACE 10^{14} cm^{-3}		Ag-MACE 10^{14} cm^{-3}		Ag-MACE 10^{16} cm^{-3}		Ag-MACE 10^{19} cm^{-3}	
Sample #	1	2	1	2	1	2	1	2
$Mass_B$ [mg]	468.25	443.02	781.10	549.52	624.33	595.47	493.31	417.47
$Mass_A$ [mg]	463.25	438.25	771.15	542.76	619.23	590.62	485.56	411.34
ΔMass [mg]	5.00	4.77	9.95	6.76	5.10	4.85	7.75	6.13
VF [-]	0.4742	0.5053	0.6262	0.6101	0.8155	0.8169	0.5005	0.4954
Thickness [μm]	10.45	10.36	13.65	12.81	13.25	13.2	9.35	8.72
Length [mm]	23.6	22.22	28.47	22.16	24.55	24.57	25.77	21.8
Width [mm]	16.61	16.65	22.06	20.45	20.96	20.13	15.89	15.89
Volume [mm^3]	4.10	3.83	8.57	5.81	6.82	6.53	3.83	3.02
$Mass_{Act}$ [mg]	4.540	4.152	10.016	6.760	10.779	10.360	1.167	0.900
$Mass_{Ideal}$ [mg]	4.524	4.511	12.502	8.248	12.949	12.422	4.463	3.485
Porosity [%]	-0.37	7.96	19.88	18.04	16.75	16.60	73.85	74.18
$Porosity_{Avg}$ [%]	3.8		19.0		16.7		74.0	

Table 5. Measured values and calculated porosity of SiNW used for thermal characterization

The value and calculations below are used to calculate the estimated error in the SiNW porosity using an error propagation analysis.

$\delta Mass_B$ [mg]	$\delta Mass_A$ [mg]	δVF [-]	δThickness [μm]	δLength [mm]	δWidth [mm]
0.1	0.1	0.15	0.25	0.1	0.1

Table 6. Fixed estimated error values for measured values used to determine SiNW array porosity

A propagation error analysis is carried out in order to determine the overall error the porosity of the SiNWs using the gravimetric method

$$\boldsymbol{\partial \Delta Mass} = \sqrt{(\boldsymbol{\partial Mass_B})^2 + (\boldsymbol{\partial Mass_A})^2} \quad \text{H-1}$$

$$\boldsymbol{\partial} Volume = \sqrt{(T \cdot L \cdot \partial W)^2 + (T \cdot W \cdot \partial L)^2 + (L \cdot W \cdot \partial T)^2} \quad \text{H-2}$$

$$\partial Mass_{Act} = \sqrt{(\rho \cdot \partial Volume)^2 + (\partial \Delta Mass)^2} \quad \text{H-3}$$

$$\partial Mass_{Ideal} = \sqrt{(Volume \cdot \rho \cdot \partial VF)^2 + (VF \cdot \rho \cdot \partial Volume)^2} \quad \text{H-4}$$

$$\boldsymbol{\partial Porosity} = \sqrt{\left(\frac{\boldsymbol{\partial Mass_{Act}}}{\boldsymbol{Mass_{Ideal}}}\right)^2 + \left(\frac{\boldsymbol{Mass_{Act} \cdot \partial Mass_{Ideal}}}{\boldsymbol{Mass_{Ideal}^2}}\right)^2} \quad \text{H-5}$$

Where T is the thickness, L is the length, W is the width and ρ is the density of silicon (2.329 mg/mm^3)

Wafer	Au/Ag-MACE 10^{14} cm^{-3}		Ag-MACE 10^{14} cm^{-3}		Ag-MACE 10^{16} cm^{-3}		Ag-MACE 10^{19} cm^{-3}	
Sample #	1	2	1	2	1	2	1	2
δΔMass [mg]	0.141	0.141	0.141	0.141	0.141	0.141	0.141	0.141
δVolume [mm^3]	0.103	0.097	0.165	0.120	0.136	0.131	0.106	0.090
$\delta\Delta Mass_{Act}$ [mg]	0.278	0.266	0.408	0.313	0.346	0.335	0.285	0.252
$\delta\Delta Mass_{Ideal}$ [mg]	0.490	0.461	3.005	2.035	2.396	2.294	0.463	0.367
δPorosity [%]	12.49	11.10	19.53	20.58	15.63	15.64	6.94	7.73
$\delta Porosity_{Avg}$ [%]	11.8		20.1		15.6		7.3	

Table 7. Error propagation analysis used to determine the overall uncertainty in the SiNW porosity values

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