THERMAL PHENOMENA IN PHASE CHANGE MEMORY

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John Reifenberg
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I certify that I have read this dissertation and that, in my opinion, it is fully adequate in scope and quality as a dissertation for the degree of Doctor of Philosophy.

Kenneth Goodson, Primary Adviser

I certify that I have read this dissertation and that, in my opinion, it is fully adequate in scope and quality as a dissertation for the degree of Doctor of Philosophy.

Philip Wong

I certify that I have read this dissertation and that, in my opinion, it is fully adequate in scope and quality as a dissertation for the degree of Doctor of Philosophy.

Mehdi Asheghi

Approved for the Stanford University Committee on Graduate Studies.

Patricia J. Gumport, Vice Provost Graduate Education

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Abstract

Information storage and accessibility form the foundation of many modern electronic systems. High speed nonvolatile memory (NVM) technologies retain data without consuming power, driving the rapid growth of the portable consumer electronics market. However, current technologies face significant challenges in meeting the continuously increasing demand for faster, higher density data storage. Phase change memory (PCM) is an emerging NVM offering exceptional speed, storage density, and cycling endurance. During programming, nanoscale PCM cells experience unprecedented thermal conditions: temperature transients of $\sim 10^{11}$°C/s, temperature excursions greater than 600 °C, and heat generation densities of $\sim 10^{18}$ W/m^3. Understanding thermal transport in PCM is essential for reducing programming current, improving reliability, and optimizing scaling. This work uses novel multiphysics models to quantify the importance of thermal phenomena in PCM. It extends optical thermometry techniques to resolve the thermal transport physics critical for device functionality.

Fully coupled finite element calculations capture the electrothermal and phase change processes in a confined cell device. The simulations demonstrate the critical role thermal boundary resistance (TBR) plays in reducing programming current. This result suggests that interface engineering can significantly reduce programming current. Compact electrothermal models use reduced cell geometries to accurately predict scaling in a variety of device geometries. These models demonstrate that the distribution of thermal resistances is the key design parameter for reducing the programming current.

Nanosecond transient thermoreflectance (TTR) measurements on a variety of chalcogenide stoichiometries show that the effective thermal conductivity depends primarily on

the material phase. This work extends nanosecond TTR up to 340 °C to measure the thickness and temperature dependent effective thermal conductivity of $Ge_2Sb_2Te_5$ (GST) in the as-deposited, fcc, and hcp phases. Process dependent material defects, partial crystallization, and TBR all significantly alter the effective thermal conductivity. Picosecond time-domain thermoreflectance (TDTR) measurements establish the Al/TiN TBR, TiN/fcc GST TBR, and intrinsic fcc GST thermal conductivity up to 325 °C. An original multi-sample, thickness-implicit data extraction technique uniquely separates the spatial distribution of thermal properties. The intrinsic conductivity increases slowly with temperature, consistent with materials with high defect and vacancy concentrations. The TiN/fcc GST TBR dominates the device thermal resistance and is the key factor determining the programming current.

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Contents

List of Tables

List of Figures

Chapter 1

Introduction

Interest in the fundamental study of chalcogenide phase change materials has accelerated over the past decade due to their application in high-density optical recording [1, 2], phase change memory (PCM) devices [3, 4], and, more recently, in thermoelectric power generation and cooling (TPG&C) technology [5, 6, 7]. Figure 1.1 [8] shows the number of papers studying chalcogenides for data storage has doubled every 6-7 years during this time span. PCM devices rely on complex interactions between temperature and electrical fields, which couple strongly to crystallization, and possibly species diffusion [9] processes. The complexity of high-density PC optical recording technology is comparable to PCM due to challenges associated with sub-diffraction optical writing and read-back. PC materials in high-density data storage applications undergo millions of temperature cycles of unprecedented magnitude, $\Delta T \sim 600$ °C, where temporal and spatial temperature gradients of $\sim 10^9$ °C/s and $\sim 10^3$ °C/nm prevail. The importance of PC thermal properties in the operation, reliability, and scaling of high-density data storage devices explains the growing interest in their study seen in fig. 1.1.

Though recent progress has been rapid, the physical principles behind PCM and the first devices using these principles are over 40 years old [10, 11, 12, 13]. In PCM devices, a chalcogenide thin film switches reversibly between the bi-stable polycrystalline (set, low-resistivity) and amorphous (reset, high-resistivity) states, shown in fig. 1.2 [14]. Joule heating, caused by a controlled current pulse, induces structural changes between

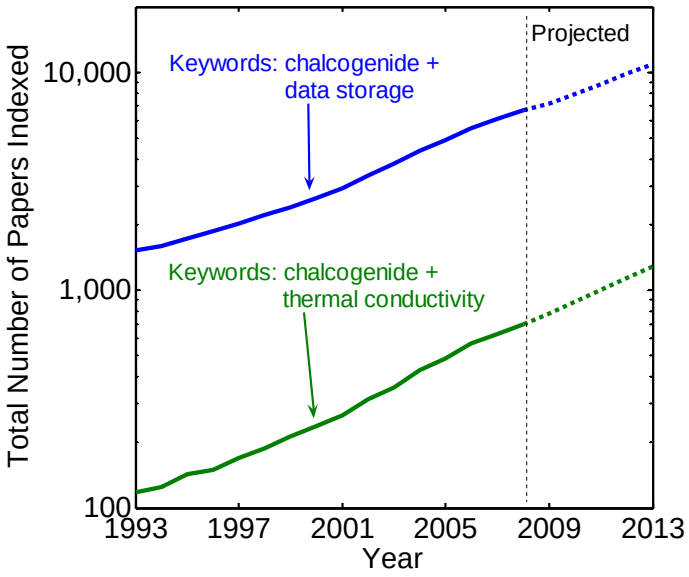

Figure 1.1: Interest in chalcogenides for data storage and their thermal properties, measured by number of papers indexed by Google [scholar.google.com accessed 8/17/09], has grown almost exponentially over the past 15 years.

phases. Rapid melting (T > 600 °C) and quenching of the crystalline phase change material at $\sim 10^{10}$ °C/s freezes it into the glass-like amorphous phase. Sustained heating above the glass temperature, ~300 °C, causes the amorphous phase to transition back to the crystalline phase. Figure schematically depicts the temperature history during programming. Threshold switching, the process whereby an amorphous semiconductor switches into a low-resistivity state in the presence of a large electric field [11], permits the amorphous to crystalline transition to occur at similar voltages as the crystalline to amorphous transition. The heating and quenching process can occur up to 10^{10}-10^{12} times [15].

A functional phase change memory array of 128 Mb (90nm node) has been demonstrated [16]. Favorable scaling is often cited [3] as one of the key advantages of PCM over other nonvolatile memory (NVM) technologies, and it is suggested that PCM may be scalable well beyond the 50 nm node [4, 17]. There have been numerous efforts to discover novel cost-effective methods for fabrication in the sub-50 nm regime to overcome the difficulties associated with the e-beam lithography. Several groups [18, 19, 20]

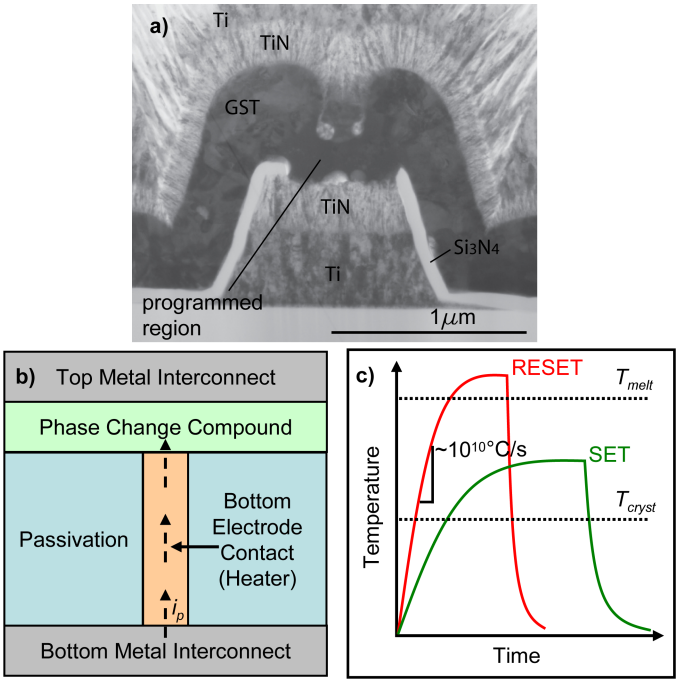

Figure 1.2: a) TEM image of a RESET PCM cell [14]. b) Schematic of a simple PCM cell with programming current i_p. c) Schematic of the temperature history during programming events.

demonstrated functioning devices using $Ge_2Sb_2Te_5$ (GST) nanowires (d=30-500 nm); however, challenges associated with proper alignment and integration processes remain. Other groups have developed bottom-up self-assembly based fabrication processes [21] that produce highly ordered PC nanoparticles of dimensions $\sim$ 10-20 nm. This process can be also utilized for growth of highly ordered Ge nanowires (NW) as the bottom electrical contact for PCM, further reducing the contact area and programming current [22].

The widespread adoption of PC materials in high-density optical phase change recording (e.g. CD-RW, DVD-RW) predates the recent advances in PCM. In high-density optical recording, a tightly focused laser heats a small spot in a PC layer sandwiched between dielectric thin films. Laser absorption in the PC layer causes phase transitions between the crystalline and amorphous phases, which have a strong contrast in optical reflectivity. Data are read by measuring the reflected intensity of a low power read laser. The main challenge facing PC optical recording is the diffraction limit. The Super-Resolution Near-Field Structure (super-RENS) has emerged to overcome this limitation by introducing a layer of randomly dispersed Ag or SbTe nanoparticles [1]. Recently, Small et al. [1] demonstrated that areal-density and readback signal noise characteristics can be considerably improved in a nano-patterned PC medium, but offered no commercially viable manufacturing process to realize the technology. Self-assembled PC nanoparticles are a promising candidate for integrating the super-RENS and patterned PC media schemes into a single media stack.

More recently, [23] reported the first evidence of the thermoelectric effect and its dramatic impact on the characteristics of linear PCM devices. Chalcogenide PC materials have also attracted much attention as candidates for thermoelectric power conversion applications [5, 7]. The figure of merit for power generation is (power factor) p $\sim 10^{-3}$ W m^{-1} K^{-2} for high performance thermoelectric materials compared to the reported values of $\sim 5 \times 10^{-4}$ and $\sim 5 \times 10^{-3}$ $Wm^{-1}K^{-2}$ for bulk [5], and superlattice $(Bi_{0.2}\ Sb_{0.8})_2Te_3$-$Sb_2Te_3$ [7] PC materials, respectively. Power factors comparable to (or larger than that of) high performance thermoelectric materials [24] may be within reach using fine grain PC thin film and nanoparticles due to enhancement in the phonon drag component of the Seebeck coefficient [25, 26]. Enhancement will be further compounded due to the reduced thermal conductivity of the thin film PC materials compared to the bulk samples [27, 28].

Thermal design and engineering plays an important role in optimizing the performance of both optical and PCM devices. In optical storage media, mark-edge jitter dominates the read signal noise. Jitter, storage density and speed are all influenced by the thermal properties of the constituent films [1, 29]. In PCM, thermal properties influence virtually every figure of merit: programming current, scaling, reliability, and cross-talk, among others [4, 30, 31, 32]. While compact models demonstrate the role of the total device thermal resistance [4, 30, 31, 33, 34], detailed finite element models discern the importance of the spatial distribution of thermal properties [30, 32, 35]. Device studies confirm that increasing interfacial [36, 37, 38] and volumetric [14, 39] thermal resistances, and confining heat generation [32, 40, 41, 42, 43, 44, 45] reduces programming current, and can simultaneously improve reliability [37, 40, 41].

In 2003 Lai [15] highlighted cell physics, programming current reduction and high density manufacture as the key areas of development needed for the success of PCM. Hudgens and Johnson emphasized similar points in their review outlining the history, fundamental physics and device operation, and recent technological progress in PCM [46]. They point out that the earliest devices [12, 13] suffered from excessive programming currents due to poor thermal efficiency, which was first addressed nearly three decades later [46]. A 2005 perspective [47] emphasized the contribution of Lankhorst [48] to reducing switching power and time through thermal design and use of new PC materials. Wuttig and Yamada [49] prepared a comprehensive review of PC material modeling and measurements. They suggest understanding the interplay between thermal and electronic conduction in the crystalline state is essential to overcoming this hurdle. Most recently, Lacaita et al. [50] reviewed PCM modeling, suggesting the need for additional study of electrical transport phenomena.

This chapter reviews thermal transport physics in phase change memory materials relevant for high-density data storage applications. We refer the reader to reviews of nanoscale thermal physics [51], thermometry [52], and thermal boundary resistance [53, 54] for broad examination of these topics. This section focuses on recent thin-film thermal measurements and the physical models important for improving phase change data storage devices. Section 1.1 summarizes the thermal property measurement techniques. Section 1.2 focuses on thermal property data and modeling. In Section 1.3 we briefly summarize topics receiving

recent attention, such as the Seebeck effect, and suggest new measurements and modeling that will improve understanding of the thermal properties of phase change memory materials.

1.1 Thermal Property Measurement Techniques

Thin film thermal conductivity measurement techniques have grown increasingly sophisticated and relevant over the past two decades. Nanoscale thin films often have lower apparent thermal conductivities than bulk films owing to increased scattering of heat carriers at lattice defects, grain boundaries, and impurities. Partial heat carrier transmission at interfaces gives rise to thermal boundary resistance (TBR). In thin films, it is common for the TBR to be comparable to the intrinsic thermal resistance of the film [51]. Chalcogenide thin films, in particular, exhibit all of these effects [27]. A key challenge in thin film thermal property measurements is separating the intrinsic thermal resistance from the TBR.

Measurement techniques may be grouped broadly into two categories: electrical and optical methods. The most common electrical technique for measuring chalcogenides is the 3ω method [55]. Several papers [2, 27, 56, 57, 58, 59, 60] utilize a variety of optical methods. The characteristic time and length scales of a measurement control which thermal properties are directly accessible through the data. The measurement technique determines the time scale. The measurement frequency limits frequency-domain electrical techniques such as 3ω. Detector bandwidth and laser pulse duration generally limit optical techniques. In the equilibrium regime, the thermal diffusivity physically links the time and length scales through the relation $L^2 \sim \sqrt{\alpha\tau}$, where L is the characteristic length, α is the thermal diffusivity, and τ is the characteristic timescale. Figure 1.3 illustrates this concept schematically for three common thermometry techniques: 3ω, nanosecond optical transient thermoreflectance (TTR), and optical time-domain thermoreflectance (TDTR). The figure's right axis assumes a chalcogenide thermal conductivity of 1 W/m/K. For films $\sim$ 100 nm and thinner, the 3ω and nanosecond TTR techniques can access only spatially averaged, or effective thermal properties. These methods offer excellent sensitivity to the thin film thermal resistance, but require multiple samples and ex-post thermal models to

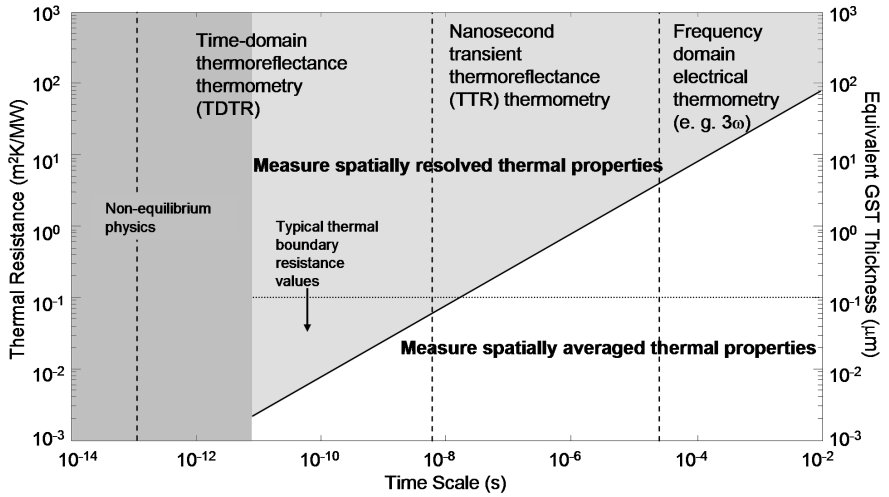

Figure 1.3: A regime map detailing the characteristic length and time scales of different measurements. The equivalent GST thickness axis assumes a thermal conductivity of 1 W/m/K. The GST thickness would need to be on the order of 1-10 μm to strongly influence the frequency response in a 3ω measurement. In contrast, typical thermal boundary resistance values can uniquely influence the transient temperature profile in TDTR measurements.

interpret thickness dependencies of the effective thermal conductivity. In contrast, TDTR has the temporal resolution to potentially resolve the TBR and intrinsic thermal properties uniquely. This section reviews the 3ω, indirect optical, nanosecond TTR, and TDTR techniques, and their application to phase change memory materials.

1.1.1 The 3ω Technique

The 3ω method uses a microfabricated metal line as both a heater and thermometer to measure the thermal response of the underlying thin films and/or substrate [55, 61]. Figure 1.4 depicts a typical experimental setup and sample structure for phase change memory materials. A current, I_ω, at frequency ω induces heat generation at frequency 2ω in the metal line. The linear thermal transfer function of the thin films and substrate relates the 2ω heating to the 2ω temperature rise in the metal line. The metal line resistance varies linearly with temperature, causing resistance oscillations, $R_{2\omega}$, at 2ω, and voltage oscillations at 2ω due to the product $R_{2\omega}I_\omega$. A lock-in amplifier captures the 3ω voltage, which determines

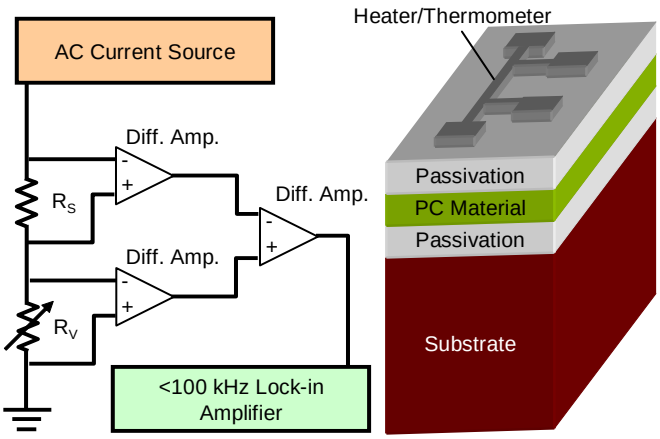

Figure 1.4: Schematic of a typical 3ω experimental system. Since many materials used in phase change memory are electrically conductive, passivation layers are necessary to prevent leakage current between the pads.

the thermal transfer function (i.e. thermal impedance) of the films and substrate [55]. The line heater must be completely electrically isolated to prevent measurement errors due to leakage current [62, 63]. Because most phase change memory materials are electrically conductive, the PCM material is often sandwiched between passivating thin films such as SiO_2, ZnS:SiO_2, or Si_3N_4 [29, 62, 63, 64].

Several assumptions accompany data interpretation in the 3ω method for thin films. The method directly measures the average temperature rise of the metal heater over a range of frequencies, typically, 1 Hz < f < 10 kHz. The thermal diffusion depth bounds the low end of the measurement frequency, which is chosen to satisfy the relations $f \gg \alpha_{sub}/d_{sub}^2$ and $b \ll \alpha_{sub}/d_{sub}^2$, where d_{sub} is the substrate thickness, $2b$ is the heater width, and α_{sub} is the substrate thermal diffusivity. The limits of the lock-in amplifier and modeling errors imposed by the thermal mass of the heating element commonly limit the upper frequency range [65]. The slope of the in-phase component of the heater temperature rise versus ln f determines the substrate thermal conductivity [55]. The 3ω technique strictly determines the frequency dependent thermal impedance of the thin film plus substrate [65, 66]. The most common assumptions for extracting thin film properties [29, 67, 61] are: 1) heat transfer through the thin films is 1-dimensional, and 2) the thermal response of the thin film

is frequency independent. Combined, these assumptions permit extraction of an effective thin film thermal conductivity, k_{eff}, using the relation [61]:

$$k_{eff} = \frac{Qd_{film}}{2bL\Delta T_{film}} \tag{1.1}$$

where Q is the total heating power, dfilm is the thin film thickness, L is the heater length, and ΔT_{film} is the temperature rise across exclusively the thin film of interest, which is commonly measured differentially [29]. Equation 1.1 explains why PCM papers employing the thin film 3ω method require differential measurements. The technique measures the total temperature difference across the thin films. Extraction of ΔT_{film} requires measuring samples with and without the PCM material. Once ΔT_{film} is determined, the effective thermal conductivity contains contributions from the TBRs between the PCM and passivation materials. Studies that also vary the PCM thickness separate the TBR from the PCM material intrinsic thermal conductivity [29, 64]. The length scales dictated by the frequency dependent thermal penetration depth and heater widths justify equation 1.1 and expose its limitations. The primary limitation is that the spatial distribution of thermal properties is not directly accessible with this technique.

Several authors report the thermal conductivity of PCM materials using the thin film 3ω method, indicated by the solid markers, and summarized versus film thickness in fig. 1.5 [27, 28, 29, 59, 60, 62, 63, 64, 67, 68, 69, 70, 71, 72]. The symbols ●, □, and ◊ correspond to the amorphous, fcc, and hcp phase values, respectively. Kim et al. [29] report the amorphous and fcc phase GST intrinsic conductivity and ZnS:SiO_2/GST TBR between 50K and 300K using multilayer samples. Giraud et al. [67] measured effective thermal conductivities for ZnS:SiO_2, SiO_2, amorphous GST, fcc GST, and TiN. Risk et al. [62] developed an in-situ 3ω technique to monitor the effective thermal conductivity of GST during the amorphous to fcc phase transition. The authors subsequently measured the effective thermal conductivities of the phase change materials GST, N-doped GST, AgInSbTe alloy, and GeSb, suggesting a modified Wiedemann-Franz law to predict the temperature dependence of the thermal conductivity [63]. Fallica et al. [64] report the room temperature thermal conductivity of SiO_2, Si_3N_4, amorphous, fcc, and hcp GST, and the SiO_2/GST TBR.

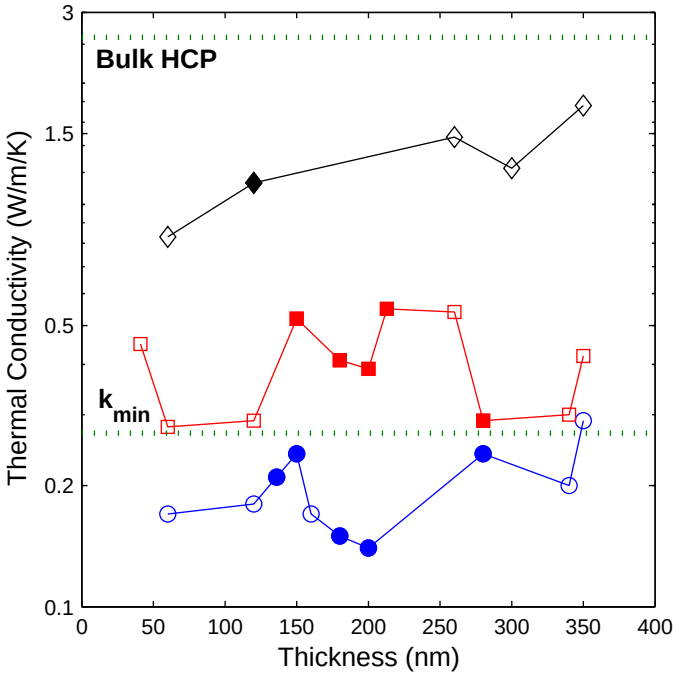

Figure 1.5: Thickness dependence of the effective and intrinsic thermal conductivities for $Ge_2Sb_2Te_5$ in the amorphous (●), fcc (□), and hcp (◊) phases. Solid markers indicate 3ω measurements. Open markers indicate optical measurements. For 3ω measurements using multiple thicknesses we plot the extracted intrinsic conductivity at the location of the average sample thickness. The horizontal line labeled kmin indicates the minimum thermal conductivity estimate in the amorphous phase [59], and the horizontal line at the top is the bulk thermal conductivity measured in the hcp phase [71].

Sample geometries and data interpretation methods vary in 3ω thin film measurements. These variations may explain some of the disparity in reported thermal conductivities. Dames and Chen [66] analyzed the effect of using a voltage source, as is common, instead of a current source as assumed in the derivation of the thermal model. They show a necessary correction factor to the thermal transfer function, $Z_{apparent}$:

$$Z_{true} = Z_{apparent}\left(1 - \frac{R_{sample}}{R_{total}}\right)^{-1} \tag{1.2}$$

where Z_{true} is the actual thermal transfer function to be used in fitting the data, R_{heater} is the heater resistance, and R_{total} is the total resistance of the circuit including output impedances. It is not clear whether the authors account for the voltage source correction, or whether their respective experimental systems are insensitive to the correction factor. For a typical voltage source with an output impedance of 50 Ω, and a series resistor comparable to the heater resistance between 5 Ω and 150 Ω, the correction factor varies between 1.09 and 1.75. The extracted effective thermal conductivity underestimates the true conductivity by a similar proportion. Using low resistance heaters or adding ballast resistors to the circuit when using a voltage source reduces the importance of the correction factor.

Heat spreading and the thermal mass of the heater introduce systematic errors to data interpretation under the 1D assumption. Risk et al. [62, 63] used an optimization algorithm [65] accounting for both effects, and Fallica et al., used a three-dimensional analytical heat transfer model [64]. Borca-Tasciuc et al. [73] examined the limits of the thin film assumptions. The ratio of the true thermal conductivity, k_{true}, to the conductivity extracted using the 1D assumptions, k_{1D}, is

$$\frac{k_{true}}{k_{1D}} = CS \tag{1.3}$$

C and S are non-dimensional parameters given by

$$C = 1 - \frac{k_y k_x}{k_S^2} \tag{1.4}$$

and

$$S = (1 + 0.38\beta_F)^{-1}; \qquad \beta_F \equiv \sqrt{\frac{k_x}{k_y}}\frac{d_F}{b}; \qquad \beta_F < 10. \tag{1.5}$$

k_y, k_x, and k_S are the thin film cross-plane, thin film in-plane, and substrate thermal conductivities, respectively. d_f and b are the thin film thickness and heater half-width, respectively. C measures the thermal conductivity contrast between the thin film and substrate. In isotropic materials, β_F reduces to the ratio of film thickness to heater width. For GST and TiN films $\sim$300 nm thick measured with 2 μm wide heaters, the 1D assumptions contribute to a $\sim$ 10% overestimation of the thermal conductivity. Equations 1.3-1.5 suggest it is possible to measure the thermal conductivity anisotropy of PCM materials by using thick films and/or thermally resistive substrates such as quartz.

3ω sample design comprises a series of trade-offs between signal maximization, analysis complexity, and the possibility of current leakage. If using a voltage source, such as the output of a lock-in amplifier, an impedance-matched, narrow heater maximizes the measurement signal, but the corrections from equations 1.2 and 1.5 may be significant. Using a current source always circumvents the need for equation 1.2 and the associated design trade-offs. Pinholes in the passivation layer or punctures from probes or wirebonds can cause current leakage through the PCM material. Increasing the passivation layer thickness can help prevent puncturing, but reduces the sensitivity to the PCM thermal conductivity. Increasing the heater thickness can also prevent puncturing, but the additional thermal mass may affect the measurement at high frequencies [73]. Risk et al. [63] recommend using beryllium-copper probe tips and advise against a wide variety of other contact methods. The need for electrical contact also complicates high temperature measurements [63]. Ultimately, leakage current characterization is essential for guaranteeing the reliability of 3ω measurements of thin films containing conducting materials.

1.1.2 Optical Thermometry Techniques

Optical thermometry techniques for PCM materials measure the transient change in reflectance to probe the thermal response of a thin film stack. In contrast to the 3ω measurement, optical techniques are non-contact and do not require electrical passivation layers or microfabrication steps beyond blanket film deposition. These features make optical techniques preferable to electrical techniques when conducting temperature dependent measurements. However, data extraction in optical thermometry often requires a numerical

solution of the heat diffusion equation, and it is significantly more challenging to measure the absolute temperature. Absolute optical temperature measurements require careful calibration of the temperature dependent reflectance, absorbed laser power, and photodiode responsivities [74]. These steps are unnecessary in linear thermal systems, where the shape alone of the transient thermal response determines the thermal properties.

The first optical measurements [2, 56, 57, 58] used the phase-dependent reflectance changes in optical PC disks to probe their thermal properties. A multi-parameter fitting routine matches the reflectance data to simulations of the coupled heat diffusion, phase change, and optical processes [2, 56, 57]. Recent optical measurements use nanosecond TTR [27, 68, 70] and TDTR [59, 60]. These techniques offer improved sensitivity and reduced errors due to systematic experimental errors compared to other optical methods [28]. In thermoreflectance measurements, a high intensity laser pulse, (i.e. pump), causes a temperature excursion in the sample. A probe beam samples the temperature of a metal transducer via its relative reflectance change. The linearity of the heat diffusion equation and transducer reflectance eliminates the need for absolute temperature measurement in thermoreflectance measurements. A wide range of materials satisfy the linearity requirements, making thermoreflectance a robust choice for thermal property measurements. This section focuses on thermoreflectance measurements of PCM materials.

1.1.2.1 Nanosecond Transient Thermoreflectance

Nanosecond TTR systems measure thermal decays with temporal resolution of < 10 ns range of ~ 10 ns to tens of microseconds [75, 76]. The reflected intensity of a continuous wave (CW) probe laser interrogates the transient surface temperature of a metal transducer via a high speed photodiode. TTR systems used in PCM material measurements have two common configurations: dual-transducer [68, 69, 70] and single-transducer [27, 72, 76]. In a dual-transducer system, two metal layers sandwich the thin film or films of interest. The pump and probe beams strike opposing sides of the sample, which is similar in principle to bulk flash diffusivity measurements [77]. The substrate must be transparent at the pump or probe wavelength. Figure 1.6 depicts a typical single-transducer TTR system [27, 72, 76]. A single metal layer coating the thin film of interest serves as both the pump absorber and

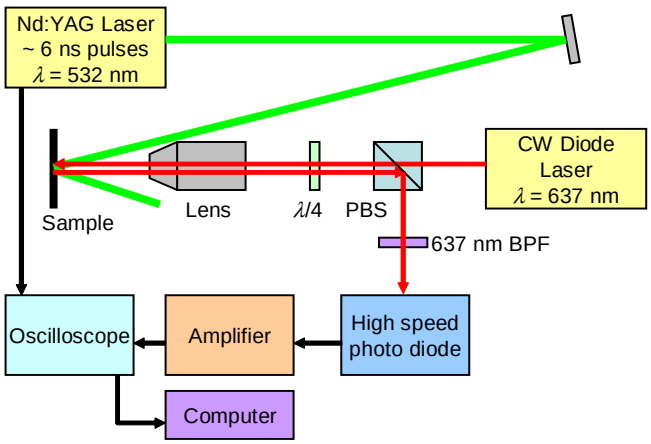

Figure 1.6: Schematic of a typical single-transducer nanosecond TTR system. The sample surface is a reflective metal.

probe transducer. When the thermal mass of the metal transducer is large, this configuration benefits from decreased sensitivity to the heat capacity of the thin film.

The hardware in both configurations is similar. A frequency doubled Q-switched Nd:YAG (yttrium aluminum-garnet) heats the sample with short (< 10 ns) pulses. The photodiode typically has a bandwidth between 500-650 MHz [27, 72, 76]. The pump pulse width and photodiode bandwidth determine the maximum temporal resolution of the measurement. Samples should have characteristic thermal diffusion times longer than this to ensure measurement accuracy. A bandpass filter at the probe wavelength is essential for preventing pump leakage into the photodiode. Pump pulses recur with a frequency of $\sim$1-10 Hz, characteristic of Q-switched lasers. The pulse repetition rate determines the maximum thermal decay time of the sample, which should be much longer than the inverse of the repetition rate to allow the sample to fully cool before the next heating event. The signal-to-noise ratio for a single pump pulse is poor, owing to the large measurement bandwidth and low transducer sensitivity. Relative reflectance changes are on the order of 10^{-4}/°C [78], and the pump pulse typically heats the sample by < 10°C [72]. Normalized thermal decay traces are, therefore, the average of thousands of pump events. The spatial extent of the pump beam is generally much larger than the thermal diffusion length, so a one-dimensional, multi-layer solution to the heat diffusion equation models the data.

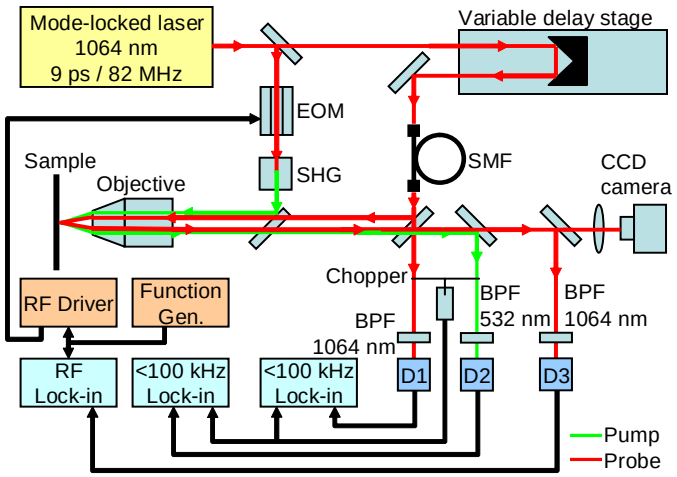

Figure 1.7: One implementation of a picosecond TDTR setup [60]. Other implementations use a Ti:sapphire laser and the phase ratio measured by the RF lock-in [79], but the systems are similar in principle.

1.1.2.2 Time-domain Thermoreflectance

TDTR is a pump-probe technique that can measure a wide range of thermal physics from electron-phonon interactions at timescales less than 10 ps to thermal decays of up to 7 ns [54, 79, 80]. TDTR uses a mode-locked laser to produce a pulse train with repetition rates between tens [60, 80] and a few hundreds [54] of MHz. Figure 1.7 shows one implementation of TDTR used in [60]. The laser output splits between a pump beam that is often frequency doubled [60, 80] and a probe beam which travels through a variable delay stage. The difference in optical path lengths fixes the delay time between the heating and probing events. The thermal decay trace is reconstructed by sweeping the delay stage through its range of motion. An electro-optic or acousto-optic modulator chops the pump beam, at frequencies below 100 kHz up to 10 MHz [79]. A lock-in amplifier detects the in-phase and out-of-phase components of the reflected portion of the probe beam at the modulation frequency. By limiting the measurement bandwidth to a small window around the modulation frequency, the lock-in amplifier greatly improves the signal to noise ratio compared to nanosecond TTR.

Several techniques can improve TDTR signal quality in practice. Capinski and Maris [81] incorporated a single-mode fiber (SMF) to reduce errors caused by probe beam misalignment and divergence as it traverses the delay stage. Schmidt et al. [80] used a beam expander to reduce beam divergence and a double pass of the delay stage to extend the measurement's temporal range. Cotescu et al., [82] and Cahill [79] demonstrated that measurements of the phase ratio rather than the signal amplitude eliminate the need for pump and probe normalization and can improve the signal to noise ratio.

TDTR data carries a wealth of information about thin film physics. At delay times less than $\sim$10 ps the two-temperature model [83] is often used to interpret the data because the electron and lattice temperatures in the metal transducer have not equilibrated. Picosecond acoustics measurements in TDTR systems can often be used to measure the local metal and thin film thicknesses and sound velocities [59], eliminating the need for other characterization methods. At longer times various models describe the thermal decays, the most general being a three-dimensional, multi-layer, frequency domain solution to the heat diffusion equation accounting for radial spreading and pulse accumulation [60, 79, 80]. Schmidt et al. [80] suggested varying the modulation frequency to sample different thermal properties, while Reifenberg et al. [60], recently used a series of different sample geometries to simultaneously extract intrinsic thermal properties and interface resistances. Because of its excellent temporal resolution, TDTR can directly measure TBR [60, 82]. Though the advantages of TDTR are numerous, the experimental apparatus and data analysis are considerably more complex than nanosecond TTR and 3ω.

1.2 Thermal Property Modeling and Measurements in PCM Materials

Figure 1.8 summarizes the temperature dependent amorphous, fcc, and hcp phase thermal conductivities of GST reported using nanosecond TTR and TDTR. For clarity the figure does not show effective conductivity data for the 350 nm and 60 nm layers measured in [27]. Including 3ω and effective thermal conductivity measurements, the amorphous, fcc, and hcp thermal conductivities span the ranges 0.14-0.29 W/m/K, 0.29-0.95 W/m/K, and

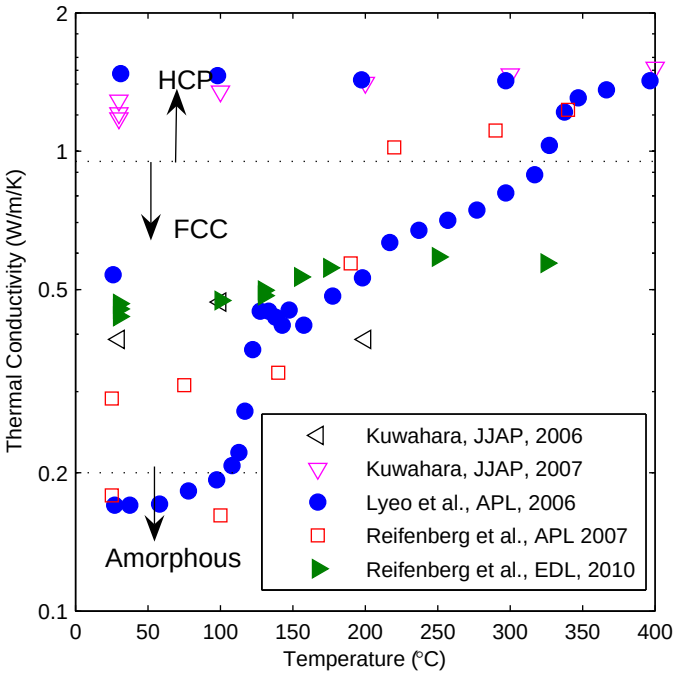

Figure 1.8: The temperature dependent thermal conductivity data taken with optical measurement systems. The data from [27] are for a 120 nm layer that underwent the fcc to hcp phase transition just above 200°C, as opposed to $\sim$ 340°C for the sample in [59].

0.77-2.14 W/m/K, respectively. Several studies note that mass diffusion [70], phase change material sublimation [27, 60], and component failure [62] limits the peak measurement temperature to 350-400°C. Overcoming these challenges to measure thermal properties up to and beyond the melting temperature remains an important goal.

The differences between amorphous phase measurements are generally small and agree well with the minimum thermal conductivity approximation, which describes phonon transport in amorphous solids in terms a network of localized oscillators [59, 84]. It is likely that local structural defects do not strongly affect the thermal conductivity because vibrations are already highly localized. The differences in the measured amorphous phase thermal conductivity may instead be due to partial crystallization [28] and/or differences in TBR in the case of effective thermal conductivity measurements.

The room temperature fcc phase conductivity generally falls between 0.3 W/m/K and 0.57 W/m/K. Measurements show increases in the electron contribution [63] and lattice contribution [59] can both account for the larger fcc phase thermal conductivity. The temperature dependence of the fcc phase conductivity is particularly important because it may strongly influence the programming current [30, 31, 32]. Lyeo et al. [59] show increasing fcc thermal conductivity with temperature. Other studies report no temperature dependence [69], or a slower increase in the fcc thermal conductivity with temperature [60].

Most thin film hcp thermal conductivity measurements span the range 1-2 W/m/K. The hcp phase exhibits a $\sim$ 10-100 fold decrease in electrical resistivity [59, 85, 86] attributed to increased hole mobility [59]. Unlike the fcc and amorphous phases, the electrical resistivity increases with temperature in the hcp phase [85]. The electron contribution dominates the hcp phase conductivity [59, 70, 71, 87]. Correspondingly, the hcp thermal conductivity shows a much weaker temperature dependence than the fcc and amorphous phases.

1.2.1 The Wiedemann-Franz Lorenz Rule

Despite the fcc phase having $\sim 10^3$-10^4 times higher electrical conductivity than the amorphous phase [85, 86], the increased electron contribution does not explain the differences in thermal conductivity in all measurements. The Wiedemann-Franz-Lorenz (WFL) rule

states the ratio of the electron component of the thermal conductivity, k_e, and the electrical conductivity, σ, is proportional to temperature, T,

$$\frac{k_e}{\sigma} = LT \tag{1.6}$$

where the proportionality constant L is the Lorenz number, 2.45×10^{-8} WΩ/K^2. The WFL rule applies at high and low temperatures when the same harmonic scattering mechanism dominates both charge and thermal transport. At intermediate temperatures, inelastic scattering reduces electron energy, degrading thermal transport without degrading charge transport [88]. At room temperature, the WFL predicts a small electron contribution in the fcc phase in [59] that does not fully account for the difference in fcc and amorphous thermal conductivities. In [63], the electron contribution does explain the difference. At 300°C, assuming an activation energy of 0.14 eV [32, 85] and constant lattice conductivity [59], the WFL overestimates the measured temperature dependent fcc thermal conductivity in [59], [60], and [69]. WFL alone cannot explain the observed temperature dependence of the fcc phase thermal conductivity. Simultaneous temperature dependent electrical and thermal conductivity measurements will offer insight into the role of electrons in thermal transport in the fcc phase.

1.2.2 Lattice Thermal Conductivity

Kinetic theory predicts the thermal conductivity, k, for a gas of particles as

$$k = \frac{1}{3}Cv\lambda \tag{1.7}$$

where C is the volumetric heat capacity, v is the characteristic particle velocity, and λ is the particle mean free path. In solids this equation applies for both the electron and phonon thermal conductivity contributions. In the high temperature limit under the Debye approximation for phonon dispersion, the minimum thermal conductivity approximation predicts no temperature dependence of the lattice component according to

$$k_{min} = \frac{1}{2}\left(\frac{\pi}{6}\right)^{\frac{1}{3}} k_b n^{\frac{2}{3}} \left(v_l + 2v_t\right) \tag{1.8}$$

where $k_b$is the Boltzmann constant, n is the atomic number density, and v_l and v_t are the longitudinal and transverse sound velocities, respectively [84]. Assuming constant or increasing heat capacity and mean free path, both models demonstrate that the increases in the sound velocity in the fcc phase [59, 89] should contribute to an increase in lattice conductivity. Molecular dynamics simulations accounting for anharmonic effects may improve understanding of lattice conduction including its temperature dependence. Reifenberg et al., [27] suggested the microstructure plays an important role in reducing the effective thermal conductivity. In crystalline materials with long range order, defects act as phonon scattering sites, reducing the intrinsic thermal conductivity [51]. The relative importance of the microstructure contribution decreases during and after annealing [27, 59]. Though no studies have directly examined their role, deposition conditions may strongly impact the microstructure. Annealing experiments with variable time and temperatures can also improve understanding of the lattice contribution to the thermal conductivity.

1.2.3 Thermal Boundary Resistance

Thermal boundary resistance arises from the partial transmission of heat carriers across an interface [53, 90]. The ratio of the temperature discontinuity, ΔT, across an interface to the heat flux, q", defines the boundary resistance:

$$R_b \equiv \frac{\Delta T}{q"}. \tag{1.9}$$

Pollack [90] and, later, Swartz and Pohl [53] prepared comprehensive reviews of TBR modeling and measurements for liquid-solid and solid-solid interfaces. Recent work offers insight into the classical mismatch models [91, 92, 93, 94, 95], high temperature TBR [96], metal-nonmetal TBR [82, 97, 98, 99], and metal-metal TBR [100]. In this context, the term metal applies to materials in which electrons contribute significantly to thermal transport, while phonons dominate thermal transport in nonmetals. There is an abundance of TBR models, but the search for a quantitatively accurate model that applies for a wide range of materials and temperatures is a topic of ongoing research. Nevertheless, many of the models offer physical insight that can be applied to improving PCM design.

1.2.3.1 Nonmetal-Nonmetal TBR

Phonons play an important role in thermal transport in PC and many electrode materials such as TiN [101]. The role of electrons is not fully understood in phase change materials such as GST. In electrode materials such as TiN, the electron contribution to the thermal conductivity depends on the material choice and process conditions [82, 60, 101]. In the molten phase, the electrical resistivity of GST is comparable to that in the hcp phase [85], so electrons probably play an important role in thermal transport [59] during reset pulses. In general, the thermal interface transport in PCM devices involves phonon-phonon, electron-phonon, and electron-electron processes. Many devices leverage TBR to reduce programming current [36, 37, 38, 102, 103] and improve reliability [37]. This section summarizes the physical models and measurements important for improving PCM devices.

The two most common analytical formulations for TBR are the acoustic mismatch (AMM) and diffuse mismatch (DMM) [53, 91]. These models predict interfacial phonon transport which dominates nonmetal interfaces. The AMM treats the TBR using a continuum acoustics model that describes phonon transmission by the mismatch in acoustic impedances. Transmission obeys an analog to Snell's law, and reflections are specular. The AMM finds agreement with experiment at temperatures less than 10 K [53]. The DMM better predicts TBR at higher temperatures by assuming diffuse phonon scattering at the boundary. Figures 1.9a and b show schematics of the AMM and DMM models, respectively, at nonmetal interfaces. TBR scales in inverse proportion to the transmission coefficient, α_{1-2}, which is given by

$$\alpha_{1-2} = \frac{\sum_j c_{2,j}^{-2}}{\sum_j c_{1,j}^{-2} + \sum_j c_{2,j}^{-2}} \tag{1.10}$$

for the DMM model, where $c_{i,j}$ refers to the sound velocity in material i in phonon mode j [53]. Equation 1.10 qualitatively describes the phonon density of states (DOS) mismatch between materials 1 and 2. Materials with large DOS mismatches generally have larger TBRs [98]. The Debye temperature ratio offers another estimate of the DOS mismatch [37, 98]. Modified approaches based on the AMM and DMM attempt to improve agreement with experiments by capturing a range of physical effects such as the actual density of states [91], and weak bonding at the interface [92]. Reifenberg et al. [60] reported that equation

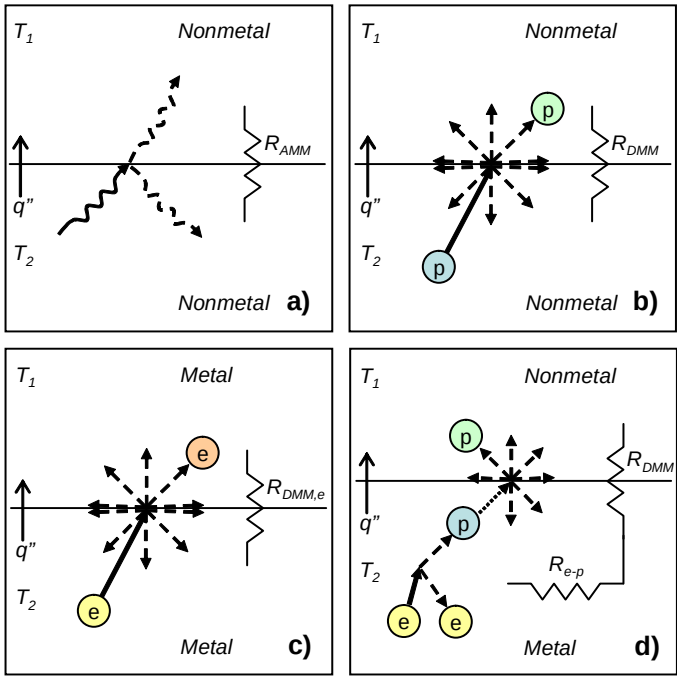

Figure 1.9: Physical depictions of several TBR models: a) acoustic mismatch model (AMM) [53]; b) diffuse mismatch model (DMM) [53]; c) electron DMM [100]; d) electron-phonon coupling model [24]. The e and p denote electrons and phonons, respectively.

1.11, the DMM using the measured heat capacity [91], $C_1(T)$, best matches temperature dependent data for phonon dominated TiN/fcc GST TBRs.

$$R_b = \left(\frac{\alpha_{1-2}}{12} c_{1,D}^3 \sum_j c_{1,j}^{-2} \right)^{-1} C_1(T)^{-1} \tag{1.11}$$

The subscript D refers to the use of the Debye model, and the assumption that all phonon polarizations have the same sound velocity. Molecular dynamics simulations offer detailed explanations of several other influential effects: the frequency dependence of the transmission coefficient [93], phonon transmission between dissimilar lattices [95], the role of anharmonic effects in the temperature dependence [96] and the effect of interface disorder [94, 96].

1.2.3.2 Metal-Metal TBR

When electrons contribute significantly to the thermal conductivity of one or both contacting materials, they also affect interfacial transport. In the case of metal-metal interfaces, electrons dominate thermal transport in both materials. The TBR at metal-metal interfaces is about an order of magnitude smaller than that when a nonmetal is involved [100]. Mahan and Bartkowiak [104] showed electrical interfaces dominated by tunneling have an exact analog for the WFL rule:

$$R_{b,WFL} = \frac{\rho_b}{LT} \tag{1.12}$$

where ρ_b is the electrical boundary resistance (EBR) in Ωm^2.This result applies to interfaces such as grain boundaries, where the contacting materials are identical. Gundrum et al. [100] derived a DMM model for TBR between different metals,

$$R_{DMM,e} = \frac{4(Z_1 + Z_2)}{Z_1 Z_2} \tag{1.13}$$

where $Z_i = \gamma_i T v_{f,i}$ is the product of the electronic heat capacity per unit volume, $\gamma_i T$, and the Fermi velocity, $v_{f,i}$, of side i, and γ_i is the Sommerfeld parameter. Figure 1.9c schematically depicts the electron DMM model, which shows relatively good agreement with experimental data for Al/Cu interfaces [100]. Given the intimate relationship between

charge and thermal transport at metal-metal contacts, in-situ characterization of the EBR could provide much insight into the high temperature TBR in PCM devices.

1.2.3.3 Metal-Nonmetal TBR

The electron and phonon systems must interact to transport heat across metal-nonmetal boundaries. Huberman and Overhauser [99] and, later, Sergeev [105] showed electrons exchange energy anharmonically with joint phonon states near the interface. The joint phonon states subsequently communicate energy between the materials. Majumdar and Reddy [97] showed that electron-phonon coupling in the bulk of the metal, followed by phonon-phonon transmission at the interface can also explain the metal-nonmetal TBR. Figure 1.9d shows this scenario schematically. The additional resistance contribution from the electron-phonon coupling, R_{e-p}, is

$$R_{e-p} = \frac{1}{\sqrt{G k_{p,metal}}} \tag{1.14}$$

where G is the rate of electron-phonon energy transfer per unit volume, $\sim 10^{16} - 10^{17}$ W/m^3/K, and $k_{p,metal}$ is the phonon contribution to the thermal conductivity in the metal, $\sim$10-20 W/m/K [97].

1.2.3.4 TBR in PCM Materials

There are limited TBR data for PCM materials. Figure 1.10 summarizes the available data [29, 37, 60, 64]. The TBR between the bottom electrode, or heater, and the GST is extremely important since the bottom electrode dissipates most of the heat during programming [30]. The TiN/fcc GST TBR decreases from 26 m^{2}K/GW to 19 m^{2}K/GW between 30°C and 325°C. A TBR of 10 m^{2}K/GW is equivalent in thermal resistance to $\sim$ 190 nm of TiN at room temperature [60], or $\sim$ 26 nm of thermally grown SiO_2. At room temperature, the series combination of the TiN/GST TBR and Al/TiN TBR increases the apparent thermal resistance through the heater by almost a factor of 7, assuming 100 nm tall TiN heater via contacted by an Al interconnect [60]. Kim et al., [37] showed an even larger average interface resistance of $\sim$ 77 m^{2}K/GW between a C_{60} layer, used as part of the bottom electrode, and Al and TiAlN films. The results for these electrode materials agree qualitatively

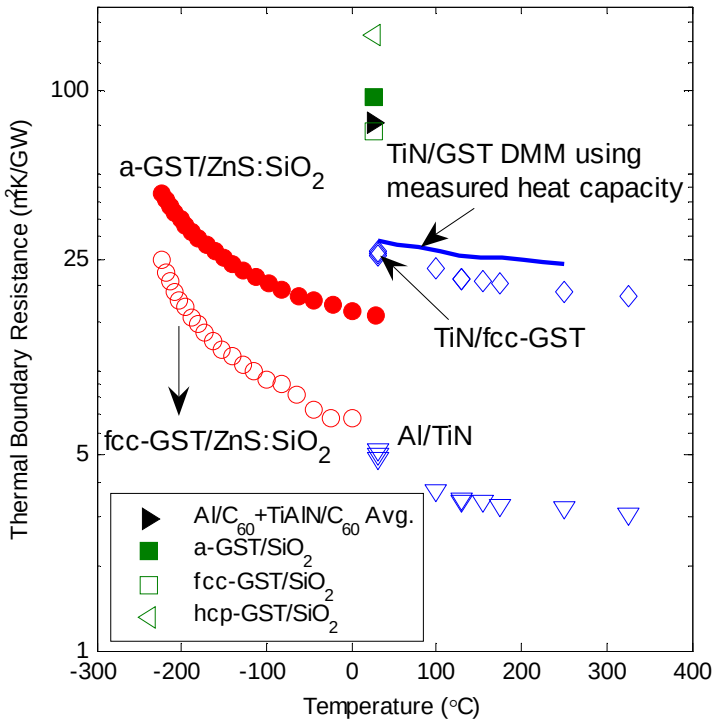

Figure 1.10: Summary of the temperature dependent thermal boundary resistance data for phase change materials. A TBR of 10 m^2K/GW has thermal resistance equal to $\sim$ 190 nm of TiN [60], or 14 nm of thermally grown SiO_2.

with other materials with similar Debye temperature mismatches [96]. Other studies used the 3ω method to extract the TBRs between GST and ZnS:SiO_2 [29], an important interface in optical media, and GST and SiO_2 [64]. Both reports show larger TBR in the amorphous phase, which the authors attribute to larger acoustic mismatch and interface roughness.

The TBR models and data raise many questions whose answers will improve PCM design and engineering. The models demonstrate that the nature of charge and thermal transport in the electrode and phase change material play an essential role in determining the TBRs. The temperature dependent transport properties of thin film electrode materials such as TiN are not well characterized. The intrinsic electrical properties of GST are well understood, but the EBR is not. High temperature TBR measurements of GST thin films at T>400°C still pose significant challenges for standard experimental approaches. Ptitsina et al. [106] showed transverse phonons dominate electron-phonon coupling in impure thin metal films over a wide temperature range. Because the molten phase does not support transverse modes, the high temperature TBR may not conform to the standard models.

1.3 New Developments

Recent years have seen rapid progress in understanding of thermal transport in PCM devices. Still, fundamental questions remain about the intrinsic thermal properties and the thermal boundary resistance in PCM materials. The push toward faster, more reliable, devices and increased storage density simultaneously offers new challenges for thermal property measurements and modeling. This section highlights many unsettled thermal transport questions and how their answers will influence future generations of PCM technology.

PCM optimization depends on a thorough comprehension of thermal properties. Significant experimental difficulties accompany temperature dependent measurements of the thin film thermal properties above 400°C. Are steady state high temperature measurements possible for the fcc, hcp or molten phases? Reset simulations often rely on the WFL rule to predict the fcc phase thermal conductivity near the melting temperature and in the molten phase. Are these models accurate at all temperatures? Simulations assume isotropic thermal conductivity. Do phase change materials show thermal property anisotropy and does

this affect cross-talk between devices? Does the thermal conductivity change during threshold switching? What are the heater/electrode thermal properties, how do they affect device performance, and can these properties be engineered to improve device performance? Lastly, the TBR strongly affects device scaling [32]. Do intrinsic properties or extrinsic effects, such as the deposition conditions and annealing history, control the TBR? Will measurements of phase change materials resolve how electron-phonon coupling physics influences the TBR?

Recent multi-level phase change cells [16, 107, 108, 109, 110] incorporate several phase change materials to increase data storage density. Three studies [27, 62, 68] measured the effective thermal conductivities of various thin film phase change materials. Yanez-Limon et al. [111] measured a wide range of bulk films. Kuwahara et al. [69] showed increasing thermal conductivity with Sb concentration in Sb-Te alloys, while Yang et al. [28], attempted to correlate thermal conductivity of GeSbTe alloys with tellurium concentration. In general multi-level designs control the heat generation location using geometry and threshold voltage differences between phase change materials. Engineering the thermal resistance can also help control the melt and crystallization locations, but has received less attention. As multi-level implementations become more common, the stoichiometry dependence of thermal property data will become increasingly important.

Scalability is one of PCM's most lauded features, but new physical complexities arise as devices shrink. As temperature gradients increase in scaled devices, thermoelectric effects may become increasingly important. A recent study [23] attributes programming asymmetry in a linear PCM cell to thermoelectric effects. Another study [85] shows the room temperature Seebeck coefficients of thin GST in the amorphous and fcc phases are comparable to those in the best thermoelectric materials [7, 112]. Further complicating matters is the existence of the boundary Seebeck effect [113], and its temperature dependence. The possibility of using phase change nanowires [18, 19, 20, 34] and nanoparticles [21] to minimize device size merits investigation of their thermal properties. Lee et al. [114], for example, reported low effective thermal conductivities for GST-SiO thin film composites. Use of vertically aligned Ge nanowires [22] or carbon nanotubes as the heater can significantly reduce the device cross-section area. The possibility of ballistic transport

in these structures further complicates thermal conductivity and TBR calculations, but may significantly reduce programming current.

Chapter 2

The Impact of Thermal Boundary Resistance in Phase-Change Memory Devices

This chapter examines how thermal boundary resistance affects the temperature profile and programming current of phase change memory devices. Thermal boundary resistance is partly responsible for the strong size dependence of the effective thermal conductivity of GeSbTe layers [27]. Kencke et al. [32] showed the combined effects of thermal and electrical boundary resistance on reducing programming current, but this work specifically isolates the impact of the thermal boundary resistance, showing that it strongly influences the device temperature profile and programming current.

2.1 Thermal Boundary Resistance

No broadly accepted model currently exists for predicting TBR at temperatures above tens of Kelvins [51, 53]. The acoustic mismatch (AM) and diffuse mismatch (DM) models lend insight into the source of TBR as partial transmission of energy carriers. More recent lattice dynamical (LD) models capture important interface physics neglected by the continuum AM and DM approaches. LD models capture the impact of interface disorder, lattice mismatch, interface bond strengths, and phonon dispersion at high frequencies on the phonon

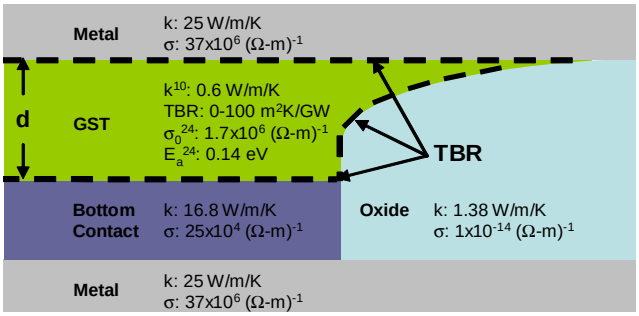

Figure 2.1: Schematic of the model geometry including electrical and thermal properties. The dashed lines indicate the interfaces where the TBR is applied. The model is axially symmetric about the left boundary.

transmission coefficient [95, 94, 93], but require precise information about atomic arrangements that is unavailable for PCM interfaces. The thermal boundary resistance between a broad variety of materials ranges from 1 m^2K/GW to 100 m^2K/GW at room temperature [96, 115]. Room temperature measurements of the TBR between phase change material $Ge_2Sb_2Te_5$ (GST) and materials of interest vary from 5 m^2K/GW to over 30 m^2K/GW [29, 60]. LD calculations on Lennard-Jones (LJ) solids predict the thermal boundary conductance increases with temperature by ~11% per 100 K for an LJ solid melting at 900 K [96]. At the upper bound, TBR at the GST-bottom contact (BC) interface would approximately double the thermal resistance of a 50 nm GST layer. The present work varies the GST TBR from 0 m^2K/GW (i.e. perfect thermal interface) and 100 m^2K/GW.

2.2 Electrothermal Modeling and Implementation

Figure 2.1 shows the GST phase change cell geometry used here. Other PCM geometries include the planar and edge-contact cells [44]. Device geometry affects programming current by changing thermal confinement [44, 116]. TBR can significantly enhance confinement, and should be considered in geometries where the TBR is comparable to bulk thermal resistances in series with the interfaces. The temperature profile is determined by the steady-state heat diffusion equation with Joule heating. The GST interface condition considers the TBR using $q'' = \Delta T / R_{th}$, where q'', ΔT, and R_{th} are the heat flux, temperature drop across the boundary, and TBR, respectively. The TBR is uniform at all GST interfaces,

though this is unlikely in actual devices. Joule heating and temperature dependent electrical conductivity couple the heat equation to the Poisson equation for the electrical potential and current distributions. Transient simulations approach the steady state solution after ~1 ns because programming pulses are much longer than the thermal time constant. Figure 2.1 shows the thermal and electrical conductivities used in the simulations. Data show that the FCC phase thermal conductivity increases with temperature up to ~300/°C with a slope of ~0.0025 W/m/K^2 above 200°C [59, 27]. Our work assumes constant thermal conductivity since no data are available at temperatures above 300°C. We neglect the temperature dependence of TBR. Both assumptions cause the model to over-predict the total thermal resistance, and underestimate the programming current. The ratio of the two resistances is not strongly affected since both resistances are expected to decrease in similar proportion to their room temperature values. The temperature dependence of the electrical conductivity of crystalline GST follows that of a semiconductor [85], $\sigma = \sigma_0 exp(-E_a/k_bT)$, where E_a is an electrical activation energy and k_b is the Boltzmann constant. We simulated set to reset transitions for various TBR and GST thickness combinations, and for different effective thermal conductivities with no TBR. Figure 2.1 shows the simulation geometry with GST thickness, d, confinement depth of 25 nm, and a BC diameter (CD) of 50 nm with height of 150 nm. The minimum current required to transition the cell from high to low resistance (set to reset states) defines the programming current. The simulations assume the GST volume begins in the crystalline phase and the entire molten region quenches into the amorphous phase.

2.3 The Role of Thermal Boundary Resistance

The thermal and electrical resistances of the BC and phase change region determine where the maximum temperature occurs. Cells that minimize programming current experience maximum temperature just above the GST-BC interface [31]. They have $R_{BC,th} \approx R_{PC,th}$ and $R_{BC,e} \approx R_{PC,e}$ [31]. $R_{BC,th}$ and $R_{PC,th}$ are the thermal resistances of the BC and phase change region, respectively, and $R_{BC,e}$ and $R_{PC,e}$ are the electrical resistances of the BC and phase change region, respectively. This work examines cells where the peak temperature occurs in the phase change region above the interface, which is common for designs with

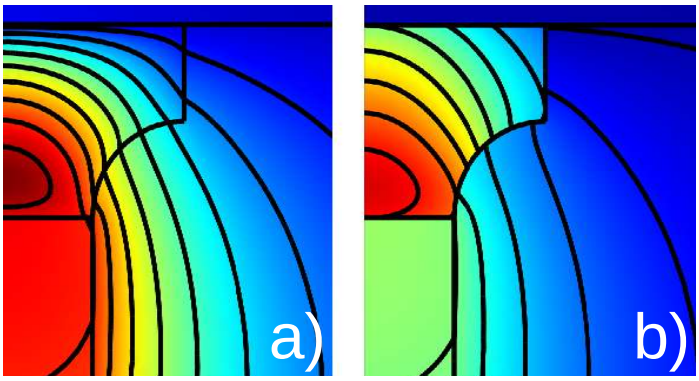

Figure 2.2: Temperature profiles for reset simulations with GST thickness of 50 nm. No TBR is applied between at the GST interfaces in a). b) shows the result of a TBR of 50 m^2K/GW. The temperature scale is the same in each figure. The peak temperature in a) is 1092 K with programming current of 1.6 mA and the peak temperature in b) is 1015 K with programming current of 1.2 mA.

$R_{BC,th} \ll R_{PC,th}$ and $R_{PC,e} < R_{BC,e}$. The results apply to cells with TBR in series with the minimum thermal resistance (commonly the BC). The TBR is in series with the BC resistance when the peak temperature occurs at or just above the interface. Electrical and thermal interface physics need to be included to fit experimental data in such a cell [32].

The temperature distribution during the reset pulse controls the phase distribution and resistance change of the cell. The temperature at the edges of the BC must exceed the melting temperature for the amorphous region to cover the BC-GST interface, as is required for large electrical resistance changes . Amorphization of the edges occurs at lower programming currents in cells with high lateral temperature uniformity. Figure 2.2 shows temperature distributions for a cell with no TBR (a) and one with a TBR of 50 m^2K/GW (b). TBR decreases the GST volume thermal resistance relative to the total thermal resistance between the active region and the ambient. This increases the lateral temperature uniformity in the GST and causes the location of maximum temperature to move toward the GST-BC interface. TBR, therefore, lowers programming currents and peak cell temperatures. Figure shows how the spatial distribution of thermal resistances modifies the programming current. Solid markers indicate varying TBR with constant thermal conductivity. Programming currents decrease with TBR for all GST thicknesses. Introducing a TBR of 50 m^2K/GW reduces the programming current by ~20% for the 25 and 50 nm GST layers,

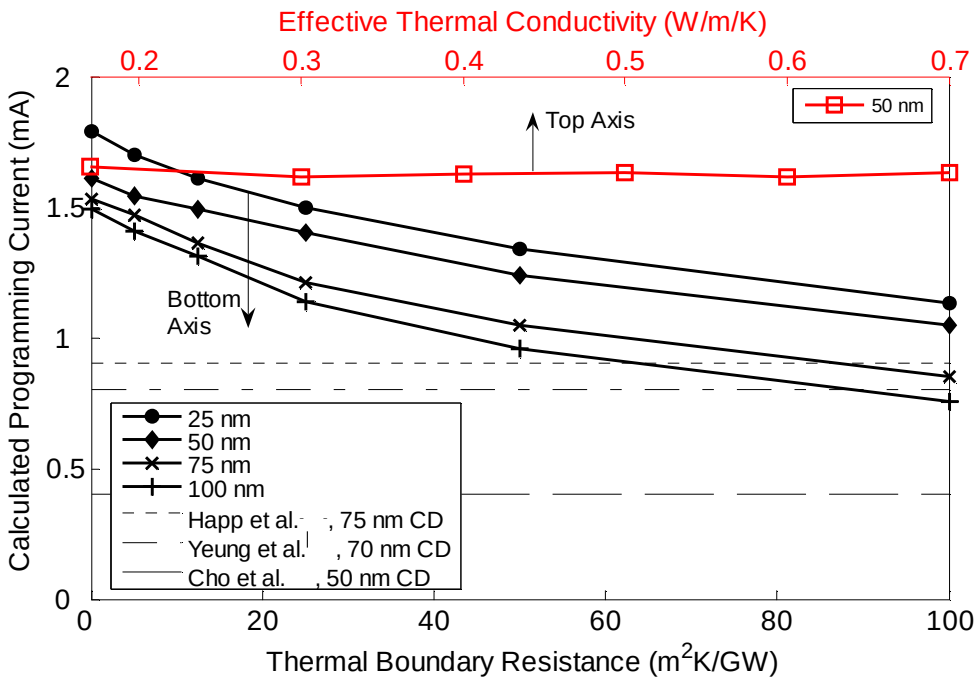

Figure 2.3: The calculated programming current for different values of TBR with constant thermal conductivity (solid markers, bottom axis) and thermal conductivity with no TBR (hollow markers, top axis). Experimental data for cells with similar geometry and different BC-GST contact diameters (CD) are shown as dashed horizontal lines.

and ~30% for the 75 and 100 nm GST thicknesses. Lateral heat loss increases with GST thickness, decreasing lateral temperature uniformity. Relative increases in lateral thermal resistance account for larger decreases in programming current in thicker films. The hollow markers in figure 2.3 show that varying the GST effective thermal conductivity (with no TBR) has little effect on programming current. When $R_{BC,th} \ll R_{PC,th}$, very little heat is lost vertically through the GST, which renders the programming current relatively insensitive to the GST thermal conductivity [31]. Additionally, decreasing the thermal conductivity increases the thermal resistance isotropically. This decreases both the heat required to affect a given temperature change and the lateral temperature uniformity. Decreased lateral temperature uniformity requires larger programming currents to heat the edges above the melting temperature. This effect offsets the decrease in programming current caused by the larger thermal resistance.

2.4 Conclusions

This work demonstrates that the TBR strongly influences the design and scaling of PCM devices. The predicted programming current decreases with TBR owing to increased thermal confinement of the active region from the BC and increased lateral temperature uniformity in the GST. Significant reductions in programming current are achievable by engineering thermal anisotropy into the active region of PCM devices. Deliberate introduction of interface disorder, Debye temperature mismatch, and weak bonding between the phase change layer and surrounding metals may increase the TBR and reduce the programming current. Materials must be carefully chosen to increase the TBR without degrading electrical properties. Recent work shows this is possible by adding fullerene layers at interfaces [37]. It may be possible to engineer thermal property anisotropy into the phase change region by alternating low conductivity phase change layers with electronically compatible layers that have high in-plane thermal conductivity. Thermal property anisotropy can enhance vertical thermal confinement and lateral temperature uniformity, thereby reducing programming current.

Chapter 3

Closed Form Thermal Analysis of Phase Change Memory Devices

This chapter examines closed form thermal models for phase change memory devices. While PCM has many desirable characteristics for non-volatile memory applications, key challenges must be overcome to ensure its long term success. As indicated in the previous chapters, two of the greatest challenges are reducing reset current and improving reliability. Programming current determines the size of the external transistors and the power consumption of the device. Reducing the programming current, therefore, increases memory capacity and reduces power consumption- key factors in consumer electronics. The consumer market also demands highly reliable devices. Failure in PCM devices is closely related to the cycling performance, phase change processes, interface reactions, and resistance-current behavior. The future success of PCM depends on understanding and using device physics and design to address these challenges.

Progress in understanding the electronic, phase change, and thermal physics of PCM has been rapid. Pirovano et al. [117] provided a model for the electronic switching effect in GST based on the competing effects of impact ionization and recombination. The model reproduced experimental I-V measurements and is the standard model used in device simulations. Later, Ielmini proposed and validated a trap limited Frenkel-Poole model explaining sub-threshold conduction in amorphous GST [118]. Kencke et al. [32], showed

electrical interface resistance (EIR) significantly affects programming current and temperature profiles in the device. Through x-ray absorption fine structure spectroscopy (XAFS) data, Kolobov et al. [119], explained the reason for rapid phase transitions in chalcogenides. The so-called "umbrella flip" of a Ge atom between interstitial sites is the main structural difference between the amorphous and FCC phases of GST. Welnic et al. [120], used the structural information to determine phase dependent material properties using ab initio density functional theory (DFT) calculations. Most recently, Hegedus and Elliott [121] performed molecular dynamics calculations for the entire melting, amorphization, and crystallization of GST. This work provides significant insight into the nature of the phase change and how to engineer phase change materials for more rapid phase transitions. Investigation of the thermal physics in phase change materials shows a slow increase of the thermal conductivity of GST with temperature [59, 60, 27]. The thermal conductivity of amorphous GST is near the physical minimum [59]. Experimental work by Reifenberg et al. [27] shows a significant size dependence of the effective thermal conductivity that is in part attributable to thermal boundary resistance (TBR). Additionally, multiphysics modeling has shown TBR strongly affects PCM programming current and temperature distributions [30].

PCM device design has also advanced rapidly. Axisymmetric planar cell geometries, as shown in figure 3.1a, have evolved into a variety of different geometries that lower the reset current. Edge-contact cells showed dramatically reduced current when compared with planar cells [44]. Axisymmetric confined cells, shown schematically in figs. 3.1b and 3.1c, show marked reductions in programming current compared to planar cells [32, 40, 43]. Yet they maintain the same simple manufacturing steps. Multiphysics finite element simulations suggest that improved thermal design is largely responsible for reset current reductions in these cells [32, 44, 40, 43]. Several simple models relating reset current and thermal design parameters compare favorably with experimental data [122, 45, 33, 31]. A more detailed thermal resistance and capacitance model demonstrated key scaling trends in confined PCM geometries [33]. Existing PCM design tools have significantly improved device performance. However, these tools are either extremely sophisticated or very simple. While the sophisticated tools incorporate increasingly complex physical models, they do so at the expense of design insight. The simple models offer excellent

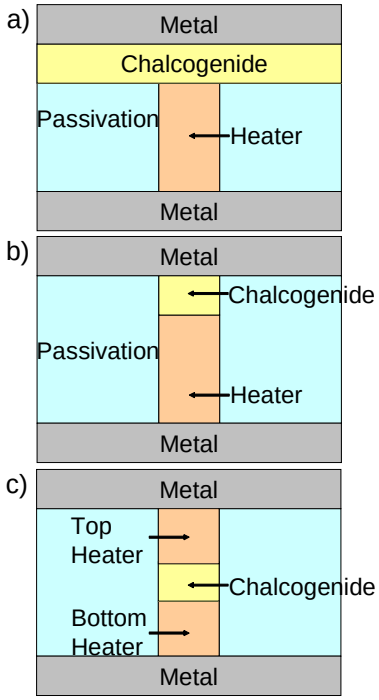

Figure 3.1: Schematics of different PCM geometries. The planar cell is in a), the confined cell is in b), and the double confined cell is in c).

physical insight at the expense of overlooking potentially important physics. This chapter presents two closed form solutions. The first is a simple resistor model used to predict peak temperature and heat flow in PCM. The second presents PCM in the framework of a thermal fin incorporating electrical and thermal interfaces. These models are used to explore the impact of electrical and thermal interfaces in PCM and to optimize confined cell geometries. The work in this chapter significantly extends the PCM designer's ability to rapidly assess and optimize device geometry and materials in physically insightful ways.

3.1 Resistance Models for Reset Current

Thermal resistance models offer a simple method for calculating the impact of geometry and material parameters in phase change cells. Solutions are closed form expressions for reset current and reset power.

3.1.1 General Solution for Planar and Confined Cells

The thermal circuit solutions for geometries in figure 3.1 condense to a general form in terms of the effective electrical and thermal resistances of the cell. Several assumptions allow this simplification. The phase change cell is in steady state because the cell's thermal time constant is much shorter than reset pulse times. Therefore the thermal circuit consists only of resistance elements. The model assumes heat is injected at a single location in the cell, rather than distributed through the cell by Joule heating. Though Sadeghipour et al. [122] showed approximately 20% of the heat in PCM is lost to the passivation material, the models neglect heat transfer into the adjacent passivation material. This causes the models to under-predict the programming current and power. A fitting parameter treats the effects of the previous two assumptions. The models also assume the top and bottom metal electrodes are thermal grounds.

Figure 3.2 shows the thermal circuits for each PCM design overlaid on their respective schematics. The models assume melting of the chalcogenide during a reset pulse begins at

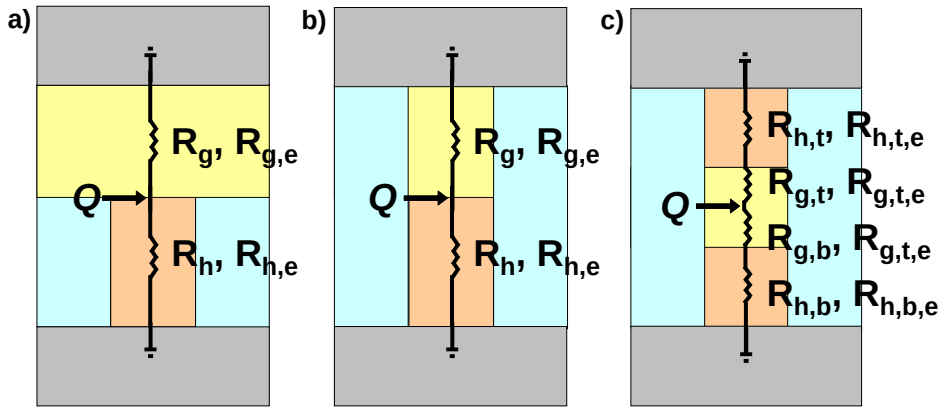

Figure 3.2: Thermal resistance models used for the different PCM geometries. The geometries are similar in the sense that heat must exit the device through one of two parallel paths.

the point of heat injection. The condition for reset is, therefore

$$QR_{th,eff} = \Delta T_m \tag{3.1}$$

where Q is the power dissipated by the cell, $R_{th,eff}$ is the effective thermal resistance, and ΔT_m is the temperature change required for melting. Injected heat flows to thermal ground via parallel upward and downward paths. For melting to occur at the point of injection is

$$\Delta T_m = Q\frac{R_{up,eff}R_{down,eff}}{R_{up,eff}+R_{down,eff}} \tag{3.2}$$

where $R_{up,eff}$ and $R_{down,eff}$ are the effective thermal resistances to the top and bottom thermal sinks, respectively. Electrical current causes Joule (I^2R) heating as it flows through the heater and chalcogenide alloy. Substituting this into equations 3.1 and 3.2 gives a general expression for the reset current, I_R

$$I_R = \sqrt{\frac{\Delta T_m}{\alpha R_{e,eff}R_{th,eff}}} \tag{3.3}$$

$R_{e,eff}$ is the effective electrical resistance of the cell, equal to the series resistance of the heater and chalcogenide, and α is a fitting parameter used to account for the actual heat generation distribution and heat loss to the passivation material.

3.1.2 Specific Solutions for Planar and Confined Cells

In planar designs, equation 3.3 reduces to

$$I_R = \sqrt{\frac{\Delta T_m}{\alpha} \frac{1}{R_{g,e} + R_{h,e}} \frac{R_g R_h}{R_g + R_h}} \tag{3.4}$$

where $R_{g,e}$ and $R_{h,e}$ are the electrical resistances of the chalcogenide and heater, respectively, and R_g and R_h are the thermal resistances of the chalcogenide and heater, respectively. This result is the same as that presented by Russo et al. [31]. The electrical and thermal spreading resistances into the chalcogenide are given by [123]

$$R_{g,e} = \frac{\rho_g}{\pi d} arctan\left(\frac{4t}{d}\right) \tag{3.5}$$

and

$$R_g = \frac{1}{\pi d k_g} arctan\left(\frac{4t}{d}\right) \tag{3.6}$$

respectively. Here d is the contact diameter between the heater and chalcogenide, t is the chalcogenide thickness, and $k_g$and ρ_g are the thermal conductivity and electrical resistivity of the chalcogenide, respectively. The heater thermal and electrical resistances are

$$R_h = 4\frac{d_h}{k_h \pi d^2} \tag{3.7}$$

and

$$R_{h,d} = 4\frac{\rho_h d_h}{\pi d^2} \tag{3.8}$$

where ρ_h, k_h, and d_h are the heater's electrical resistivity, thermal conductivity and height, respectively.

For the confined cell, equation 3.3 also reduces to equation 3.4. Substituting for the electrical and thermal resistances for 1D cylindrical geometry yields

$$I_R = \frac{\pi d^2}{4}\sqrt{\frac{\Delta T_m}{\alpha}\frac{k_h}{\rho_h d_h^2}\left(1+\frac{\rho_g d_g}{\rho_h k_h}\right)^{-1}\left(1+\frac{d_h k_g}{d_g k_h}\right)} \tag{3.9}$$

In the double confined cell the effective electrical and thermal resistances are

$$R_{e,eff} = \frac{4}{\pi d^2}\left(\rho_h d_{h,b} + \rho_g d_g + \rho_h d_{h,t}\right) \tag{3.10}$$

and

$$R_{th,eff} = \frac{4}{\pi d^2}\frac{\left(\frac{d_g}{2k_g}+\frac{d_{h,b}}{k_h}\right)}{\left(\frac{d_g}{2k_g}+\frac{d_h}{k_h}+\frac{d_{h,t}}{k_h}\right)} \tag{3.11}$$

respectively. The subscripts b and h denote the bottom and top heaters, respectively.

3.2 Thermal Fin Model

The thermal fin model offers the simplicity of a closed form solution with the power to resolve the device temperature profile. The model includes thermal and electrical interface resistances, conduction into the passivation material and distributed heat generation terms.

3.2.1 Model Formulation

Figure 4 shows the geometry and physical parameters used in the thermal fin model. Table 3.1 describes and quantifies each of the parameters. The fundamental assumption of the thermal fin is constant cross-sectional temperature at any location along the length of the fin. The heat diffusion equation reduces to

$$\theta_i^{"} - m_i^2\theta_i + \frac{Q_i^{'''}}{k_i} = 0; \quad m_i^2 = \frac{P}{R_i k_i A}; \quad \theta = T - T_0 \tag{3.12}$$

Here T is the position-dependent temperature, P is the perimeter equal to πd and A is the cross section area equal to πd^2. TBR boundaries conditions between regions are treated

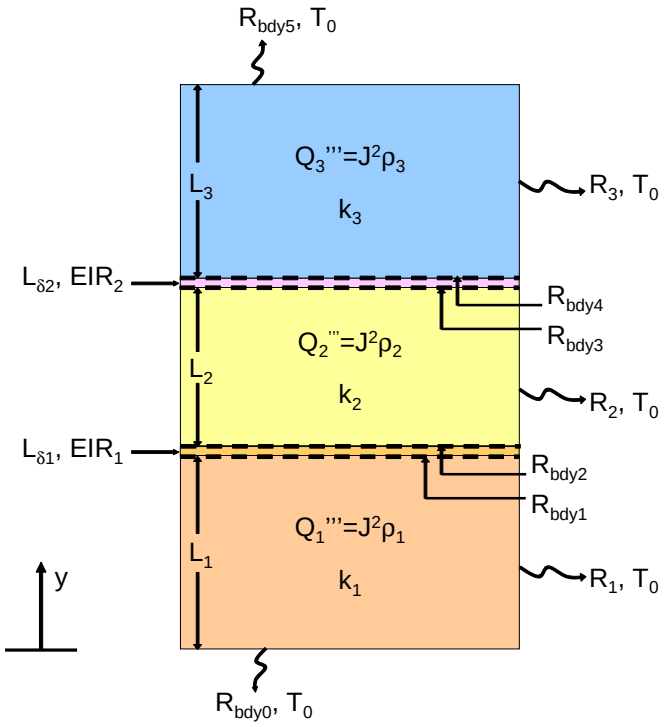

Figure 3.3: Schematic geometry for the thermal fin model

Symbol	Definition	Default value	Unit
Q_i'''	Volumetric heat generation	Varies	$\frac{W}{m^3}$
J	Electrical current density	Varies	$\frac{A}{m^2}$
ρ_i	Electrical resistivity	Chalcogenide: 5.6×10^{-6} Heaters: 3.3×10^{-6}	Ωm
k_i	Thermal conductivity	Chalcogenide: 0.5 Heaters: 17	W/m/K
R_i	Thermal resistance to passivation material	Varies	m^2K/W
$R_{bdy,i}$	Thermal boundary resistances	1×10^{-8}	m^2K/W
L_i	Height of region i	Chalcogenide: 50 Heaters: Sum to 150	nm
$L_{\delta i}$	Width of electrical interface region	1	nm
EIR_i	Electrical interface resistance	1×10^{-12}	Ωm^2
T_0	Ambient temperature	25	°C
ΔT_m	Temperature rise for melting	700	°C

Table 3.1: Description and values of model parameters

using

$$k_i \frac{d\theta_i}{dy} = \frac{1}{R_{bdy,i}} (\theta_{i+1} - \theta_i) \tag{3.13}$$

where $R_{bdy,i}$ is the boundary resistance between regions i and $i+1$. The general solution for temperature rise as a funcitno of position, y, in region i is

$$\theta_i = B_i^1 e^{m_i y} + B_i^2 e^{-m_i y} + \frac{Q_i'''}{k_i m_i^2} \tag{3.14}$$

A matrix vector equation determines the coefficients B_i^1 and B_i^2

$$\mathbf{Mc} = \mathbf{g} \tag{3.15}$$

The vector $\mathbf{c}$ contains the unknown coefficients, B_i^1 and B_i^2. $\mathbf{M}$ has dimensions $2n \times 2n$ where n is the total number of regions in the thermal fin. $\mathbf{M}$ is invertible. Equations 3.14 and 3.15 form the general solution to n thermal fins with arbitrary length, thermal properties, and uniform volumetric heating, connected by resistance interfaces. The entries

of **g** and **M** are given by

$$g_i = \begin{cases} \dfrac{Q'''_1}{R_{bdy,0} k_1 m_1^2} & i = 1 \\ \dfrac{Q'''_{\frac{i-1}{2}}}{R_{bdy,\frac{i-1}{2}} k_{\frac{i-1}{2}} m^2_{\frac{i-1}{2}}} - \dfrac{Q'''_{\frac{i+1}{2}}}{R_{bdy,\frac{i-1}{2}} k_{\frac{i+1}{2}} m^2_{\frac{i+1}{2}}} & i\,odd \\ \dfrac{Q'''_{\frac{i}{2}}}{R_{bdy,\frac{i1}{2}} k_{\frac{i}{2}} m^2_{\frac{i}{2}}} - \dfrac{Q'''_{\frac{i}{2}+1}}{R_{bdy,\frac{i}{2}} k_{\frac{i}{2}+1} m^2_{\frac{i}{2}+1}} & i\,even \\ \dfrac{Q'''_{\frac{i}{2}}}{R_{bdy,\frac{i}{2}} k_{\frac{i}{2}} m^2_{\frac{i}{2}}} & i = 2n \end{cases} \tag{3.16}$$

and

$$i\,odd:\ m_{ij} = \begin{cases} \dfrac{-1}{R_{bdy,\frac{i-1}{2}}} \exp\left[m_{\frac{i-1}{2}} \sum_{p=0}^{\frac{i-1}{2}} L_p\right] & j = i-2 \\ \dfrac{-1}{R_{bdy,\frac{i-1}{2}}} \exp\left[-m_{\frac{i-1}{2}} \sum_{p=0}^{\frac{i-1}{2}} L_p\right] & j = i-1 \\ \left(-k_{\frac{i+1}{2}} m_{\frac{i+1}{2}} + \dfrac{1}{R_{bdy,\frac{i-1}{2}}}\right) \exp\left[m_{\frac{i+1}{2}} \sum_{p=0}^{\frac{i-1}{2}} L_p\right] & j = i \\ \left(k_{\frac{i+1}{2}} m_{\frac{i+1}{2}} + \dfrac{1}{R_{bdy,\frac{i-1}{2}}}\right) \exp\left[-m_{\frac{i+1}{2}} \sum_{p=0}^{\frac{i-1}{2}} L_p\right] & j = i+1 \\ 0 & otherwise \end{cases} \tag{3.17}$$

$$i\,even:\ m_{ij} = \begin{cases} -\left(k_{\frac{i}{2}} m_{\frac{i}{2}} + \dfrac{1}{R_{bdy,\frac{i}{2}}}\right) \exp\left[m_{\frac{i}{2}} \sum_{p=0}^{\frac{i}{2}} L_p\right] & j = i-1 \\ \left(k_{\frac{i}{2}} m_{\frac{i}{2}} - \dfrac{1}{R_{bdy,\frac{i}{2}}}\right) \exp\left[-m_{\frac{i}{2}} \sum_{p=0}^{\frac{i}{2}} L_p\right] & j = i \\ \dfrac{1}{R_{bdy,\frac{i}{2}}} \exp\left[m_{\frac{i}{2}+1} \sum_{p=0}^{\frac{i}{2}} L_p\right] & j = i+1 \\ \dfrac{1}{R_{bdy,\frac{i}{2}}} \exp\left[-m_{\frac{i}{2}+1} \sum_{p=0}^{\frac{i}{2}} L_p\right] & j = i+2 \\ 0 & otherwise \end{cases} \tag{3.18}$$

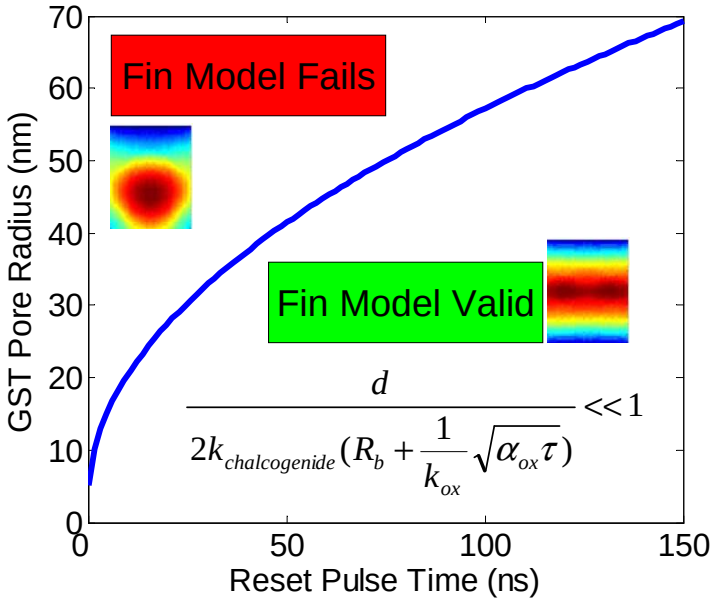

Figure 3.4: Graphical map showing programming regimes where the fin model is valid. R_b is the TBR between the chalcogenide and the surrounding oxide.

3.2.2 Applicability of the Fin Model

The fin model is valid when the cross-sectional temperature is uniform. This is true when the maximum lateral thermal resistance within the fin, R_{lat}, is much smaller than the thermal resistance to ground through the passivation material, R_2. The resistance through the passivation material is approximated in terms of the TBR between the chalcogenide and passivation materials and the diffusion depth for a reset pulse of duration τ. Figure 3.4 shows the combination of contact diameters and reset pulse times for which the model holds, assuming thermal oxide as the passivation material. The model holds for all common confined cell geometries and reset pulse times.

3.3 Results and Discussion

A key benchmark for PCM models is whether they predict the correct reset current for different contact diameters. Figure 3.5 compares experimental data with calculations of

the programming current for each model. All models except the confined resistor are in excellent agreement with the experimental data. The confined cell resistor model predicts the current required to melt the chalcogenide at the heater interface. At this current, the fin model shows the peak temperature is in the bulk of the chalcogenide and it greatly exceeds the melting temperature. Melting begins in the bulk of the chalcogenide, so the predicted current is not the minimum reset current. The fin model predicts nearly identical reset currents for the confined and double confined cells. The predictions agree well with the double confined resistor model. The thermal resistances from the hot spot in each model are approximately equal. This result highlights the key conclusion in equation 3.3: the effective thermal resistance is the critical factor determining reset current in electrically equivalent cells. Optimal cells, therefore, maximize the thermal resistance with respect to a given electrical resistance.

3.3.1 Optimal Geometries for Confined Cells

When the EIR is large compared to the cell's total electrical resistance, the peak temperature occurs at the chalcogenide-heater interface. Equivalently, the heat generated by the interface, $Q_{interface}$, is a significant fraction of the total heat generation, Q_{tot}. Figure 3.6a plots the predicted reset current versus the height ratio: heater height to chalcogenide height. The cell's total electrical resistance is constant for a given $Q_{interface}/Q_{tot}$. Comparison with figure 3.6b shows that the minimum reset current for large $Q_{interface}/Q_{tot}$ ratios occurs at the same height ratio, $\sim$2.3, as the peak thermal resistance value, $R_{th,int}$, as equation 3.3 predicts. As $Q_{interface}/Q_{tot}$ decreases, the location of the peak temperature (i.e. the hot spot) migrates into the volume of the chalcogenide. The thermal resistance from this location, $R_{th,chalc.}$, increases rapidly as the aspect ratio decreases. Correspondingly, figure 3.6a shows that the reset current decreases monotonically as the height ratio decreases.

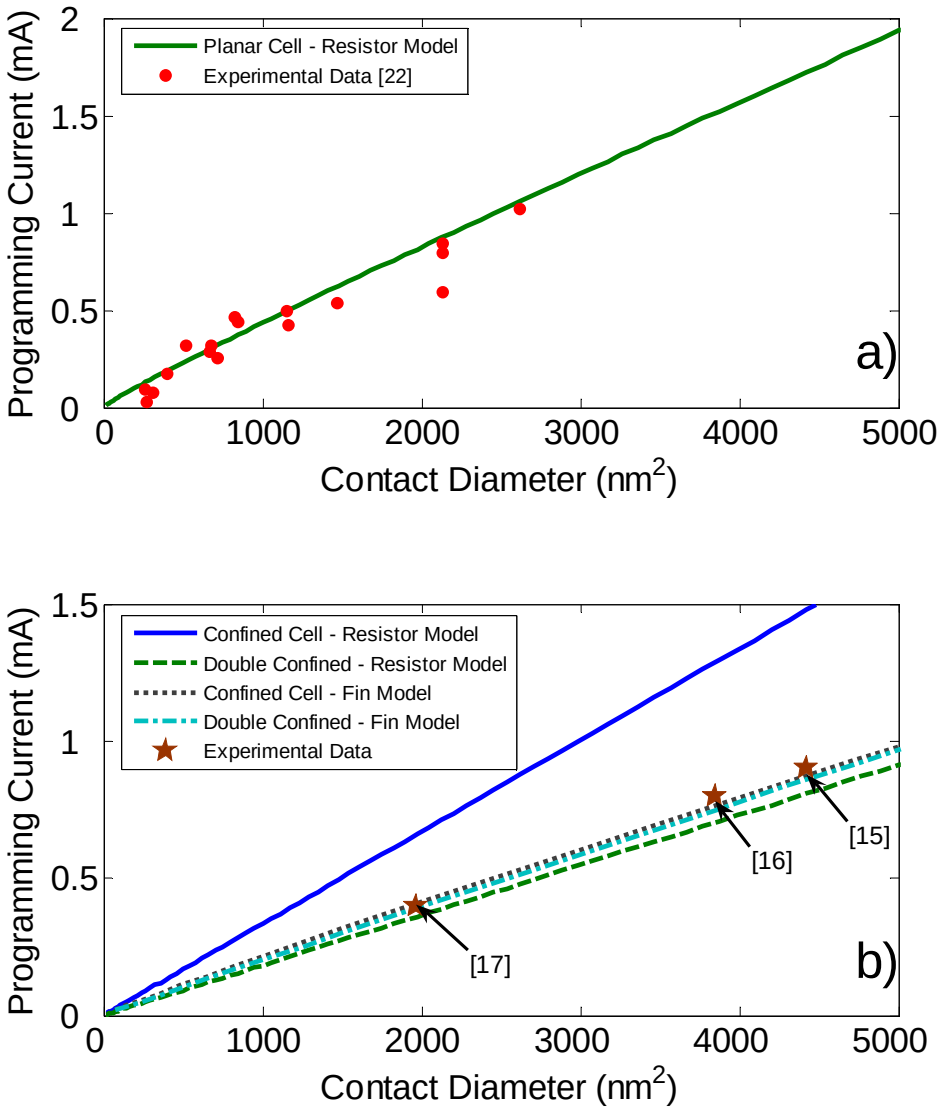

Figure 3.5: Comparison of predicted and experimental reset currents for planar geometry, a), and confined geometries, b).

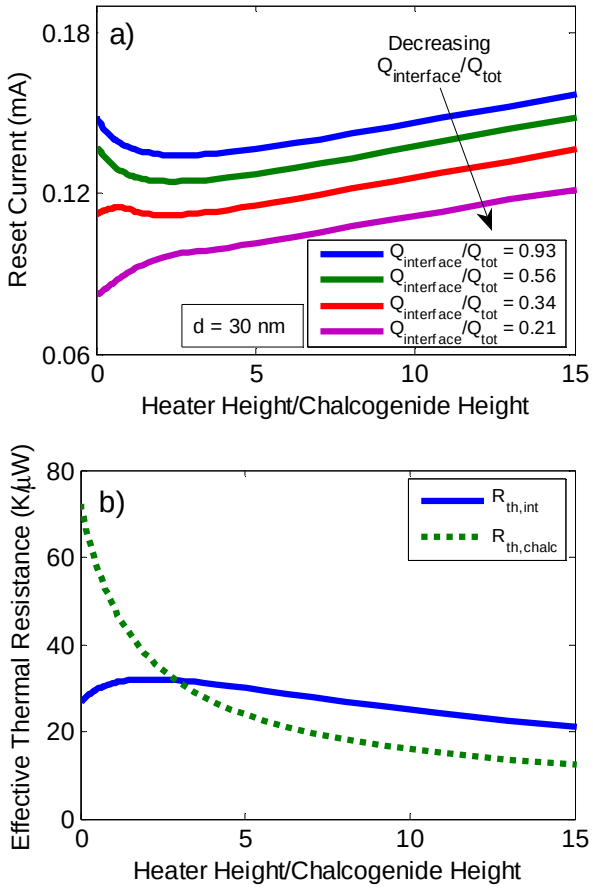

Figure 3.6: The effect of confined cell geometry on the reset current, a), and thermal resistances, b).

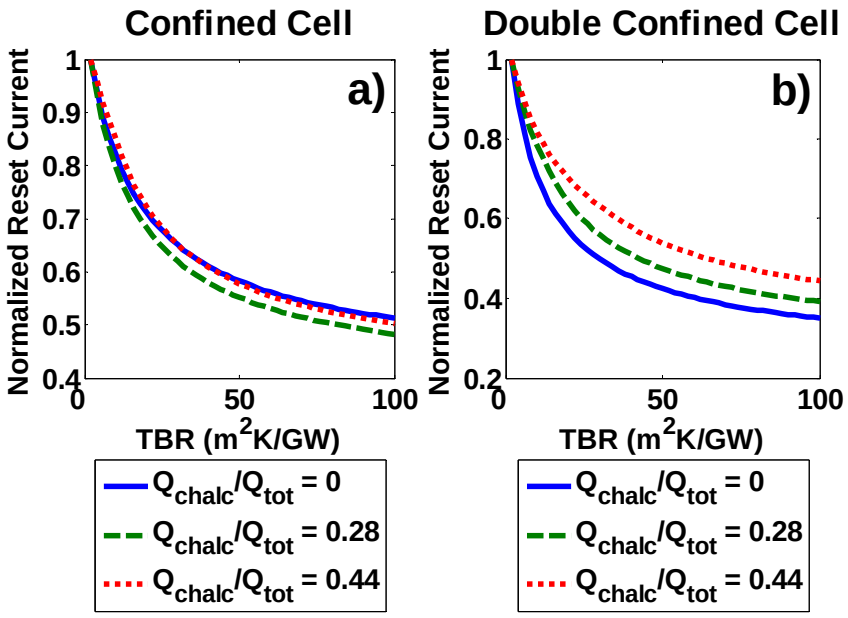

Figure 3.7: The effect of TBR on reset current in confined (a) and double confined (b) cells.

3.3.2 Effect of Thermal Boundary Resistance

Finite element simulations show TBR at the chalcogenide-heater interface strongly affects the temperature profile and reset current in confined cells [30]. Figure 3.7 shows the normalized reset current calculations from the fin model. The TBR spans the range of commonly measured values [30]. A TBR of 100 m^2K/GW is equivalent to the thermal resistance of 50 nm of crystalline GST. Relative to a perfect thermal interface, the calculated reset current decreases by up to $\sim$50% and $\sim$60% in the confined and double confined configurations, respectively. TBR has a stronger effect on reset current in the double confined cell because there are two interfaces impeding heat flow from the hot spot. In confined cells as Q_{chalc}/Q_{tot} increases, the hot spot migrates from the interface toward the center of the chalcogenide where the thermal resistance is at a maximum. Increasing the TBR moves the location with peak thermal resistance toward the interface. Therefore increasing the TBR draws the hot spot toward the interface.

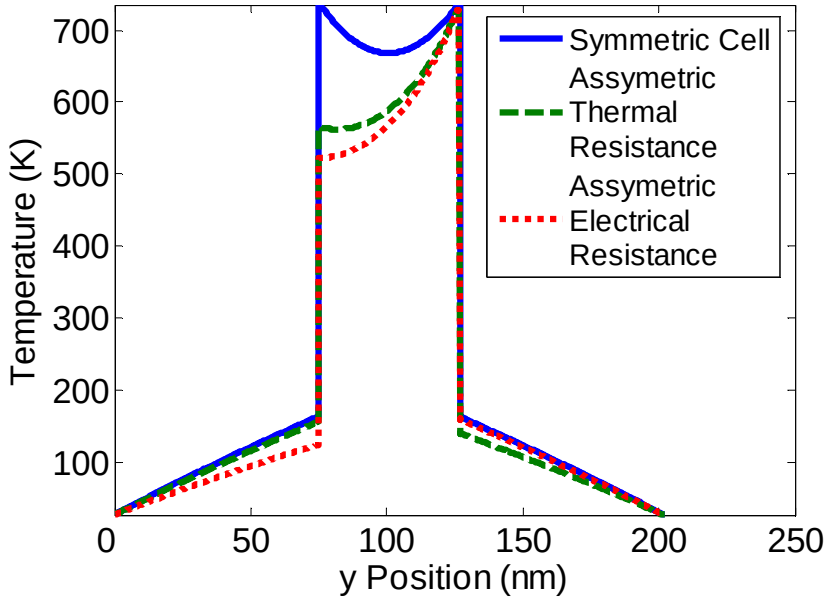

Figure 3.8: Temperature distributions along the length of a double-confined cell. Assymetric distributions of electrical and/or thermal properties allow multiple resistance level programming by changing the magnitude of the programming pulse.

3.3.3 Cell Designs for Multi-level Storage

Multi-level PCM cells store data by changing between several distinct resistance values. The magnitude and duration of the programming current or voltage pulse controls the phase distribution and resistance level. By engineering the distribution of electrical and/or thermal properties in the cell, the magnitude of the voltage or current pulse selects which regions melt or recrystallize. Figure 3.8 shows calculated temperature profiles for three double confined cell configurations with different electrical and thermal resistance distributions. Both interfaces melt at the same reset current level in cells with symmetric thermal and electrical resistance distributions. By increasing the thermal resistance from the chalcogenide to the top electrode, the top interface melts and recrystallizes at a lower current than the bottom interface. The same is true for increasing the electrical interface of the top half of the cell, or, equivalently, increasing the fraction of heat generated in the top half of the cell. The top and bottom interfaces change phase with a slightly higher current pulse. The

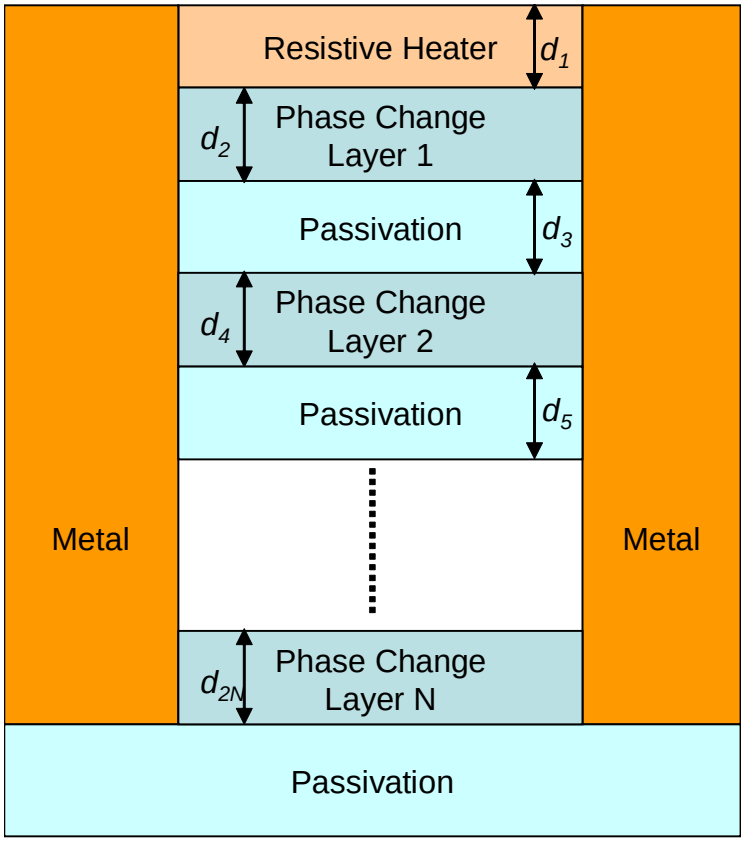

Figure 3.9: Schematic of the proposed multi-level cell

magnitude of the current, therefore, determines the level of the cell. The distinct resistance levels correspond to the phase distribution in the chalcogenide: all crystalline, one amorphous interface, or two amorphous interfaces. One way to modify the electrical and thermal resistances without changing the cell geometry is to engineer the interface properties.

3.3.3.1 Novel Multi-level Design

This section proposes and analyzes a simple multi-level design that offers promising dynamic range and control of an arbitrary number of discrete memory levels. Figure 3.9 shows a schematic of the multi-level cell design for an $N+1$ level cell. The number of melt-quenched amorphous phase change layers dictates the resistance level of the cell. The

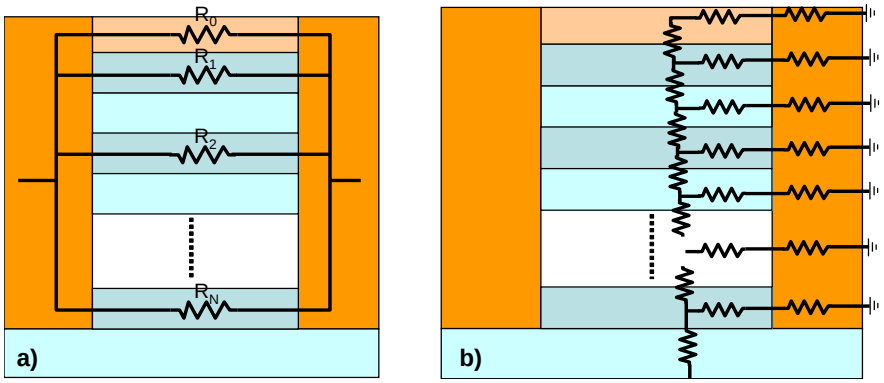

Figure 3.10: Resistance networks for the a) electrical problem and b) thermal problem.

resistive heater and phase change layer thicknesses control the heat generation distribution caused by current, i. The series combination of phase change and passivation layer thicknesses (i.e. thermal resistances) controls the thermal resistance, and, therefore, the temperature gradients required for discrete melting of the layers. Figure 3.10 illustrates approximate thermal and electrical circuits in the device. Equations 3.19-3.21, below, outline an algorithm that calculates layer thicknesses, d_i, required for a given number of resistance levels, $N+1$, with resistance ratio, χ, for given electrical resistivities and thermal conductivities.

$$R_{n+1} = \frac{\chi \prod_{k=0}^{n} R_k}{(1-\chi) \sum_{j=0}^{n} \prod_{\substack{k=0 \\ k \neq j}}^{n} R_k}; \quad d_n = \frac{\rho_n}{R_n} \tag{3.19}$$

$$Q_i = -\frac{1}{R_{i-1,vert}} T_{i-1} + \left(\frac{1}{R_{i-1,vert}} + \frac{1}{R_{i,lat}} + \frac{1}{R_{i,vert}} \right) T_i - \frac{1}{R_{i,vert}} T_{i+1} \tag{3.20}$$

$$\overrightarrow{T} = \mathbf{K}^{-1} \overrightarrow{Q} \tag{3.21}$$

T_j, $R_{j,vert}$, $R_{j.lat}$, and Q_j represent the temperature, thermal resistance in the vertical direction, thermal resistance in the lateral direction, and heat generation at node j. A series of finite element simulations using a stochastic crystallization model, shown in figure 3.11, confirm the validity of the design and analysis algorithm. Figure 3.12 shows the R-I curve predicted by a finite element simulation for a 160 nm wide, 4-level cell with an inter-level resistance ratio of 5. Intermediate resistance levels can be easily programmed due to the

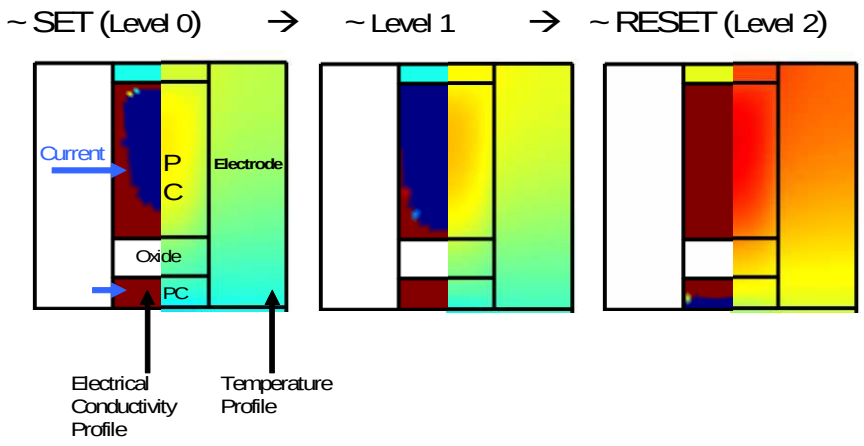

Figure 3.11: Example of electrical conductivity profile and temperature profile during programming to successive resistance levels in a simplified 3 level geometry.

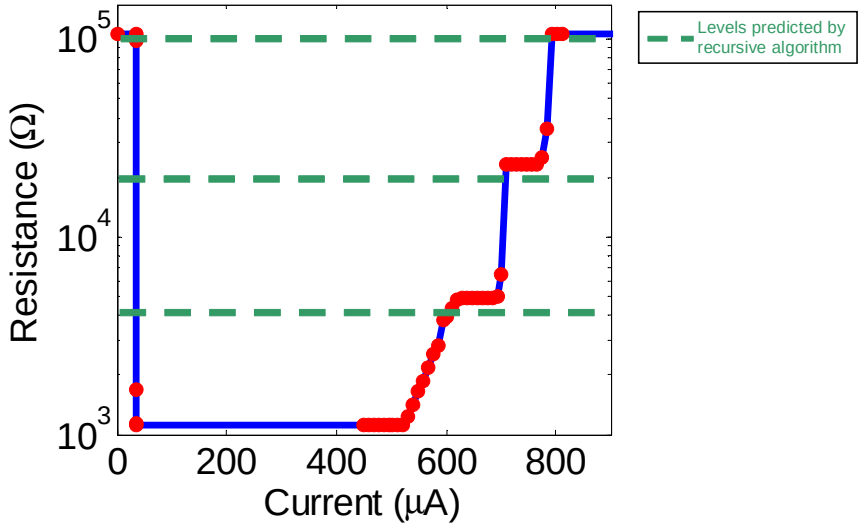

Figure 3.12: R-I curve for a four level cell with logarithmically spaced resistance levels, calculated from multiphysics finite element simulations for a design generated by the recursive algorithm.

large programming current window. The tailored passivation layer thicknesses and thermal properties permit precise control of the temperature profile. By adding a resistive heater, the device does not need to rely on threshold switching, separating it from all previous multi-level designs. The dynamic range of 2-3 orders of magnitude of resistance is limited by the maximum resistance of the resistive heater, and is well within the sensing capabilities of existing memory architectures.

3.4 Summary and Conclusions

This chapter analyzes PCM within the framework of closed form thermal resistance and thermal fin models. It examines three common PCM cell configurations: planar, confined, and double confined. The thermal resistor models provide simple expressions for the relation between effective thermal resistance, effective electrical resistance, contact diameter and reset current. It develops the general solution for a series of n thermal fins of constant cross-sectional area with TBR boundary conditions and arbitrary length, material properties, and Joule heating. Calculations from the fin model show the scaling of reset current with contact diameter, the optimal geometry for confined cells with EIR, and the impact of TBR in confined and double confined cells. It shows the feasibility of multi-level PCM designs through engineering the distribution of thermal and electrical properties.

The effective thermal resistance from the hot spot is the key parameter in predicting the reset current in PCM devices with the same electrical resistance. The heat generation and thermal resistance distributions determine the location of the hot spot. The hot spot must occur at the heater-chalcogenide interface or in the bulk of the chalcogenide in devices with low reset current. In confined cells if the fraction of heating at the interface is large (i.e. large EIR) there is an optimal height ratio of heater to chalcogenide height. This occurs when the effective thermal resistance from the interface is at its maximum. Conversely, if the EIR is small and the chalcogenide resistance large, the hot spot moves to bulk of the chalcogenide. In this case the confined cell exhibits the lowest programming current when the entire pore is filled with chalcogenide, since this maximizes the thermal resistance. TBR can be a significant fraction of the effective thermal resistance. It plays a key role in cell design by reducing the reset current and changing the location of the hot spot.

Interface engineering is a promising way to improve PCM cell performance. By tailoring the EIR and the chalcogenide resisitivity it is possible to control the location of the hot spot. Reliability in confined cells depends on reducing heater-chalcogenide interface reactions. Reducing the ratio of EIR to chalcogenide resistance moves the hot spot into the bulk of the chalcogenide which may reduce interface reactions and improve reliability in confined cells. TBR can be increased by adding interface layers with highly mismatched Debye temperatures [37]. The TBR and EIR are not completely independent of each other. Optimizing PCM cells depends on understanding their interdependence and improving understanding of electrothermal interactions such as the Thomson effect. This chapter provides design tools for considering these and myriad other physical effects in insightful ways.

Chapter 4

Thickness and Stoichiometry Dependence of the Thermal Conductivity of GeSbTe Films

The increasing emphasis on phase change memory device scaling and optimization of phase change materials strongly motivates the need for thorough understanding of their thermal properties. This chapter presents the thickness and temperature dependent thermal conductivity of $Ge_2Sb_2Te_5$ (GST) between 25°C and 340°C in the as-deposited, face-centered cubic (fcc) and hexagonal close packed (hcp) phases. It also provides conductivity and phase transition data for films with stoichiometry variations ranging from GeTe to $Ge_2Sb_2Te_5$.

4.1 Nanosecond Transient Thermoreflectance

Nanosecond laser heating and laser-reflectance thermometry measure the effective thermal conductivity of metal coated phase change layers between 60 and 400 nm thick, deposited on a silicon substrate. A 6 mm diameter, 532 nm wavelength, 6 ns pulse from a Nd:YAG laser heats the metal film surface. A 10 mW, 637 nm wavelength, ~10μm diameter probe beam is focused on the heated portion of the surface[76]. The apparatus is similar to that depicted in figure 1.6. The relative temperature dependent changes in reflectivity yield the

normalized surface temperature with sub-microsecond temporal resolution [76]. Because the heated region is much larger than the probe beam, sample thickness, and diffusion depth, we solve the 1D heat diffusion equation in the layered structure assuming a semi-infinite substrate. Fitting the analytical solution of the heat diffusion equation to the measured temperature response extracts the effective thermal conductivity of the phase change layer in the cross-plane direction.

4.2 Sample Preparation and Material Characterization

Samples for the temperature and thickness dependent measurement are prepared by RF-sputtering $Ge_2Sb_2Te_5$ films of thickness near 60 nm, 120 nm, and 350 nm films on Si wafers using an AJA International, ATC 1800-F sputtering tool. A $\sim$ 120 nm Au layer deposited on the phase change film via e-beam evaporation provides the high optical reflectivity at the pump and probe wavelengths required by the thermoreflectance technique. No adhesion layer is deposited between the Au and GST films.

To study the stoichiometry dependence of thermal conductivity and phase transition temperature, six layers of varying stoichiometry are deposited on Si wafers using the ATC 1800-F sputtering tool. GeTe and $Ge_2Sb_2Te_5$ targets are co-sputtered to produce the following compositions, measured using X-ray photoemission spectroscopy: GeTe, $Ge_{0.41}Sb_{0.07}Te_{0.52}$, $Ge_{0.31}Sb_{0.14}Te_{0.55}$, $Ge_{0.25}Sb_{0.20}Te_{0.55}$, $Ge_{0.22}Sb_{0.24}Te_{0.54}$, $Ge_2Sb_2Te_5$. An $\sim$ 80 nm aluminum film deposited via RF-sputtering in the same system enables the thermoreflectance measurement.

Figure 4.1 shows cross section images of the $\sim$ 60 nm as-deposited and hcp films taken via scanning electron microscopy. X-ray diffraction measurements confirm the phase transition from as-deposited to fcc at $\sim$ 130°C and the transition from fcc to hcp at $\sim$ 200°C, consistent with results from Yamada et al. [124] The hcp phase shown in figure 4.1 was obtained by annealing the as-deposited sample at 340°C for 20 minutes. The images show a thickness decrease from 65 nm to 60 nm in the transition from the as-deposited to hcp phases. We attribute the reduction in thickness to the increase in density of the crystallized material. Wiedenhoff et al. [125] reported similar density increases of 6.2% ± 0.8% in the

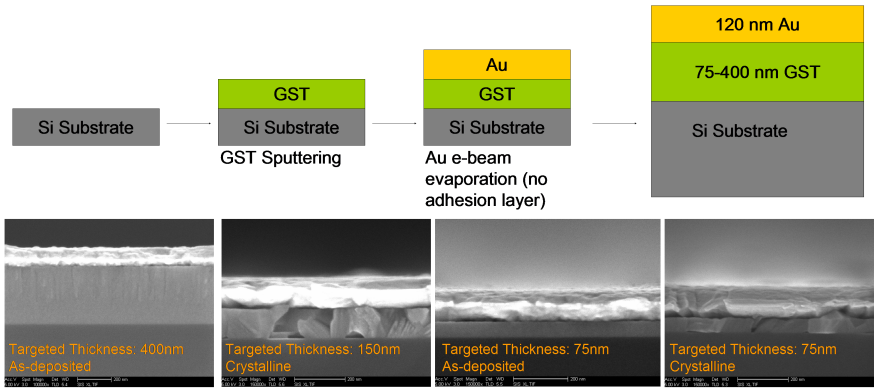

Figure 4.1: Fabrication process and cross-section images of a sample in the as-deposited and crystalline phases taken by scanning electron microscope.

transition from as-deposited to crystalline phases of $Ge_2Sb_2Te_5$. Kim et al. [29] and Giraud et al. [67] reported similar fractional changes in thickness upon crystallization.

4.3 Thickness and Temperature Dependence of the Thermal Conductivity of $Ge_2Sb_2Te_5$

Figure 4.2 shows the effective thermal conductivity as a function of temperature, phase, and GST layer thickness. For the 350 nm thick sample, at room temperature, we measure thermal conductivities of 0.29, 0.42, and 1.76 W/m/K in the as-deposited, fcc, and hcp phases, respectively. The room temperature thermal conductivities for the $\sim$ 60 nm film are 0.17, 0.28 and 0.83 W/m/K in the respective phases. These values are similar to previously reported values which vary from 0.17-0.34, 0.26-0.95, and 1.40-1.57 W/m/K in the respective phases [29, 67, 59, 57].

The average relative errors across all thicknesses are 7.2%, 8.7% and 9.3% for the as-deposited, fcc, and hcp phases, respectively. We attribute the increases in error with increasing thermal conductivity to the increased relative significance of the measurement noise.

The thickness variation of the thermal conductivity can be due to boundary resistances and variations in microstructural quality. This can be investigated using a simple model

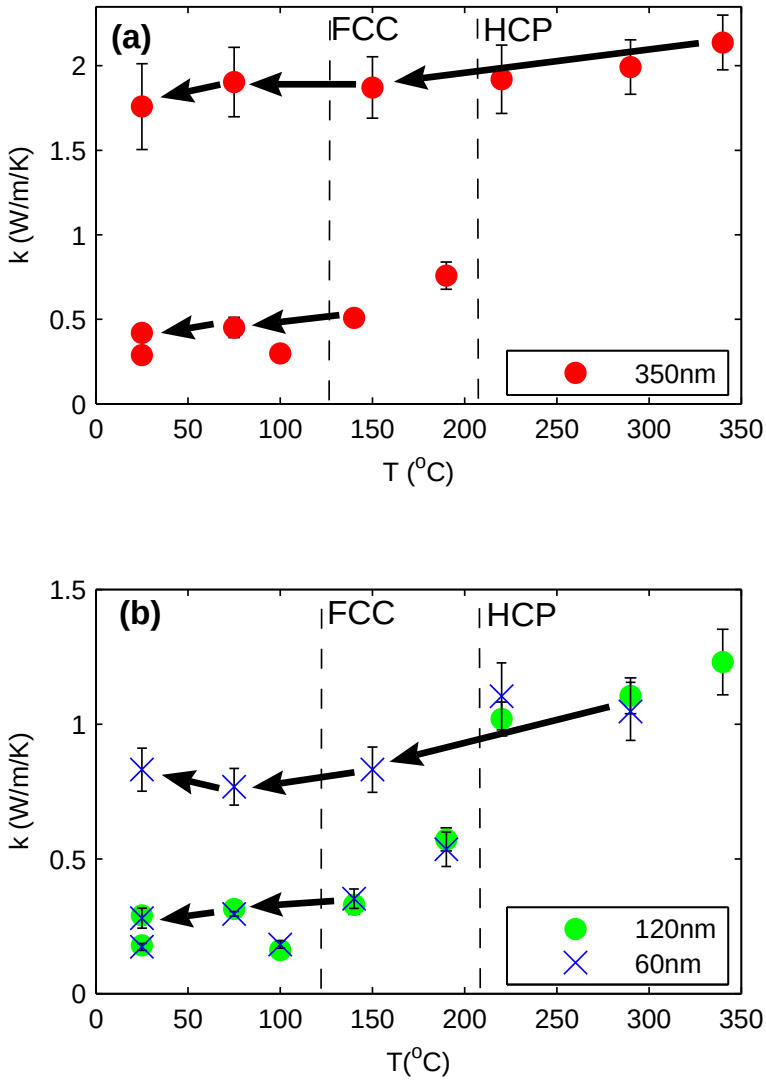

Figure 4.2: The effective thermal conductivity of $Ge_2Sb_2Te_5$ versus temperature for (a) $\sim$ 350 nm and (b) $\sim$ 60 and 120 nm films. The dashed lines indicate the phase transition temperatures. Arrows show the temperature hysteresis due to phase change, measured by ramping the temperature back to room temperature after heating to 150°C and, subsequently, to 340°C.

that separates a minimum internal resistance, R_{int}, from the boundary resistance, R_B, and the extra internal resistance due to microstructural defects, $R_{defects}$

$$R_{net} = R_{int} + R_{defects} + R_B \tag{4.1}$$

Assuming the internal thermal conductivity, k_{int}, is independent of layer thickness, equation 4.1 may be rewritten as

$$\frac{d}{k_{eff}} = \frac{d}{k_{int}} + R_{defects} + R_B \tag{4.2}$$

where d is the layer thickness and k_{eff} is the measured effective thermal conductivity. The assumption that k_{int} is independent of thickness is justified when the layer thickness is much greater than the heat carrier mean free path, which is satisfied here[29].

In this model the local slope of $1/k_{eff}$ vs. $1/d$ indicates the combined magnitude of boundary and defect resistances, R_B and $R_{defects}$. When analyzed assuming a thickness independent boundary resistance, the data show a non-linear dependence on $1/d$, indicating that the microstructural contributions to the thermal resistance are thickness dependent, as seen in figure 4.3. Characteristic magnitudes of the slope for the as-deposited and hcp phases are 10^{-7} m^2K/W and 10^{-8} m^2K/W, respectively, with values in the fcc phase lying between these limits. The slope for the as-deposited phase is larger than previously measured values for thermal resistances while the slope for the hcp phase is of similar magnitude to measured values [51, 29]. These observations suggest that interface resistance alone cannot account for the thickness dependence of the effective thermal conductivity. The decreased magnitude of the slope after crystallization and annealing may be caused by reduction in the quantity of interface defects, and enhanced physical contact and adhesion due to annealing.

4.4 Stoichiometry Dependence of the Thermal Conductivity of Chalcogenides

Figure 3 shows the effective thermal conductivity of layers of six stoichiometric compounds produced by co-sputtering GeTe and $Ge_2Sb_2Te_5$. The effective thermal conductivity of

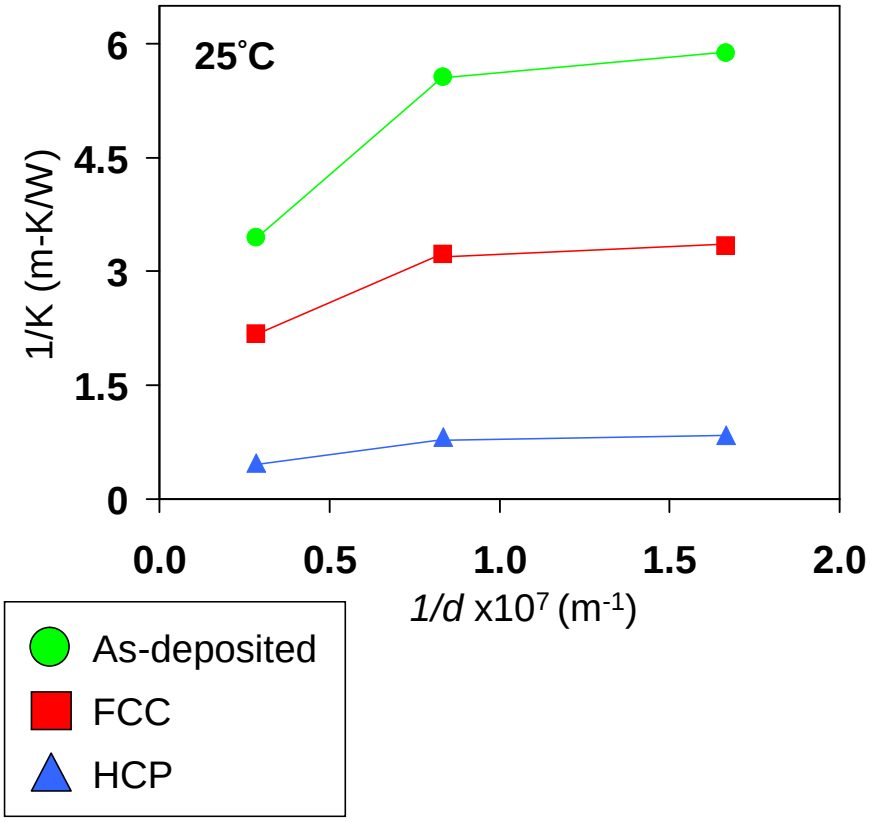

Figure 4.3: Thickness dependence of the effective thermal conductivity of GST.

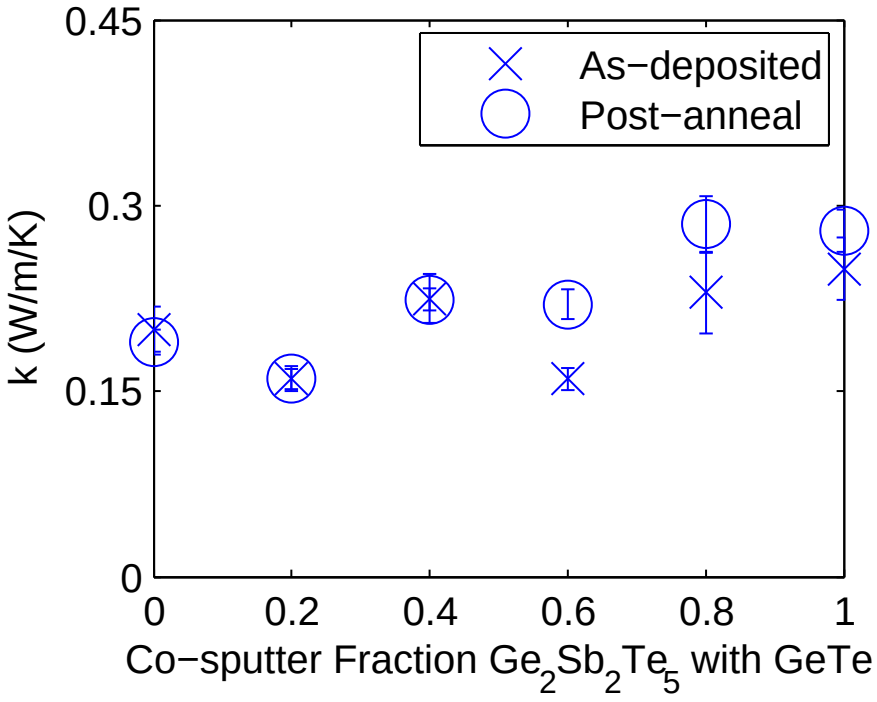

Figure 4.4: The effective thermal conductivity at 75°C of six stoichiometric compounds in the as-deposited phase and after annealing at 150°C for 15 minutes. Compounds are produced by co-sputtering $Ge_2Sb_2Te_5$ with GeTe. $Ge_2Sb_2Te_5$ and the two compounds closest in stoichiometry crystallized during annealing, leading to larger values of thermal conductivity. SEM images show thicknesses of the as-deposited samples vary between 235 and 413 nm.

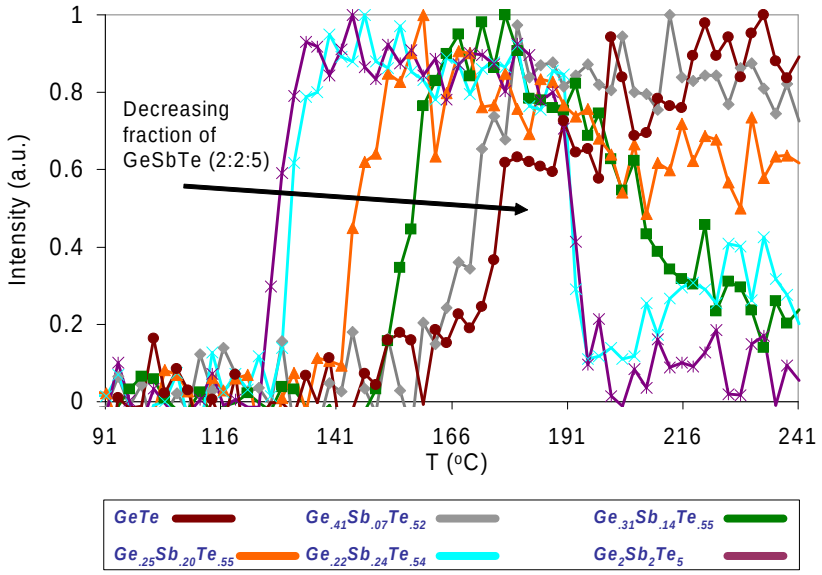

Figure 4.5: Relative intensity of the first crystalline peak as a function of annealing temperature and stoichiometry. [14]

all compounds in the as-deposited phase is between 0.16 and 0.25 W/m/K with relative errors between ±5.0% and ±14.3%. X-ray diffraction measurements of $Ge_2Sb_2Te_5$ and the two compounds of closest stoichiometry confirm these samples crystallized after a 15 minute 150°C anneal. Compared to the as-deposited phase, the crystalline compounds exhibit larger thermal conductivities of 0.22, 0.29, and 0.28 W/m/K for $Ge_{0.25}Sb_{0.20}Te_{0.55}$, $Ge_{0.22}Sb_{0.24}Te_{0.54}$, and $Ge_2Sb_2Te_5$, respectively. Figure 4.5 [14] shows the intensity of the first crystalline peak as a function of annealing temperature and stoichiometry.

Table 4.1 shows the crystallization temperature and as-deposited thickness for each of the six compounds. The phase transition temperature from as-deposited to crystalline increases monotonically as the fraction of Sb decreases in the compound. This is consistent with calculations by Lankhorst [48], that predict transition temperatures increase with increasing bond enthalpies and coordination numbers. This suggests the decrease in transition temperature is due in part to the three-fold coordination of Sb relative to the four-fold coordination of Ge in the amorphous material.

Composition	Targeted $Ge_2Sb_2Te_5$ co-sputter fraction	As-deposited thickness (nm)	First as-deposited to cystalline transition temperature (°C)
GeTe	0	327	180
$Ge_{0.41}Sb_{0.07}Te_{0.52}$	20%	235	171
$Ge_{0.31}Sb_{0.14}Te_{0.55}$	40%	400	158
$Ge_{0.25}Sb_{0.20}Te_{0.55}$	60%	268	146
$Ge_{0.22}Sb_{0.24}Te_{0.54}$	80%	345	131
$Ge_2Sb_2Te_5$	100%	413	121

Table 4.1: Measured compositions, targeted co-sputter fraction of $Ge_2Sb_2Te_5$, thicknesses, and phase transition temperatures for the six stoichiometric compounds.

4.5 Summary and Conclusions

In summary, these results illustrate the temperature, phase, and thickness dependence of the effective thermal conductivity of $Ge_2Sb_2Te_5$ layers. The data show that a fixed thermal interface resistance alone cannot explain the trends in thickness dependence, though it may be the most significant factor in the thickness dependence of annealed and crystallized films. Additionally, the thermal conductivity of the as-deposited phase does not depend strongly on stoichiometry for compounds varying between GeTe and $Ge_2Sb_2Te_5$. The phase transition temperatures, however, may be tailored by changing the fraction of Sb in the phase change material. The increase in the thermal conductivity in the crystalline phases corresponds to the bonding configuration of the Ge atom in the phase change material. When the Ge flips from an octahedral interstitial to a tetrahedral site [119], it forms strong covalent bonds with neighboring Te atoms that support higher vibrational frequencies, a greater sound velocity, and, therefore, an increase in the phonon contribution to the thermal conductivity in the crystalline phases consistent with the findings reported in this chapter.

Chapter 5

Thermal Boundary Resistance Measurements for Phase Change Memory Devices

This chapter develops picosecond time-domain thermoreflectance (TDTR) [79] measurements for the fcc $Ge_2Sb_2Te_5$ (GST) intrinsic thermal conductivity, and the TiN/GST and Al/TiN thermal boundary resistances (TBR) between room temperature and 325°C. In phase change memory (PCM) devices, the phase change material temperature reaches up to 700°C during the phase transitions [30], necessitating temperature dependent data for the spatial distribution of thermal resistances. Write current reduction remains a challenge for decreasing the size of programming transistors. Programming pulses contain $\sim$1000 times more energy than is required for the phase transitions. Heat conduction through the bottom electrode, commonly made of TiN, dissipates most of the excess energy [30, 122]. Understanding the conduction physics in thin TiN and GST films and at their interfaces is therefore essential for improved PCM device engineering and simulation [32, 30, 37].

5.1 Picosecond Time-Domain Thermoreflectance

The picosecond time-domain thermoreflectance (TDTR) system measures the spatial distribution of thermal properties on the nanometer length scale. A pump beam rapidly (<10 ps)

heats the surface region of a metal-coated thin film of interest. At a controlled delay time, a co-aligned probe beam strikes the sample. The reflected intensity of the probe beam measures the relative surface temperature of the metal. By sweeping through a range of delay times, the system measures the thermal decay of the metal film. Thin film thermal conductivities (cross-plane and in-plane) and thermal boundary resistances can be determined uniquely by fitting the thermal decay data to a 3-D frequency-domain analytical solution of the heat diffusion equation [79]. Other thermal metrology techniques such as nanosecond thermoreflectance [27], and 3ω [29] resolve spatially averaged thermal properties, typically providing only indirect measurements of TBR. In contrast, picosecond TDTR can uniquely separate the TBR from intrinsic thermal resistance.

A mode-locked Nd:YVO4 laser produces 9 ps pulses at wavelength λ =1064 nm with a repetition rate of 82 MHz. The pump beam passes through an electro-optic modulator (EOM) operating at up to 50 MHz. In this work, the EOM frequency is 8 MHz to maximize sensitivity to the desired thermal properties. The reflected intensity of the probe beam varies at the modulation frequency and is measured and normalized using photodiodes and a lock-in amplifier. A mechanical delay stage and retro-reflector delay the probe beam relative to the pump over a temporal range of ∼3.5 ns. Beam modulation and the single-mode fiber (SMF) significantly increase measurement accuracy by improving beam quality and reducing beam walking at long delay times. The reflected intensity of the probe beam measures the sample surface temperature decay. The 19 mW, 10.0 μm $1/e^2$ diameter pump and 10 mW, 5.0 μm $1/e^2$ diameter probe beams cause instantaneous and steady temperature rises less than 6°C and 1.5°C, respectively, for a reflectance of $\sim$ 0.9 [80]. Figure 1.7 depicts the TDTR setup used in this work.

5.2 Sample Preparation

Four TiN/GST/TiN stacks were produced by physical vapor deposition (PVD) on Si substrates at 135°C. Figure 5.1 shows scanning electron microscope (SEM) images of two of the TiN/GST/TiN stacks. Table 5.1 lists the sample geometries. TDTR requires the top metal be opaque at the pump and probe wavelengths, so ∼53 nm of Al was evaporated on

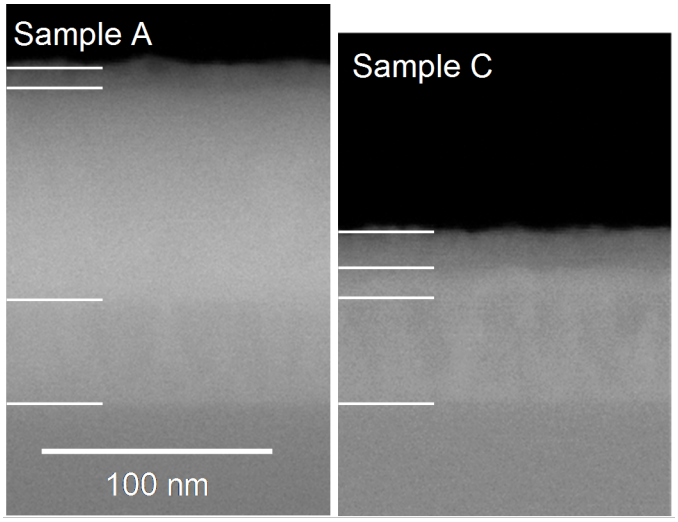

Figure 5.1: Cross-sectional scanning electron microscope (SEM) images of two measured samples. From the top, the layers are TiN, fcc GST, TiN, Si. $\sim$ 53 nm layers of Al were evaporated on these structures and measured using atomic force microscopy (AFM) after the SEMs were taken. The white lines are intended as a guide for distinguishing between layers.

	Aluminum	Top TiN Layer	GST	Bottom TiN Layer
Sample A	52.5 nm	10.8 nm	91.4 nm	45.1 nm
Sample B	52.5 nm	10.3 nm	51.9 nm	47.3 nm
Sample C	52.5 nm	15.7 nm	14.0 nm	44.5 nm
Sample D	52.5 nm	17.4 nm	6.5 nm	47.4 nm

Table 5.1: Thin-film geometries for different samples. The sample geometry is Al/Top TiN/GST/Bottom TiN/Si substrate.

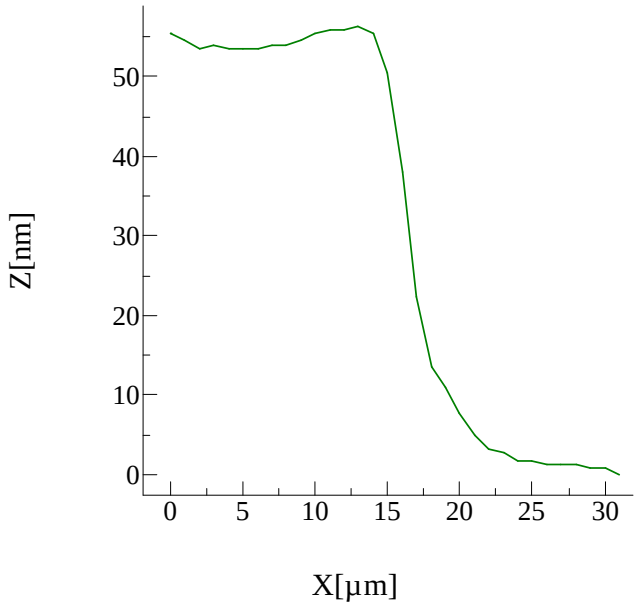

Figure 5.2: AFM topographic profile of the Al film height.

the exposed TiN surface after an extended air break. Atomic force microscopy (AFM) measurements over a masked region determine the Al thicknesses. Figure 5.2 shows a typical AFM topographic profile over the edge of the masked region. The thickness uncertainties are +/- 2.5 nm for the Al films and +/- 1.5 nm for the TiN and GST films.

5.3 Multi-sample Thickness-Implicit Data Extraction

A transient 3-D multi-layer frequency domain solution to the heat diffusion equation [79] models the measured thermal decays. A nonlinear least-squares curve fitting algorithm finds the TiN/GST TBR, Al/TiN TBRs, and intrinsic GST conductivity that simultaneously optimizes the curve fits for all four samples. Data are fit using GST heat capacity data from [126]. Figure 5.3 shows representative data and curve fits for each sample from the final measurement at 30°C. The fits are insensitive to the initial guess. To reduce the influence of random noise we average ten traces for each sample at every temperature and normalize by the average value between 100-115 ps. Data are fit over the range 100-3500 ps.

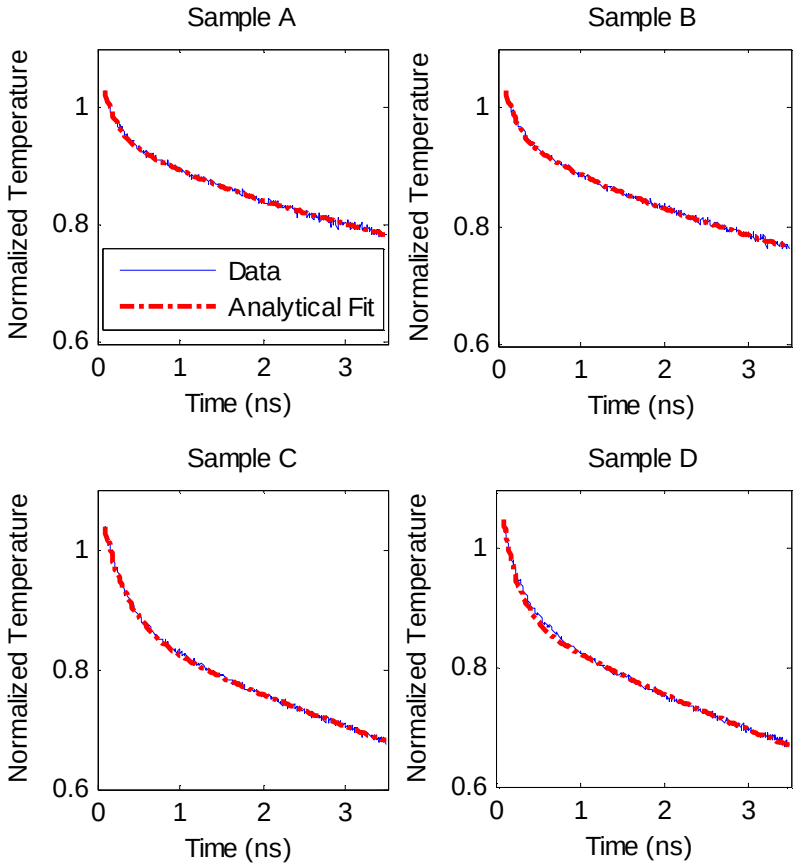

Figure 5.3: Representative thermal traces and data fits at 30°C for each of the four samples. Each thermal decay trace is the average of 10 traces.

The metal's thermal diffusion time, τ, due to the Al/TiN boundary is $\tau \sim R_{b,Al/TiN}C$ where $R_{b,Al/TiN}$ is the Al/TiN TBR and C is the thermal mass of the Al layer. At times less than $\tau \sim 650$ ps, the thermal decay is highly sensitive to the Al/TiN TBR and minimally sensitive to other thermal properties. This permits unique fitting of the Al/TiN TBR in each sample. Figure *** a) and b) show analytical solutions for sample A with varying Al/TiN TBR showing that this TBR only affects the short time curvature of the solution. At long times, t > 2000 ps, the influence of the Al/TiN resistance is small compared to the underlying films' thermal impedances. The sample geometry determines the relative sensitivities to the TiN/GST TBR and intrinsic thermal conductivity. For example, the intrinsic GST conductivity dominates the response of sample A since heat does not diffuse entirely through the GST film during the measurement time range. Samples C and D show sensitivity to both the TiN/GST TBR and intrinsic thermal conductivity since heat diffuses through the entire stack at the characteristic measurement time scale. Figure 5.5 shows how the long time behavior of sample A depends almost exclusively on the GST intrinsic thermal conductivity while sample C is sensitive to both the intrinsic GST conductivity and the TiN/GST TBR. Unique extraction of the TiN/GST TBR is possible under the assumption that the intrinsic GST conductivity and TiN/GST TBR are the same in all samples.

5.4 Temperature Dependence of the Thermal Boundary Resistance

Figure 5.6 shows the fitted Al/TiN TBR, GST/TiN TBR, and intrinsic GST thermal conductivity as a function of temperature between 30°C and 325°C. The Al films cracked and the GST films sublimated near 350°C, preventing measurements at higher temperatures. Other metals, such as W, also cracked at high temperature and exhibited smaller signal-to-noise ratios and nonthermal responses at short times, similar to those in [127]. The measurement time at each temperature was 30 min. +/- 5 min. The intrinsic GST thermal conductivity values between 0.44 and 0.59 W/m/K agree well with previous fcc phase measurements [27, 29, 59, 67]. The glass-like temperature dependence of the thermal conductivity, which roughly tracks the temperature dependence of the heat capacity, is likely due to the large

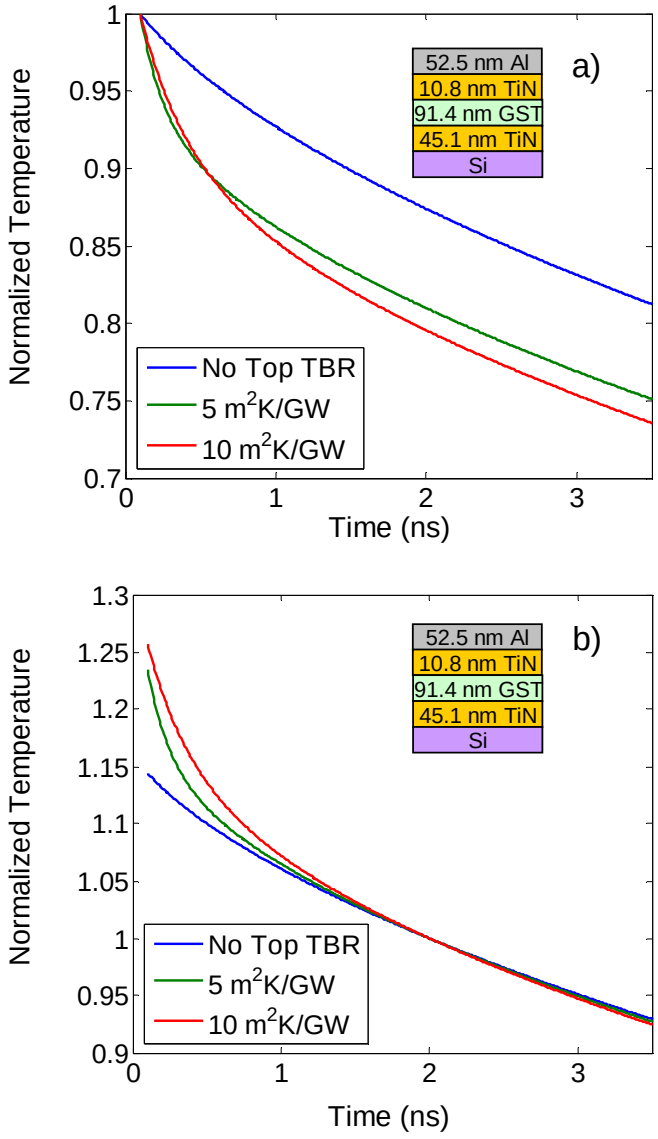

Figure 5.4: The effect of the Al/TiN TBR on the thermal response of sample A, normalized around a) 100 ps and b) 2000 ps. By normalizing at a time unaffected by the Al/TiN TBR, b) demonstrates that the first TBR has negligibly impacts the long time behavior of the thermal decay.

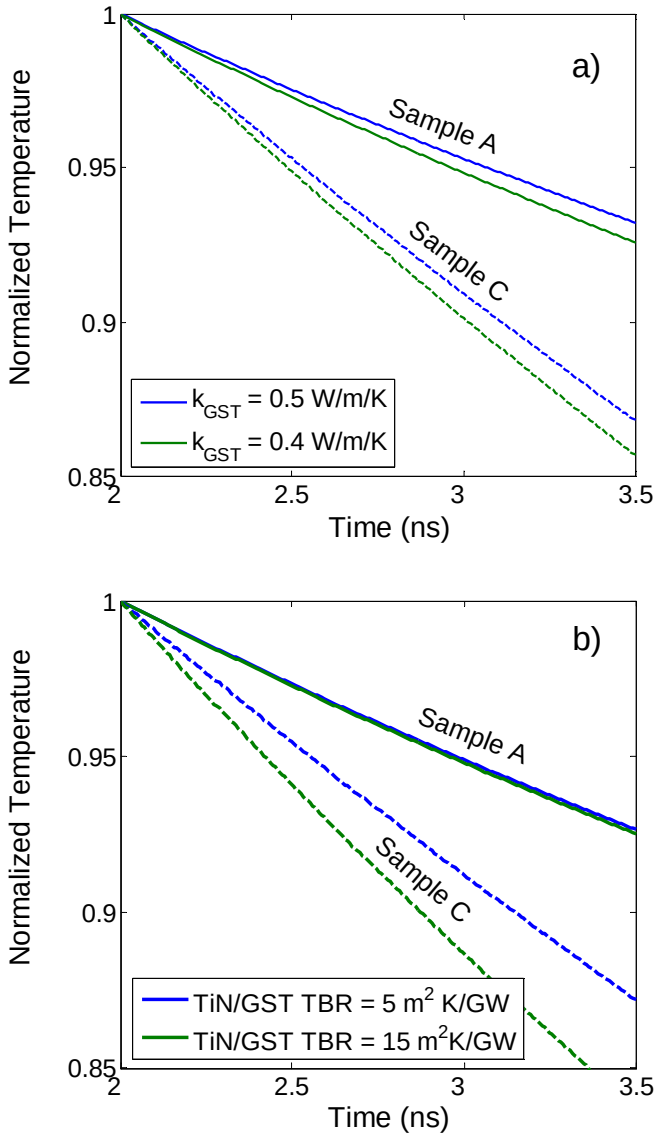

Figure 5.5: Long time sensitivity to different thermal properties. a) shows that samples A and C are both sensitive to the intrinsic thermal conductivity. b) shows that sample A is insensitive to the TiN/GST TBR, while C is highly sensitive to this parameter.

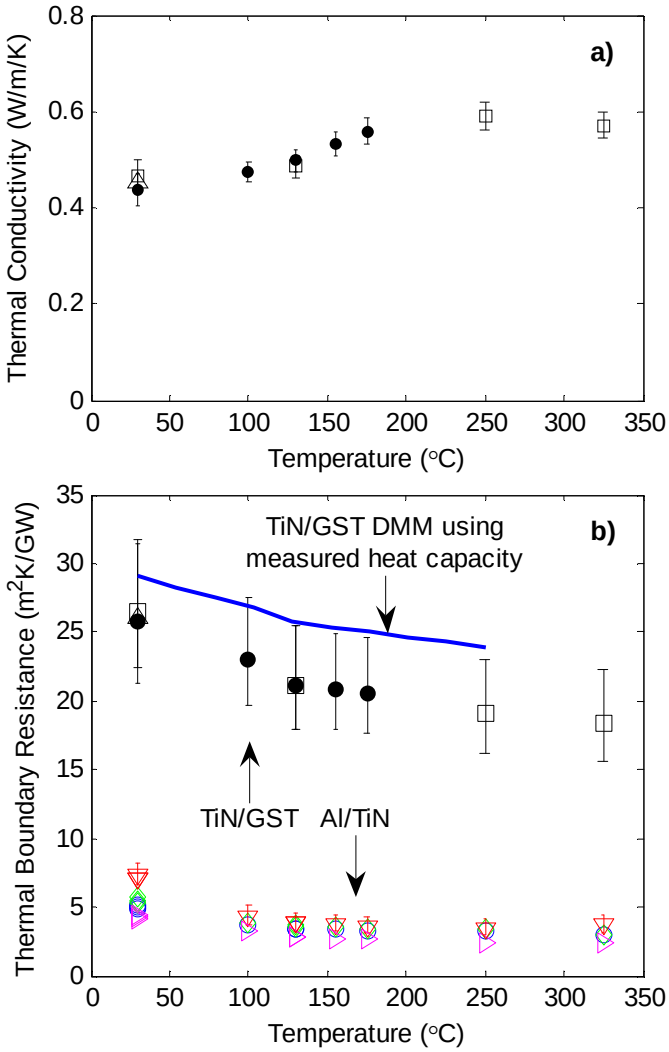

Figure 5.6: The GST intrinsic thermal conductivity, a), and TiN/GST and Al/TiN TBR, b). For the GST intrinsic conductivity and TiN/GST TBR, filled circles indicate measurements from the initial temperature ramp between 30°C to 175°C, hollow squares indicate measurements after ramping back to 30°C then up to 325°C, and the hollow upward pointing triangle indicates the final measurement after ramping back to 30°C. The hollow circle, diamond, downward, and rightward facing triangles indicate the Al/TiN TBR for samples A, B, C, and D, respectively. For clarity, error bars are shown only for sample C. Al/TiN TBR errors are similar for other samples.

vacancy and interstitial concentration in fcc GST [59]. The data do not show hysteresis with annealing, suggesting that irreversible changes in defect density are not significant in our films, in contrast to [59]. This may be due to the higher deposition temperature of our films. The TiN/GST TBR varies between $\sim$ 26 m^{2}K/GW and 18 m^{2}K/GW. A TBR of 10 m^{2}K/GW is approximately equivalent to the thermal resistance to 192 nm of TiN. The Al/TiN TBR varies between $\sim$7 m^{2}K/GW and 2.3 m^{2}K/GW. Different levels of oxidation, contamination, and roughness explain the difference in Al/TiN values between samples.

We use nanosecond transient thermoreflectance (TTR) [27] to measure the room temperature effective thermal conductivity, k_{eff}, of $\sim$ 60, 100, and 120 nm layers of PVD TiN on Si, coated with $\sim$ 500 nm PVD Ti. By modeling the data as thermal resistors in series [29], the relation $1/k_{eff} = 1/k_{int,TiN} + 2R_{b,avg}/d$ determines the intrinsic TiN conductivity, k_{int} = 19.2 W/m/K, and the average of the Ti/TiN and TiN/Si TBRs, $R_{b,avg}$ = 11.8 m^{2}K/GW, where d is the TiN layer thickness. The error bars in figure 5.6 account for the thickness uncertainties, +/-50% variation in $k_{int,TiN}$ [101], and TiN/Si TBRs between 0 and 11.8 m^{2}K/GW.

5.4.1 Thermal Boundary Resistance Modeling

Phonons dominate thermal transport in fcc GST [127] and high-resistivity PVD TiN films. The acoustic mismatch (AMM) and diffuse mismatch models (DMM) describe TBR as the partial transmission of phonons across an interface [53]. While many variations of these models exist [91], the DMM using the measured heat capacity,

$$R_b = \left(\frac{\alpha_{1-2}}{12} c_{1,D}^3 \sum_j c_{1,j}^{-2} \right)^{-1} C_1 (T)^{-1} \tag{5.1}$$

best represents the data, where R_b is the TBR, $C_1(T)$ is the measured heat capacity of material 1 at temperature, T, and $c_{i,j}$ is the velocity of phonon mode j in material i [91]. Figure 5.6 shows this model slightly over-predicts the data but captures its temperature trend. It estimates the Al/TiN TBR as $\sim$0.3 m^{2}K/GW at 30°C. The large disagreement between the model and the measured value of the Al/TiN TBR is likely due to impurity adsorption and

oxidation during the air break between the Al evaporation and the initial deposition. Materials with dissimilar Debye temperatures, (i.e. large acoustic mismatch), have larger TBRs, which explains the difference in the TiN/GST and Al/TiN TBRs. Acoustically mismatched phase change and electrode materials should, therefore, provide better thermal insulation of the PCM programming region. The Debye temperature of fcc GST, is $\sim$100 K [89] while the Debye temperature of TiN is $\sim$ 557 K [128]. Stiff materials with low density such as carbon nanotubes have the highest Debye temperatures, up to $\sim$2000 K [129].

The AMM and DMM predict constant TiN/GST TBR at device operating temperatures. The data show decreasing TBR with temperature for both TiN/GST and Al/TiN interfaces. Lattice dynamics calculations on Lennard-Jones solids predict decreasing TBR up to the melting point [96]. Recent experimental work attributes a $1/T$ dependence of the TBR to anharmonic phonon processes [115]. Assuming a $1/T$ temperature dependence coincident with the data at 325°C, the TiN/GST TBR extrapolates to ~ 12.6 m^2K/GW at the GST melting temperature of 610°C.

5.5 Conclusions

This chapter uses an original multi-sample data extraction technique in the first temperature dependent measurements of the TiN/GST TBR, a critical quantity for PCM device simulations and engineering. DMM calculations using the measured heat capacity offer the best simple means to estimate the TBR between electrode and phase change materials. Acoustically mismatched phase change and electrode materials may improve thermal isolation of the PCM programming region.

Chapter 6

Conclusions

This dissertation developed fundamental understanding of thermal phenomena in phase change memory from the standpoints of both device design and physics. Its contributions may be loosely divided into advancements in PCM modeling and innovations in thin film thermal metrology that explain heat conduction physics in a host of phase change materials.

6.1 Summary of Modeling Advancements

The finite element analysis (FEA) model developed in this dissertation provides a robust means of simulating a variety of PCM devices. The model uses standard commercial packages to solve the coupled electrothermal problem for the temperature and voltage distributions while incorporating an original phase change model. A stochastic implementation of classical nucleation and growth theory comprises the phase change model, which was validated empirically for $Ge_2Sb_2Te_5$ in optical media [2]. By coupling the phase change model to the traditional FEA packages, the model resolves the evolution of the spatial distribution of phases during programming.

The FEA model demonstrates for the first time that the spatial distribution of thermal resistances is critical in determining PCM device performance. The thermal boundary resistance (TBR) strongly modifies the device temperature profile to decrease the reset programming current. This work shows that an effective thermal conductivity that lumps the

bulk and interface resistance contributions cannot cause the same reduction in programming current. The presence of TBR leads to a reduced lateral temperature gradient in the device active region. Reset programming requires that the amorphous dome form a series path with the bottom contact, which explains how the TBR reduces the programming current. Additionally, the reduced lateral temperature gradient minimizes overheating in the center of the active region. The FEA model establishes, therefore, that engineered thermal interfaces will lead to reduced programming current and enhanced reliability.

The closed form models developed in this dissertation reveal that the thermal resistance from the active region is the key design parameter for reducing the programming current without adversely affecting the electrical performance. The cell's effective electrical resistance influences the programming current in an analogous manner to the thermal resistance but also impacts other design parameters such as dynamic range. The electrical resistances of PCM cells should therefore be comparable when their relative performance is compared. Several explicit expressions predict the programming current in the three standard cell geometries (i.e. standard, confined, and double confined). These models accurately capture the experimentally measured programming current for PCM cells with a large range of contact diameters. The closed form expressions show that the distribution of heat generation influences the optimal confined cell geometry (i.e. minimized programming current) by changing the location of the active region. However, the optimal cell geometry maximizes the thermal resistance from the active region regardless of its location.

This work develops a general solution of the one-dimensional heat diffusion equation for an arbitrary number of domains. The solution is referred to as the thermal fin model for PCM devices. The model combines the physical insight and rapid calculation time of closed form solutions with the temperature profile offered by FEA simulations. The thermal fin model applies to a wide range of cell geometries and programming conditions and captures the effect of the spatial distribution of thermal and electrical properties. It quantitatively demonstrates how the location of the active region depends on the distribution of electrical properties in the cell. This work uses the fin model to demonstrate a novel multi-level programming scheme. By engineering asymmetry in the electrical and/or thermal interface resistances in confined cells, different regions of the cell are programmed at

different current levels. A key finding is that future multi-level implementations must depend on careful engineering of the heat generation and thermal resistance distributions in order to control the amorphous and crystalline domains during programming.

A new multi-level cell design uses a current-divider geometry to individually program different phase change regions. Compared to all previous multi-level cells, the proposed design offers many benefits: logarithmically spaced resistance levels, control of the programming current range for each level, and no reliance on threshold switching. A recursive design algorithm based on coupled electrical and thermal resistance networks automatically generates the required geometry for a given set of material properties and specified spacing between resistance levels. FEA simulations confirm the predicted R-I behavior. The original features and design attributes significantly advance understanding of the requirements for advanced multi-level PCM implementations.

6.2 Summary of Measurements and Metrology Advancements

Physical understanding of the thermal properties of phase change materials is essential for PCM device modeling and optimization. This dissertation reports the thickness dependent effective thermal conductivity of thin film $Ge_2Sb_2Te_5$ in the amorphous, fcc crystalline, and hcp crystalline phases at temperatures up to 340°C. As the first work to extend the nanosecond transient thermoreflectance (TTR) technique to high temperatures, it significantly advances the state of the art in TTR metrology. The effective thermal conductivity of $Ge_2Sb_2Te_5$ increases with thickness in all phases at all temperatures. The thickness dependence is due in part to thermal boundary resistance (TBR) and in part to the process and thickness dependent microstructural quality of the films. The process dependent component highlights the potential to engineer the thermal conductivity of phase change materials to optimize devices. These previously unmeasured phenomena clarify the important transport physics in thin film $Ge_2Sb_2Te_5$, and are critical in understanding PCM device performance.

The concentration of Sb in phase change materials ranging from GeTe to $Ge_2Sb_2Te_5$ has little impact on the effective thermal conductivity at room temperature. However, the amorphous to crystalline phase transition temperature decreases with increasing Sb concentration. The crystalline phase thermal conductivity is larger than the amorphous phase thermal conductivity for all the measured compounds. These results are consistent with crystal structure observations, and suggest the increasing Sb concentration reduces the average bond strength of the Ge interstitial atoms within the Te lattice. Combined with independent sound velocity [59], stiffness [89], and material structure [119] measurements, these data provide a self-consistent picture explaining the differences in thermal transport between the amorphous and crystalline phases of many chalcogenides. The increase in bond strength between Ge and Te atoms in the crystalline phase results in a stiffer material that supports higher sound velocities. The higher sound velocities and the increase in the electron contribution to the thermal conductivity account for the overall increase in thermal conductivity in the crystalline phases.

A picosecond time-domain thermoreflectance system was developed and optimized for measuring $Ge_2Sb_2Te_5$ thin films and their thermal boundary resistances. The system is among the first capable of accurately measuring both the phase and amplitude response of thin film samples, and is the first to measure the full thermal decay at temperatures up to 325°C. A solution of the radially-symmetric three dimensional heat diffusion equation models the complex-valued temperature evolution measured by the TDTR system. The solution advances existing techniques [79, 80] by predicting the measured temperature at an arbitrary location and by accounting for bi-directional heat flow from an arbitrarily located, embedded, heat source. These improvements enable a wide range of novel measurements that require separate transducers for the pump and probe beams in the TDTR system. New measurements include through-substrate probing for high surface roughness thin films (e.g. carbon nanotubes), measurements requiring models of the laser absorption, and flash diffusivity measurements on nanometer scale films.

An original thickness-implicit, multi-sample data extraction routine is the first to enable the simultaneous measurement of the thermal boundary resistance between the transducer and the adjacent thin film, the intrinsic thin film thermal conductivities, and the buried thermal interface resistances. This critical development permits a host of new measurements

that were previously inaccessible to picosecond TDTR systems. Specifically, it allows the measurement of thermal boundary resistance between a wide range of dielectric and semiconductor materials that are optically thin and/or sensitive to the laser excitation required by TDTR.

These techniques are used to measure the temperature dependence of the fcc $Ge_2Sb_2Te_5$ intrinsic thermal conductivity between 25°C and 325°C. The intrinsic thermal conductivity increases slowly with temperature, roughly tracking the temperature dependence of the volumetric heat capacity. Throughout the measurement temperature range the phonon mean free path is temperature independent and fixed at approximately half the lattice spacing, owing to the highly defective crystal structure. The sound velocity depends weakly on temperature. These measurements, therefore, confirm both the validity of the kinetic theory approximation of the thermal conductivity in $Ge_2Sb_2Te_5$ and the physical description revealed by the nanosecond TTR measurements. Additionally, the intrinsic conductivity shows no annealing hysteresis in contrast to previous measurements. Relatively high temperature fcc-phase deposition, therefore, offers a means to control the process dependent defect contribution to the thermal conductivity.

The TiN/fcc $Ge_2Sb_2Te_5$ and Al/TiN TBR measurements dramatically improve the accuracy of PCM device simulations by revealing the boundary resistance physics up to 325°C. In reporting the first TBR measurement results well above 100°C, this work makes significant advances in thin film TBR metrology and in the understanding of high temperature TBR physics. Both the TiN/$Ge_2Sb_2Te_5$ and Al/TiN TBRs decrease slowly with temperature which is qualitatively consistent with molecular dynamics calculations [96]. The diffuse mismatch model using the measured $Ge_2Sb_2Te_5$ heat capacity closely approximates the data, suggesting the actual phonon density of states (DOS) and its temperature dependence are essential for predicting the TBR between these materials. Additionally, the measurements show the room temperature TiN/$Ge_2Sb_2Te_5$ TBR is $\sim$4-5 times larger than the thermal resistance through the bottom contact heater. Consequently, this TBR is the key parameter determining the PCM programming current. These insights suggest that engineering the TBR by introducing interface layers with high phonon DOS mismatch can significantly reduce the programming current and improve device performance.

6.3 Suggestions for Future Work

The success of smaller, faster, devices requires increasingly sophisticated understanding of nanoscale device physics. Electron-phonon interactions, interface effects, and mass diffusion effects all become more important as devices are pushed to their physical scaling limits. This section highlights many of the challenges facing phase change memory and offers paths toward their solutions.

6.3.1 Modeling

Successful PCM implementations rely on careful engineering of the thermal resistance and heat generation distributions in the device. While current models do an excellent job informing basic thermal device design, the extreme electrical and thermal conditions near the active region severely limit understanding of how nanoscale physics may impact future device generations, illustrated schematically in figure 6.1. Lumped RC models adequately capture the physics important for general device scaling [31], but do not provide the detailed temperature profile necessary for predicting scaling of more advanced designs such as the confined cell [32]. Diffusion and drift-diffusion based finite element calculations readily incorporate more sophisticated physics such as interface effects. However, as the characteristic device dimensions approach the phonon and electron mean free paths, ballistic transport effects will become increasingly important for resolving the temperature and electrical current distributions. The heat generation and thermal resistance distributions will depend intimately on electron phonon scattering physics in the interface region, requiring the solution of the Boltzmann transport equation to accurately capture the programming current scaling, phase distribution, and threshold switching voltage.

6.3.2 Electron-Phonon Interactions Near the Interface

Thermal interface physics play a dominant role in PCRAM device programming current, reliability, and scaling [32, 30, 60]. The coupled electron-phonon interactions near the interface, some of which are depicted schematically in figure 6.2, give rise to a host of important effects: the interface Seebeck effect [113], the interface Wiedemann-Franz Lorenz

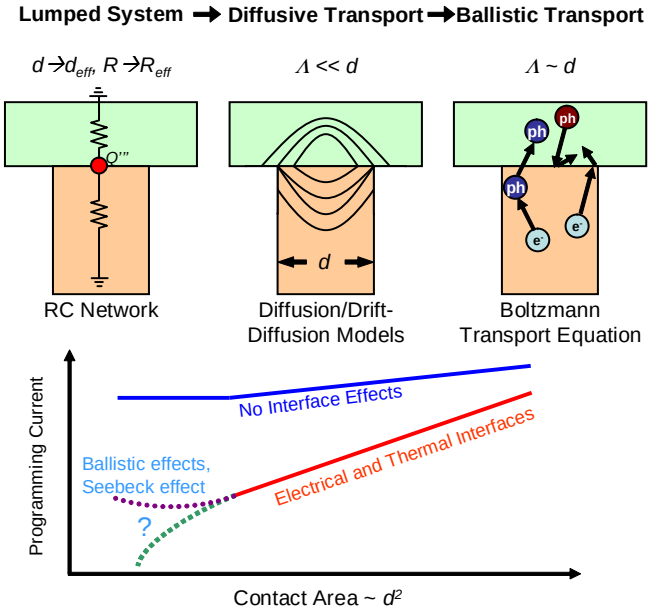

Figure 6.1: The thermal design considerations increase quickly in physical complexity as PCM devices scale. In the figure, d represents the characteristic length scale in the device, d_{eff} is an effective length scale for reduced geometries, R indicates electrical or thermal resistance, R_{eff} represents an effective resistance (electrical or thermal), Λ is the carrier mean free path, *ph* indicates a phonon, and e^- indicates an electron.

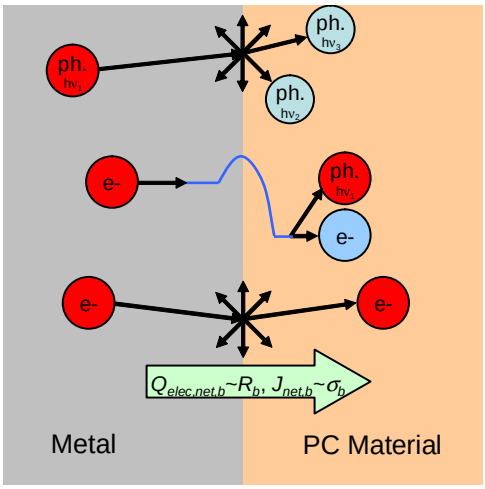

Figure 6.2: Schematic depicting some of the important electrothermal physics at PCM interfaces.

(WFL) rule and its applicability [104], the role of electron-phonon coupling in thermal boundary resistance (TBR) [97], and the role of anharmonic phonon scattering in TBR, specifically at interfaces with large temperature differences. These effects give rise to many practical questions that influence PCRAM device scaling and optimization: 1. How does the interface Seebeck effect influence the distribution of heat generation, and consequently device thermal efficiency? 2. What are the electrical interface resistance physics at metal-GST interfaces and does the interface WFL rule apply? How does this affect thermal interface engineering to reduce programming current? 3. Do electrons and phonons contribute comparably to conduction at metal-GST interfaces as they do in bulk crystalline GST conduction? How does coupling between electrons and phonons influence the TBR? 4. What is the nature of TBR at interfaces with large ΔT, such as the GST-metal interface in PCRAM? Does the TBR depend on heat/charge flux at the interface? How does it influence device scaling? How do large temperature differences affect electron-phonon coupling near the interface?

6.3.3 Thermal Boundary Resistance Engineering and Modeling

Design and engineering of material interfaces with large thermal boundary resistance and negligible electrical contact resistance are required to enhance the reliability and endurance

of the device while providing effective thermal insulation and heat generation confinement. These features will significantly reduce the programming current and required power. TBR and intrinsic conductivity measurements of electrode materials using picosecond TDTR are an essential step toward optimizing PCM device structures. Composite multilayer electrodes and interface layers comprised of metallic multilayers (e.g. Ti/W/C) or ultra-thin thin passivation layers (SiO_2) offer promise for increasing device thermal efficiency.

These advances will enhance multibit PCM which demands numerous additional requirements such as low power consumption, stable and repeatable intermediate states, multilevel programming strategies that result in a tight distribution of intermediate resistance values for multi-bit operation, larger spread in resistance versus programming current (set), reduced complexity of the driving circuitry, understanding of the physical origin of the threshold voltage drift, and eliminating the threshold voltage drift and variability.

6.3.4 Reliability: Anisotropy, Process Control, Mass Diffusion

While scaling and improvements in device thermal engineering will dramatically reduce programming current, improving the reliability of large arrays of bits is an essential step toward realizing PCM. Thermal transport in the phase change material sits at the heart of many reliability issues. Write disturb, induced by thermal cross-talk between adjacent bits, may be exacerbated by anisotropy in the phase change material's thermal conductivity. Specially designed electrical measurement structures using suspended membranes or the 3ω technique will identify the existence, if any, of thermal conductivity anisotropy. In-plane and out-of-plane electrical conductivity measurements and x-ray and electron diffraction experiments will help confirm the physical origin of any observed anisotropy. The existence of process dependence in the thermal conductivity implies that device cycling may impact the thermal properties and the device programming characteristics. Studies evaluating the process dependence of the thermal conductivity will help minimize cycling-dependent property variations, which will be particularly important in multi-bit applications. Repeated thermal and electrical stresses near the interface lead to mass diffusion and compositional changes in the phase change material. Composition changes can strongly modify the programming behavior and, in many cases, cause permanent device failure.

It is essential to understand the nature of the mass diffusion process, and whether novel materials and thermal engineering can mitigate its impact on reliability. Microfabricated suspended membranes with integrated heaters will establish the physical nature of the mass diffusion process in thin film chalcogenide materials by permitting independent control of the temperature, electric field, and current density. Auger electron spectroscopy (AES) and/or energy dispersive x-ray spectroscopy (EDS) measurements will quantify the elemental composition variation within the films after controlled thermal and electrical stressing events. Taken together these steps will dramatically improve the reliability of PCM architectures at the chip level.

6.3.5 Full-cycle Crystallization and In-Situ Device Probing

Previous work exploring thermal and electrical properties over a range of temperatures and programming conditions has suffered from the inability to precisely control the temperature evolution and distribution at timescales less than $\sim$10 seconds. Future work using integrated microheaters with thermal time constants below $\sim$100 ns will vastly improve understanding of numerous important phenomena such as the nature of resistance drift in the amorphous phase, the effect of cycling on the electrical and thermal interface resistances, the temperature dependence of the thermal conductivity, the effect of annealing on the electrical and thermal properties, and the nature crystallization at short timescales. These studies will help identify and overcome key scaling challanges, enable programming pulse shape optimization, and identify the role of electrons in bulk and interfacial thermal transport.

Thorough understanding of the de-coupled crystallization kinetics, electron transport, and thermal transport effects will enable meaningful, in-situ, device probing for the first time. In-situ device probing will solidify the validity of the coupled physics, leading to the first quantitatively accurate, directly validated multiphysics simulations. In-situ probing will require an integrated electro-optical test system, such as that depicted in figure 6.3, to probe the ultrafast phase change physics in an operating 150 nm technology PCM device. A simplified device geometry consists of a reflective bottom electrode metal in direct contact with the active region of the PC device. A conductive, transparent indium

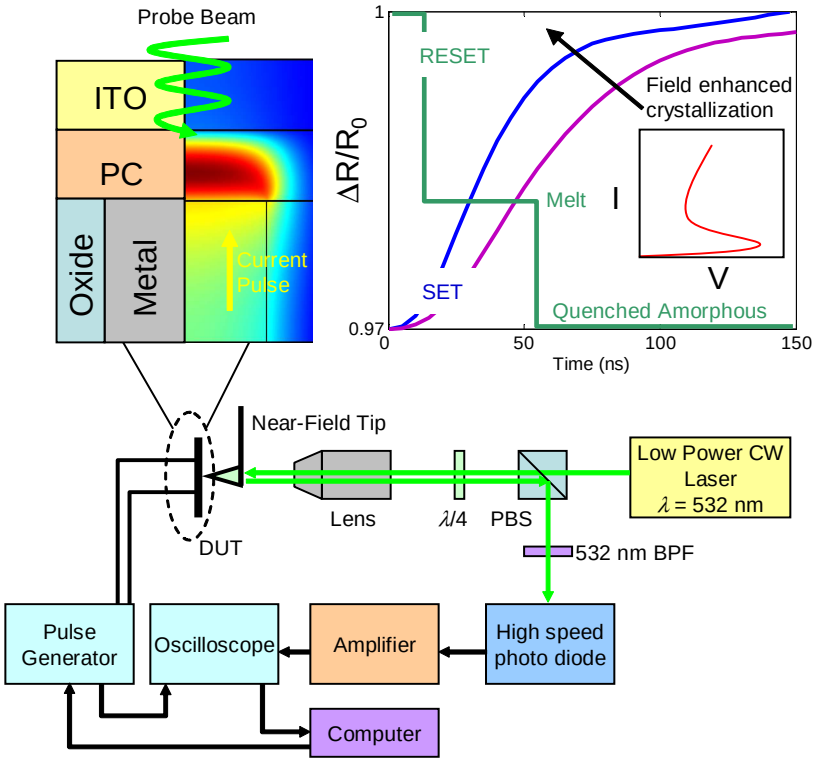

Figure 6.3: A potential electro-optical test system for in-situ device probing

tin oxide (ITO) top electrode permits optical access to the active region ($\sim$150 nm x 150 nm) of the device through tightly-focused diffraction limited optics or a near-field probe. A high power pulse generator programs the cell with controlled pulses between 10 ns $< t <$ 200 ns. Advances in modern digital oscilloscopes and photodiodes permit measurement bandwidths approaching 10 GHz. The physics revealed by these experiments are essential for understanding temporal and spatial device scaling rules, and will help bridge the fundamental gap between emerging understanding of ultrafast non-thermal phase change processes and established quasi-steady thermodynamic kinetics models.

6.4 Epilogue

With countless emerging applications requiring high-speed, non-volatile memory, the future of phase change memory is promising. The impending challenges require an increasingly interdisciplinary view of the nanoscale physical interactions at the core of PCM's remarkable characteristics. In the end, the solutions to these challenges and the physical insights they reveal will drive the innovations in memory required to satiate the hunger of a data driven world.

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