ULTRAFAST OPTICAL CHARACTERIZATION OF NANOSCALE THERMAL PROPERTIES

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Abstract

Ultrafast thermoreflectance is a powerful technique designed to measure thermal properties in films less than a micrometer thick. Careful sample design and control over the measurement timescale allow spatial and temporal confinement of the measurement to a region of interest. This work explores the capability of nanosecond and picosecond thermoreflectance in capturing the thermal properties of a host of exotic materials used in next generation electronic devices. These include the phase change material $Ge_2Sb_2Te_5$ (GST), diamond substrates for high electron mobility transistors (HEMT), and multilayer Mo/Si mirrors for extreme ultraviolet wavelengths (EUV).

Nanosecond and picosecond thermoreflectance were used to determine the thermal properties of the phase change material, GST, along with several candidate electrode films (C, Ti, TiN, W, and WN_x) and novel electrode multilayers (C-TiN and W-WN_x). These results offer a material selection roadmap for device designers seeking to tune the thermal properties of their PCM cell. This work also reports picosecond thermoreflectance measurements of GST films sandwiched between TiN electrode layers and annealed at multiple temperatures. Thermal conductivity of the hexagonal close-packed (HCP) phase exceeds that of the face centered cubic (FCC) phase due to the addition of electron thermal conduction. Electron interface transport is shown to be negligible, implying that the addition of electrons as energy carriers does not significantly affect thermal boundary resistance (TBR).

Thermal spreading analysis of a representative HEMT structure on diamond and SiC substrates shows that a device-substrate thermal interface resistance in excess of 20 m^2 K GW^{-1} negates the benefits of diamond as a substrate material. Picosecond thermoreflectance measurements on multiple diamond samples were performed to

determine the thermal conductivity, thermal anisotropy, and boundary resistance of diamond on AlN substrates. Further measurements on the top and bottom surfaces of a suspended diamond films demonstrated the thermal conductivity of the coalescence region (80 W m^{-1} K^{-1}) and high quality layer (1350 W m^{-1} K^{-1}) of a single diamond film. Using a two-layer model of the diamond film, we predict the thickness of the coalescence region and show it to be less than 1 μm.

The operating temperatures of Mo/Si multilayers used in EUV lithography affect their lifetimes. Predicting the mirror/mask damage threshold fluence requires accurate knowledge of the mirror thermal properties. This study reports high temperature thermal properties of the TaN masking film, the $MoSi_2$ intermetallic, and the room temperature properties of the Mo/Si multilayer. The thickness dependent electrical conductivity of TaN estimates the mean free path of electrons in the film unhindered by the material interfaces (~ 30 nm). Measurements on $MoSi_2$ demonstrate the change in thermal conductivity due to crystallization, from 1.7 W m^{-1} K^{-1} in the amorphous phase to 2.8 W m^{-1} K^{-1} in the crystalline phase. Mo/Si results demonstrate thermal conductivity (1.1 W m^{-1} K^{-1}) significantly lower than previous literature assumptions (4-5 W m^{-1} K^{-1}). A finite element thermal model uses these results to predict the maximum EUV fluence allowed on a Mo/Si mirror for a single shot and for a one billion pulse lifetime before causing a reflectance loss of 1%.

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Published Chapters

The listed chapters and sections of this thesis are based, in part, on the following published works.

2.1 E. Bozorg-Grayeli, J. P. Reifenberg, K. W. Chang, M. Panzer, and K. E. Goodson, "Thermal conductivity and boundary resistance measurements of GeSbTe and electrode materials using nanosecond thermoreflectance," in *IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITHERM) 2010*, June 2-5, Las Vegas, NV

2.2 E. Bozorg-Grayeli, J. P. Reifenberg, M. A. Panzer, J. A. Rowlette, and K. E. Goodson, "Temperature-Dependent Thermal Properties of Phase-Change Memory Electrode Materials," *Electron Device Letters, IEEE,* vol. 32, pp. 1281-1283, 2011.

3.1-3.2 E. Bozorg-Grayeli, Z. Li, V. Gambin, M. Asheghi, and K. E. Goodson, "Thermal Conductivity, Anisotropy, and Interface Resistances of Diamond on Poly-AlN", *IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITHERM) 2012*, May 30 - June 1, San Diego, CA

4.1 E. Bozorg-Grayeli, Z. Li, M. Asheghi, G. Delgado, A. Pokrovsky, M. Panzer, D. Wack, and K. E. Goodson, "High Temperature Thermal Properties of Thin Tantalum Nitride Films," *Applied Physics Letters*, vol. 99, p. 261906-1 – 261906-3, 2011.

4.2 E. Bozorg-Grayeli, Z. Li, M. Asheghi, G. Delgado, A. Pokrovsky, M. Panzer, D. Wack, and K. E. Goodson, "Thermal Conduction Properties of Mo/Si Multilayers for Extreme Ultraviolet Optics," *Journal of Applied Physics*, vol. 112, p. 083504-1 – 083504-7, 2012.

Chapter 1

Introduction

The scaling down of electronic device size has proceeded hand-in-hand with drastic increases in device heat flux. In particular, the last 15 years have seen a surge in the heating density of the CPU, with server processors pushing more than 100 W of thermal energy into 4 cm^2 packages. This phenomenon has made thermal engineering an essential part of processor design, with vast resources dedicated to mitigating the temperature rise in an operating device.

The first step towards predicting the thermal response of a device is to understand its thermal properties. The materials involved in such devices consist mostly of silicon, metal, and organic packaging materials, with a few exotic exceptions. For the most part, these materials are thermally well-characterized in bulk form. However, when these materials scale down to device sizes, energy carrier scattering can significantly impede thermal conductivity. As a result, bulk thermal properties may no longer apply. For this reason, there has been a concerted effort over the past few decades to develop methods of characterizing the thermal properties of materials at the nanoscale.

There are two main classes of nanoscale thermal characterization: electrical and optical. The former uses an electrical current through a metal wire, along with knowledge of the temperature-dependent electrical resistivity, to gauge the temperature of a material [1-10]. Optical probing techniques include Raman spectroscopy [11-18], infrared photothermometry [19-22], and thermoreflectance [23-33]. Of all these techniques, optical thermoreflectance accesses thermal properties on the smallest length scales, with

some samples less than 10 nm thick [34]. Further, sample preparation for thermoreflectance is typically minimal, involving only the deposition of a thin transducer film. Lastly, thermoreflectance setups can be tuned to access a wide range of thermal properties, including thermal conductivity, thermal boundary resistance (TBR) [35], heat capacity, thermal anisotropy [36], sound speed [37], and electron-phonon relaxation time [25, 38].

Chapter 1 introduces the physics behind the thermoreflectance technique, as well as offering background into its application. We explain the concepts of temporal and spatial confinement in transient and time-domain thermoreflectance, and discuss how they can be used to control the sensitivity of the technique to thermal properties in different regions of a thin film stack. The remainder of this thesis applies these techniques to understanding thin film thermal properties of materials used in phase change memory (Chapter 2), high electron mobility transistors (Chapter 3), and multilayer extreme ultraviolet mirrors (Chapter 4).

1.1 The Principle of Thermoreflectance

When a given material experiences a temperature change, its optical properties change as well. In particular, the reflectivity of a material tends to decrease as it is heated above room temperature. If the temperature-dependent optical properties of a material are known, then the reflectivity becomes an effective thermometer. The first authors to document this phenomenon took particular interest in the temperature-reflectance spectra of semiconductors. Batz first used the technique to characterize the spectra of Germanium in 1967 [39]. The following year saw reports on the thermoreflectance spectra for alkali metals [40], silicon [41], and a host of other semiconductors [42].

In 1972, Ujihara constructed a model for the thermoreflectance spectra of metals using the Drude theory for electrons along with an electron-phonon collision model [43]. The author used the temperature-dependent electron-phonon collision frequency to define the electron relaxation frequency:

$$\omega_c = K\left|\vec{k}\right|T^5 \int_0^{\theta/T} \frac{z^4}{e^z - 1} dz \tag{1.1}$$

where ω_c is the electron-phonon collision frequency, k is the electron wave vector, T is temperature, θ is the Debye temperature, and K is a constant. This value determines the dielectric constant of the material:

$$\epsilon = \epsilon_r + i\epsilon_i = 1 - \frac{\omega_p^2}{\omega^2 + \omega_c^2} - i\frac{\omega_p^2 \omega_c}{(\omega^2 + \omega_c^2)\omega} \tag{1.2}$$

where ω_p is the plasma frequency of the electrons and ω is the optical frequency. This, in turn, gives the metal reflectivity:

$$R(T) = \left|\frac{\epsilon^{1/2} - 1}{\epsilon^{1/2} + 1}\right|^2 \tag{1.3}$$

Ujihara showed monotonic and nearly linear temperature-reflectance spectra for metals. In particular, copper and aluminum were highly linear over the range of 300-1300 K, and demonstrated a large change in reflectance over the temperature range. The predictable and monotonic thermoreflectance behavior of metals ignited new interest in these materials [44, 45], along with the idea of using metal reflectance as a thermometer. In this method, a low-intensity laser shines on a metal film during a heating event (fig. 1.1(a)). As the temperature of the metal changes, so does the reflected signal (fig. 1.1(b)). If the temperature change is within the linear range of the thermoreflectance spectra, then the thermoreflectance coefficient is temperature-independent. As a result, the temperature of the metal film relates to the reflected signal via:

$$T(t) = T_0 + \Delta T(t) = T_0 + c_{tr}^{-1}\frac{\Delta I(t)}{I_0} \tag{1.4}$$

where T_0 is the initial temperature of the metal, ΔI is the change in reflected intensity, I_0 is the initial reflected intensity of the probe beam, and:

$$c_{tr} = \frac{d\left(\frac{\Delta R}{R}\right)}{dT} \tag{1.5}$$

is the thermoreflectance coefficient.

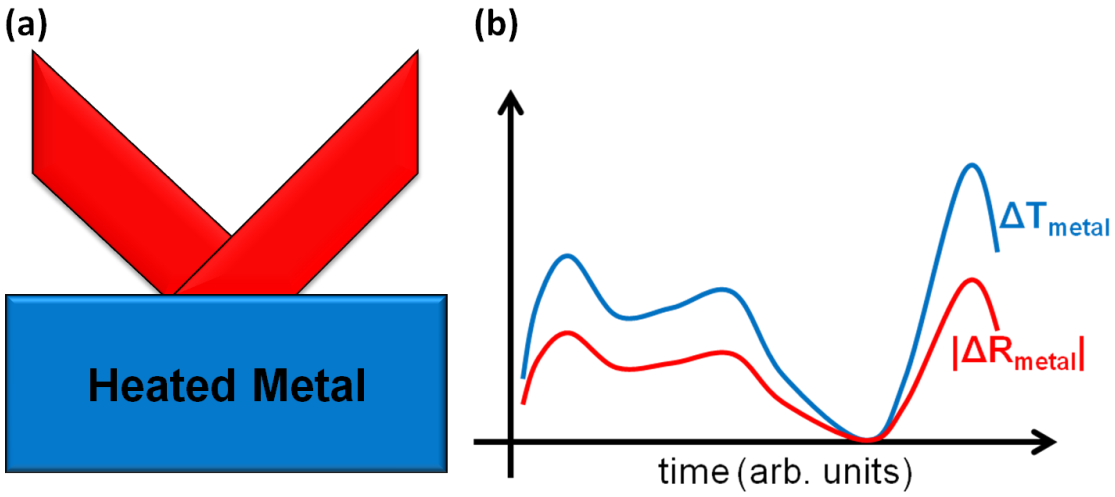

Fig. 1.1 (a) As the metal is heated, the reflected signal of a probe laser on the surface gauges the temperature. (b) If the temperature excursion of the film is within the linear range of the thermoreflectance spectra, then the temperature of the metal is linearly related to the reflectivity.

This technique offered great promise for determining the thermal properties of a variety of thin metal films. In 1986, Paddock and Eesley reported a transient thermoreflectance (TTR) experiment on metal films as thin as 60 nm [23]. The authors used a modelocked Ar ion laser with an 8 ps full-width at half-maximum pulsewidth as the pump and probe source. The pump beam travelled along a fixed optical path and heated the metal film. A retroreflector mounted on a variable delay stage controlled the probe beam path length. By varying the stage position, the authors controlled the transit time of the probe pulse, delaying when the probe arrival time relative to the pump. By moving the retroreflector, the reflected probe signal indicated the temperature of the metal film at some point in time after the pump pulse arrived. Since the pump pulse was only 8 ps long, and the delay time less than 200 ps, the heat generated in the metal film by each pulse would have time to diffuse ~60 nm into the film. This made the measurement insensitive to the thermal properties of the substrate material.

Temporal confinement of the heating event thus became one of the first tuning knobs on a thermoreflectance setup. By varying the characteristic heating time, one could control the thermal penetration depth of the measurement:

$$d_{pen} = \sqrt{\alpha \tau_c} \tag{1.6}$$

where d_{pen} is the thermal penetration depth, α is the thermal diffusivity of the heated material, and τ_c is a characteristic timescale associated with the measurement. Pulse width, measurement time, and modulation frequency of the pump beam contribute to this timescale [36]. Figure 1.2 demonstrates where various thermal measurement techniques fall in terms of temporal confinement.

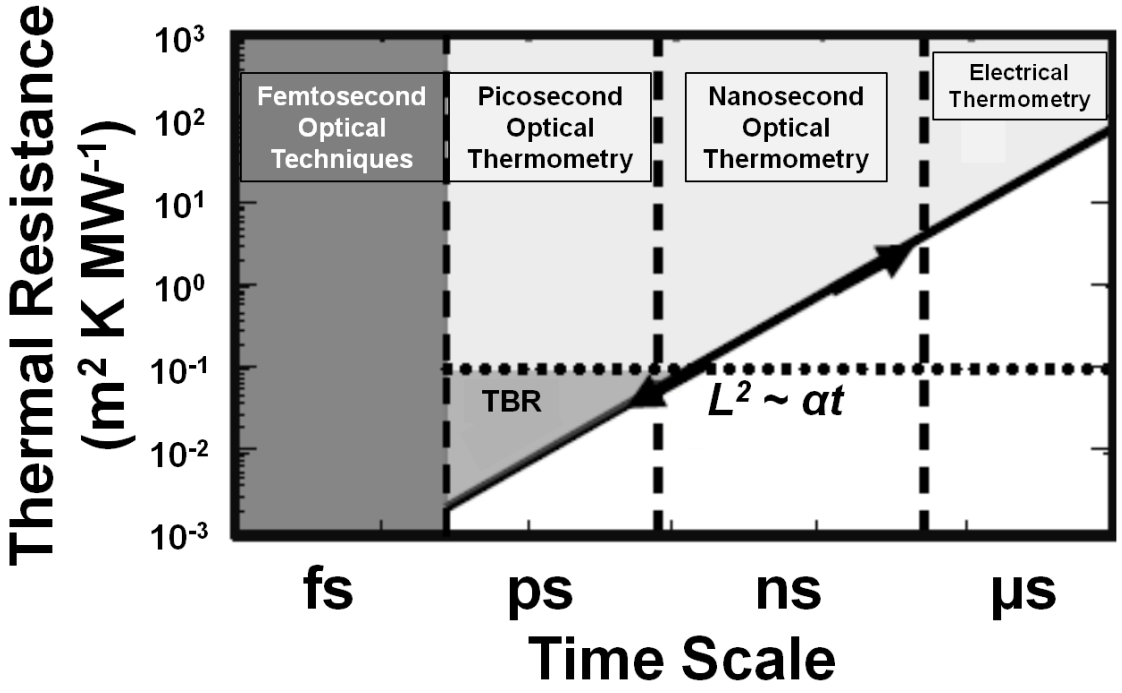

Fig. 1.2 (a) Resolvable thermal resistance (darkened region) as a function of characteristic measurement time scale. Thermal boundary resistance becomes resolvable at picosecond timescales. In the femtosecond regime, non-equilibrium physics dominates the thermoreflectance response.

In the case of electrical thermometry, the electrical time constant of the heating wire limits the measurement timescale to the order of microseconds. This enables thermal measurements down to ~ 10 m^2 K MW^{-1} (equivalent to ~ 7 μm of SiO_2). Nanosecond optical techniques can reach resistances ~ 100 m^2 K GW^{-1} (equivalent to 70 nm of SiO_2). In the case of picosecond optical thermometry, the timescale is short enough to resolve a single thermal boundary resistance. At femtosecond timescales, we enter the regime of nonequilibrium physics. In this case, the heating event is shorter than the electron-phonon relaxation time, temporarily causing the electron temperature to greatly exceed the

phonon temperature [38, 46]. Allen developed a theoretical model for electron-phonon relaxation [46], and Qiu and Tien used this with a two-step heating model to analytically fit the thermoreflectance response to a 96 fs pump pulse [47].

In 1999, Feldman developed an algorithm to compute the temperature due to 1-D heat diffusion through a multilayer stack of materials [48]. Up to this point, analysis of thermoreflectance response relied on the assumption that the generated heat did not reach the substrate. This limited the technique to either metals with thickness greater than the thermal penetration depth, or thin metal films on top of films thick enough to prevent substrate sensitivity. Feldman's algorithm revolutionized the thermoreflectance technique by creating a numerical model for heat diffusion through multiple materials. Sensitivity to substrates became less of a concern as long as the substrate thermal properties were known, since the model could account for them. In 2004, Cahill expanded this model to include heat spreading from a Gaussian heat source [49].

The history of this technique led to two separate methods for capturing the temperature decay of the metal transducer. When the thermal decay time was longer than several microseconds, a single photodiode and oscilloscope could capture the entire decay curve in a single shot. We refer to this technique as nanosecond thermoreflectance (NTR). NTR is not effective, however, with decay times on the order of a nanosecond or less. In this case, Paddock and Eesley's time-delay technique is necessary [23]. Although this method was also originally referred to as TTR by Paddock and Eesley [23], many now refer to it as time-domain thermoreflectance (TDTR). The following sections illustrate the NTR and TDTR setups used in this thesis.

1.2 Nanosecond Thermoreflectance

Nanosecond thermoreflectance characterizes the thermal properties of sample structures by optically measuring their transient thermal response to nanosecond pulse heating. A high-power 532 nm Nd:YAG pump laser heats a 10 mm^2 area on the surface of the sample with a 6 ns pulse at a repetition rate of 10 Hz (fig. 1.3). The pump laser has a "top-hat" profile, and since it is much wider than the pump beam, heat diffusion from the transducer is effectively one-dimensional. Assuming total absorption of a 6 mJ pulse

with no heat dissipation, the maximum temperature rise of the transducer is ~ 10 K. This is well within the linear thermoreflectance coefficient range of metals at room temperature.

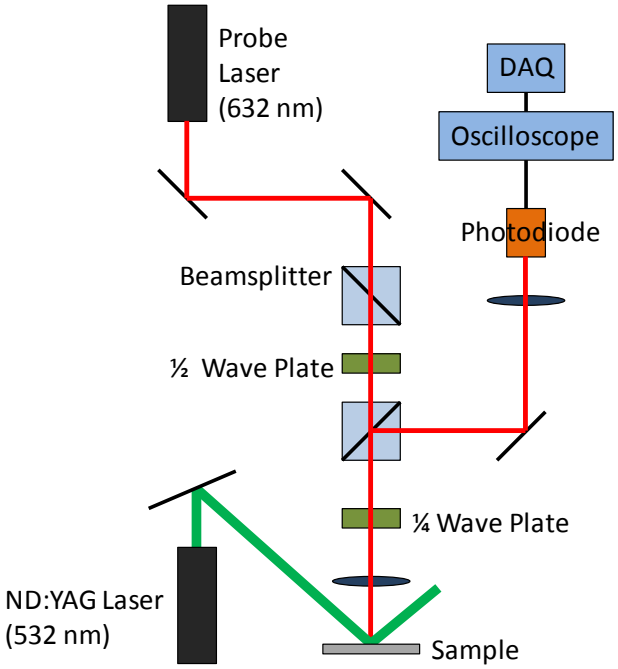

Fig. 1.3 Diagram of the nanosecond TTR setup.

A 650 MHz photodiode and amplifier measures the reflected intensity of a coincident 632 nm CW probe beam during a 20 μs temporal window after the pump pulse. The voltage signal, captured with an oscilloscope, tracks the relative temperature decay of a metal transducer with a temporal resolution of ~ 2 ns. Since the measurement technique and non-dimensional heat diffusion equation are both linear with temperature, the thermal properties of the stack can be determined without knowledge of c_{tr}. The accuracy of the nanosecond setup was confirmed by observing the decay time of a TiN transducer layer on a quartz substrate. Figure 1.4 shows the experimental data and a corresponding analytical fit using the known properties of these materials.

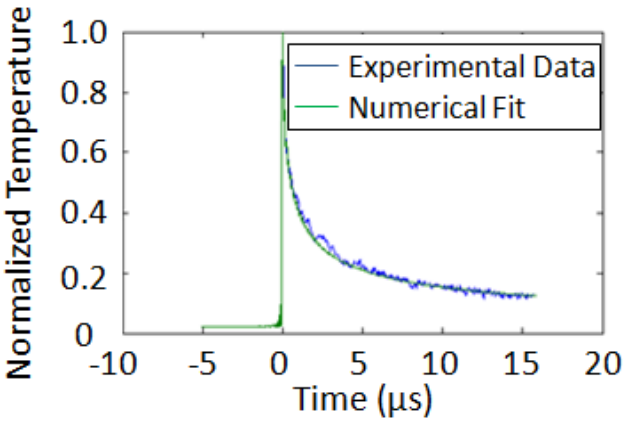

Fig. 1.4 Experimental result for a TiN on quartz calibration sample along with numerical fit for k_{quartz} = 1.4 W m^{-1} K^{-1}.

1.3 Picosecond Time-Domain Thermoreflectance

Picosecond TDTR is an optical pump-probe technique which uses an ultrafast laser system as a simultaneous heat source and thermometer [27, 34]. In this measurement, a passively-modelocked Nd:YVO_4 laser generates 9.2 ps optical pulses at 1064 nm (fig. 1.5). A half waveplate and polarizing beamsplitter separate this pulse into pump and probe components, with the pump intensity being significantly greater than the probe. The pump beam travels along a fixed optical path, during which it is frequency-doubled and modulated by an electro-optic modulator. The pump modulation frequency controls the thermal diffusion depth of the heating event [36]. The pump then travels through an objective and heats a metal transducer on the sample. The probe beam travels along a separate optical path containing a linear delay stage. This stage controls the total path length taken by the probe beam, allowing us to control the relative delay between when pump and probe strike the sample. A lock-in amplifier measures the reflected probe signal component at the pump modulation frequency. This reflected signal scales linearly with the transducer temperature [23, 50], allowing one to plot normalized transducer temperature as a function of time after the heating event (fig. 1.6). Using a theoretical model of heat diffusion through a multilayer stack of materials due to modulated optical heating [48, 49], one can extract the thermal properties of the films beneath the transducer.

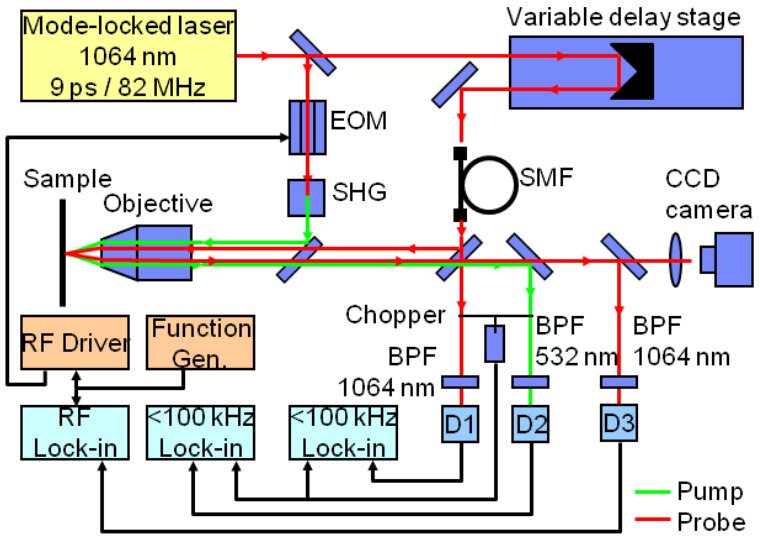

Fig. 1.5 Diagram of the picosecond TDTR setup.

High-temperature thermal measurements are often necessary for thin films expected to operate at temperatures greatly in excess of 300 K. Unfortunately, exposure to elevated temperatures can accelerate oxidation in the transducer film. To prevent this, high-temperature measurements are performed in an optical access oven (fig. 1.7). This oven maintains the sample in vacuum (or a non-reactive gas environment) in front of a transparent sapphire window, allowing both the pump and probe beams through. This extends the measurement range to temperatures on the order of 700 K [34, 51].

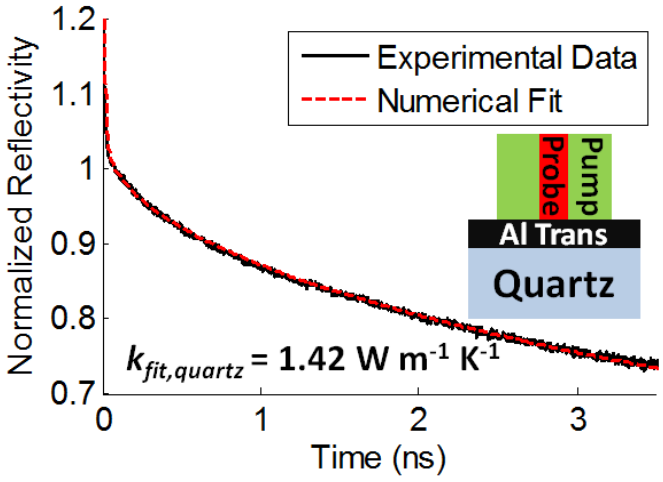

Fig. 1.6 Experimental result for an Al on quartz calibration sample along with analytical fit for k_{quartz} = 1.42 W m^{-1} K^{-1}.

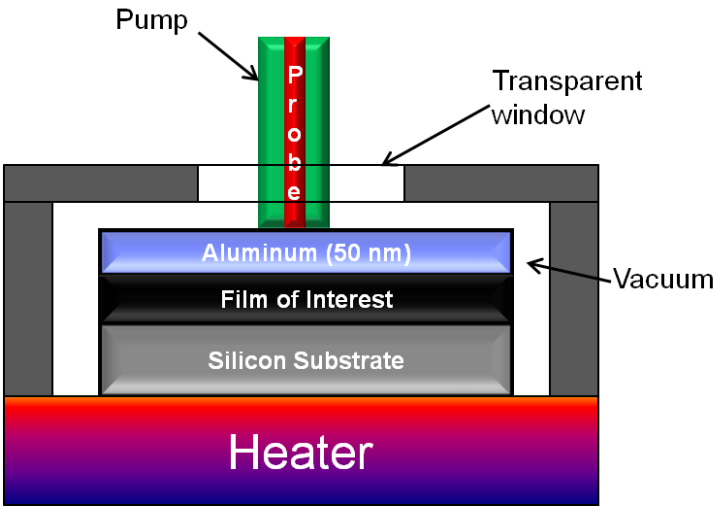

Fig. 1.7 Cross-sectional diagram of the optical access oven.

1.4 Data Fitting and Error Sources

Analyzing transient heat conduction through a multilayer stack of films relies on an algorithm developed by Feldman in 1999 [48]. This approach solves the Fourier heat conduction equation assuming a modulated heat input at frequency ω at the boundary of each layer. The solution to this equation is given by:

$$T(z) = T_j^+ \exp(u_j z) + T_j^- \exp(-u_j z) \tag{1.7}$$

where T_j^+ and T_j^- are complex constants associated with the propagation of thermal waves in the $+z$ and $-z$ directions, $u_j^2 = -i(\omega/\alpha)$, and α is the thermal diffusivity of the film. At each material boundary, the analysis assumes the following boundary conditions:

$$T_a(\xi^-) = T_b(\xi^+) + R_{ab} q \tag{1.8}$$

$$k_a \frac{dT_a}{dz}\bigg|_{z=\xi^-} = k_b \frac{dT_b}{dz}\bigg|_{z=\xi^+} + q \tag{1.9}$$

where a and b refer to the two materials in contact, k is thermal conductivity in each medium, R is the TBR between the films, q is the heat input at the boundary, and ξ is the local coordinate referring to the boundary plane in each film. Equations (1.7)-(1.9) can be expressed in terms of the matrices:

$$\boldsymbol{T}_a(z_j) = \boldsymbol{U}_a(L)\boldsymbol{T}_a(z_i) \tag{1.10}$$

$$\boldsymbol{T}_b = \boldsymbol{\Gamma}_{ba}\boldsymbol{T}_a \tag{1.11}$$

where $\boldsymbol{T}_a(z_j)$ is the temperature in medium a at location z_j, $\boldsymbol{T}_b$ is the temperature in medium b adjacent to medium a, $L = z_j - z_i$, and:

$$\boldsymbol{U}_a = \begin{bmatrix} \exp(u_a L) & 0 \\ 0 & exp(-u_a L) \end{bmatrix} \tag{1.12}$$

$$\boldsymbol{\Gamma}_{ba} = \frac{1}{2\gamma_b}\begin{bmatrix} \gamma_b + \gamma_a + \gamma_b\gamma_a R_{ab} & \gamma_b - \gamma_a - \gamma_b\gamma_a R_{ab} \\ \gamma_b - \gamma_a + \gamma_b\gamma_a R_{ab} & \gamma_b + \gamma_a - \gamma_b\gamma_a R_{ab} \end{bmatrix} \tag{1.13}$$

where $\gamma_j = u_j k_j$.

This algorithm provides the temperature of a stack of thin films under modulated heating. However, this analysis assumes only 1-D conduction. To expand this model to a Gaussian heat source and 3-D conduction, we use the following formulation developed by Cahill [49]:

$$\Delta T(\omega) = 2\pi A \int_0^\infty G(k') \exp\left(-\frac{\pi^2 k^2 (w_0^2 + w_1^2)}{2}\right) k' dk' \tag{1.14}$$

where ΔT is the temperature rise measured by the Gaussian probe beam, A is the amplitude of the heat source, w_0 is the $1/e^2$ radius of the probe beam, w_1 is the $1/e^2$ radius of the pump beam, and:

$$G(k) = \left(\frac{B_1^+ + B_1^-}{B_1^- - B_1^+}\right)\gamma_1^{-1} \tag{1.15}$$

where:

$$\begin{aligned} \begin{bmatrix} B^+ \\ B^- \end{bmatrix}_j = {} & \boldsymbol{U_j}(\xi - L_j) \times \Gamma_{j,j+1} \times \boldsymbol{U_{j+1}}(-L_{j+1}) \times \Gamma_{j+1,j+2} \times \ldots \\ & \times \Gamma_{N-2,N-1} \times \boldsymbol{U_{N-1}}(-L_{N-1}) \times \Gamma_{N-1,N} \times \boldsymbol{U_N}(-L_N) \times \Gamma_{N,N+1} \\ & \times \begin{bmatrix} 1 \\ 0 \end{bmatrix} \end{aligned} \tag{1.16}$$

This offers the temperature solution for Gaussian beam heating at a single frequency. To convert this solution into the time-domain for a Gaussian heating event, we use:

$$\Delta T(t) = \int_{-\infty}^{\infty} \sqrt{\pi\tau^2} P \exp(-\pi^2\omega^2\tau^2) \exp(2\pi i\omega t)\, \Delta T(\omega)\, d\omega \tag{1.17}$$

where 2τ is the 1/e pulsewidth and P is the power amplitude of the Gaussian function defining the heating event. Since we typically solve for the nondimensionalized solution to the Fourier heat diffusion equation, and since we want to avoid sensitivity to electron-phonon coupling effects with the first tens of ps after the pump pulse, we then normalize the temperature decay via:

$$\Theta = \frac{\Delta T(t)}{\Delta T(t_{norm})} \tag{1.18}$$

where t_{norm} is the normalization time point. We select 100 ps after the pump pulse as the normalization time to minimize the sensitivity of our fit to non-equilibrium electron-phonon physics occurring during the pump pulse. Changing this normalization time point by 50% results in a 1-2% change in the fitted parameter result. This suggests the extracted parameter is not significantly sensitive to the user-selected normalization time.

The fitting code uses this algorithm to iterate over various predictions for the properties of the material stack to find the solution with the lowest residual value between the numerical fit and the thermoreflectance data. These properties include thermal conductivities, thermal boundary resistances, heat capacities, thermal anisotropy, and film thicknesses. It is usually the case that the geometry and heat capacities of the stack are known, and the films are assumed to be thermally isotropic. As a result, this algorithm primarily fits for thermal conductivity and thermal boundary resistance. There are exceptions to this rule where heat capacity, film thickness, and anisotropy are unknown. In these cases, careful sample design, temporal confinement of the heating event, or spatial confinement of the pump beam can enhance sensitivity to the desired properties.

Within a given measurement, there are several potential sources of uncertainty. These include signal noise, film thickness uncertainty, and degenerate solutions. To determine the total error for a given sample, we calculate each error component separately by: 1) fitting for multiple thermal decay traces which fit within the sample noise data, 2) fitting for multiple thermal decay traces using a range of assumed film thicknesses within the thickness uncertainty, and 3) fitting for multiple thermal decay traces by varying the two parameters which result in degenerate solutions (usually these parameters are the thermal conductivity and film-substrate thermal boundary resistance).

The sum of the squares of these uncertainty components determines the total uncertainty of the measurement. These uncertainty sources can be reduced, respectively, by: 1) taking multiple thermoreflectance traces and averaging the results to reduce signal noise, 2) performing cross-sectional SEMs or TEMs to verify the sample geometry, and 3) designing films sufficiently thick to prevent sensitivity to the film-substrate TBR.

Of these sources, the uncertainty due to degenerate solutions is the most subtle and difficult to eliminate. To begin with, the error created by altering one parameter in the fit depends on the thickness of the film. A given film has a total thermal resistance:

$$R_{total} = R_{Transducer-Film} + \frac{d_{Film}}{k_{Film}} + R_{Film-Substrate} \tag{1.19}$$

where d_{Film} is the thickness of the film of interest, k_{film} is the intrinsic thermal conductivity, and $R_{a\text{-}b}$ is the thermal boundary resistance between layers *a* and *b* in the stack. The thermoreflectance technique extracts the total thermal resistance, and the fitting code separates the results into TBR and intrinsic resistance components. If we assume one component of the fit incorrectly, it affects the other parameters as well.

Let us assume that $R_{Film\text{-}Substrate}$ is negligible. In this case, reducing the assumed value of $R_{Transducer\text{-}Film}$ by a factor, ε, would alter k_{Film} according to the formula:

$$k'_{Film} = d_{Film}\left(\frac{d_{Film}}{k_{Film}} + \varepsilon R_{Transducer-Film}\right)^{-1} \tag{1.20}$$

where k'_{Film} is the fitted film thermal conductivity assuming error, ε, in $R_{Transducer\text{-}Film}$. As an example, assume we have a 100 nm SiO_2 film, with a transducer-film TBR of 10 m^2 K GW^{-1} and film thermal conductivity of 1.4 W m^{-1} K^{-1}. A 100% error in TBR (i.e. $R_{Transducer\text{-}SiO2}$ is assumed to be negligible), we predict k'_{Film} = 1.23 W m^{-1} K^{-1} (an error of ~ 12%). This value estimates the best possible fit for k_{SiO2} assuming no TBR between the film and the transducer. However, this may not be the best possible fit for the total film stack. This is because different sections of the thermal decay curve are sensitive to different properties within the stack. For example, the thermal decay behavior in the first ns depends mainly on the transducer-film TBR (fig. 1.8(a)). At later times, the film thermal conductivity and film-substrate TBR control the thermal decay behavior (fig.

1.8(b)). So, although we can find a fitted thermal conductivity even with a poor TBR assumption, the fit may not offer the lowest residual value.

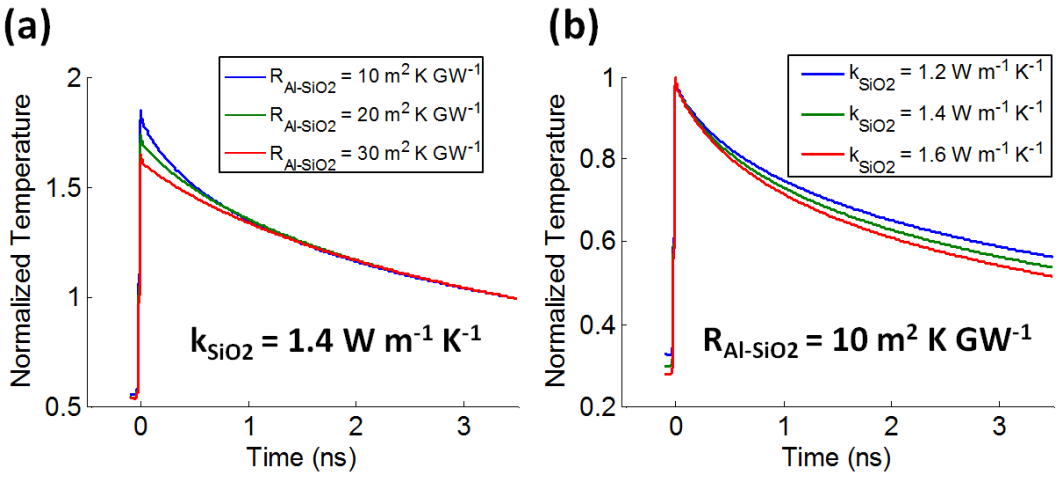

Fig. 1.8 (a) The thermal decay behavior during the first ns after the pump pulse depends primarily on the transducer-film TBR. (b) During the following 2.5 ns, the intrinsic thermal conductivity of the film controls the thermal decay behavior.

Figure 1.9 demonstrates this principle, showing the two separate fits using different assumptions for $R_{Transducer\text{-}Film}$. Even though both fits minimize the residual value given their assumptions for TBR, the resulting curves are different. This difference helps one determine whether a particular thermal property assumption for the film is valid, reducing the potential error caused by degenerate solutions.

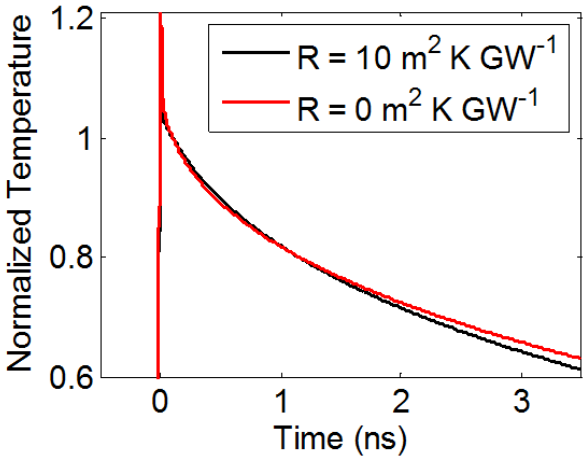

Fig. 1.9 Thermal decay traces for 50 nm Al transducer on 100 nm SiO_2 on Si assuming: (1) $R_{Al\text{-}SiO2}$ = 10 m^2 K GW^{-1} and k_{SiO2} = 1.4 W m^{-1} K^{-1}, and (2) $R_{Al\text{-}SiO2}$ = 0 m^2 K GW^{-1} and k_{SiO2} = 1.23 W m^{-1} K^{-1}

1.5 Summary

Nanosecond thermoreflectance and picosecond time-domain thermoreflectance are non-contact/non-destructive techniques capable of extracting thermal properties at nanometer length scales. The characteristic heating timescale of each technique controls the thermal penetration depth of the measurement, allowing temporal confinement of the measurement to a region of interest. These techniques enable us to measure thermal properties in films less than hundreds of nanometers thick, including boundary resistances. This work presents thermoreflectance measurements of several classes of materials used in novel electronic devices. These include phase change memory materials, high electron mobility transistor materials, and multilayer mirrors for extreme ultraviolet lithography.

Chapter 2

Phase Change Memory

Increasing the data storage density of magnetic hard drive technology is becoming more difficult due to the rising magnetic field densities required. Future hard drives will require new methods of data storage with bit sizes on the order of tens of nanometers and data stability for millions of cycles [52]. Phase Change Memory (PCM) is a promising new non-volatile memory technology that addresses these challenges by offering scalability down to nanometer bit sizes, bit stability during power loss, and long memory cycling life. Phase change materials, first observed by Ovshinsky in 1968, are capable of rapidly switching between amorphous and crystalline phases via joule heating [53]. The amorphous-crystalline transition is the 'set' operation, and the reverse is called 'reset'. PCM cells perform the set operation by rapidly heating the bit above the glass temperature, and allowing it to cool over a period of ~100 ns. The cell resets into the amorphous phase by melting the phase change material and rapidly quenching over a ~10 ns time period (fig. 2.1).

There are many ways to implement this style of data storage using both non-contact and contact methods. In non-contact PCM, a laser rapidly heats and quenches a bit on an optical disc, using the phase-dependent reflectance contrast to store data. Contact-based PCM utilizes Joule heating in an electrode and/or phase change material to heat the cell (fig. 2.2). More complex forms of contact PCM cells have been demonstrated by IBM's Millipede structure, which utilizes heated probe tips to locally write and read individual bits [54]. In order to differentiate between the set and reset states of the bit, the electrical resistance of each phase must be dissimilar. The goal of

PCM design thus becomes the creation of cells with distinct set and reset resistances, as well as minimized write times, maximum reliability, and maximum bit density. Commonly known phase change materials exhibit well-known and low thermal conductivities.

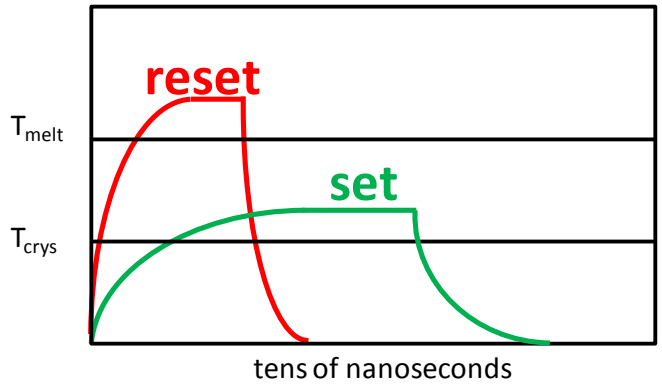

Fig. 2.1 Set and reset operations for a phase change cell.

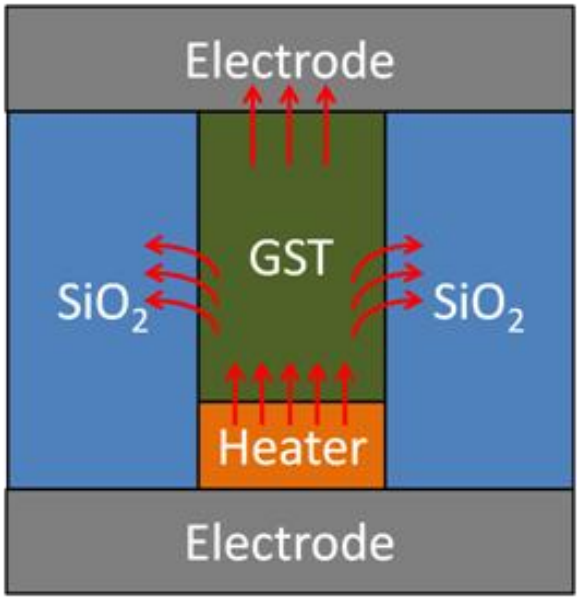

Fig. 2.2 Cross-sectional view of an electrically switched PCM cell. The arrows indicate direction of heat flow in the device.

$Ge_2Sb_2Te_5$ (GST) is the most common phase change material in PCM devices. This material offers a large difference in electrical conductivity between the amorphous and crystalline phases [55]. The intrinsic thermal conductivity is well-characterized and stable up to 10^5 cycles [56]. GST exists in one of three phases: 1) an electrically resistive

amorphous phase, 2) a slightly less electrically resistive face-centered cubic (FCC) phase, and an electrically conductive hexagonal close-packed (HCP) phase. The crystallization kinetics of GST allow phase change to occur at nanosecond timescales with a temperature rise ~100 ^{o}C. These crystallization properties are well-documented. Senkader and Wright demonstrated numerical models of crystal nucleation and growth in a PCM cell [57, 58]. Zhou [58], Kooi et al. [59], and Kolobov et al. [60] presented results on measurements of crystallization rates in GST and other PCM materials.

Phase change memory materials can be switched via electric fields [53], optical pumping [61-64], and thermal heating [30, 65]. Switching in the presence of an applied electric field occurs when a current filament sets up through the phase change medium [66, 67]. Joule heating within this filament causes the local temperature to rise rapidly. If this temperature exceeds the melting/crystallization temperature of the phase change material and the material is subsequently quenched, the heated region is amorphized/crystallized. The switching times, temperatures, and currents involved are affected by local phase content [68-70], film thickness [70, 71], stoichiometry [72, 73], and thermoelectric properties [74, 75].

In the case of optical switching, if sufficient photon energy flux is incident on the phase change material, the absorbed energy will result in a temperature excursion in the pumped area which induces phase change. This technique, commonly used for CD-RW drives, is thermal in nature. However, Dresner and Stringellow demonstrated phase transformations using high-energy optical pulses without exceeding the crystallization temperature [76]. The wavelength dependence of the observed transition further demonstrated that phase transformation depended upon the number of electron-hole pairs created by the influx of optical energy. Later experiments confirmed the non-thermal nature of optical phase change using ultrafast laser pulses [77, 78]. Konishi et al. were able to amorphize $Ge_{10}Sb_2Te_{13}$ using a single 140 fs pulse from a Ti:Sapphire laser. By measuring the resulting reflectivity change over time, they confirmed that the irradiated area had amorphized within 1 ps of the application of the pulse [77]. Such a transition is on the order of the electron-phonon relaxation time in metals [38], making it unlikely that the lattice could have reached amorphization temperatures. Rather, the authors suggest

that the high density electron excitation directly breaks the Ge-Te bonds in the structure, displacing the Ge sublattice [79, 80].

Thermal heating methods, however, demonstrate that electrical current is not necessary to change the phase of a device. In measurements done by Lyeo et al. [30] and Reifenberg et al. [65], the authors were able to induce phase change through the use of temperature-controlled ovens or hot plates. By heating the samples above the crystallization temperatures and quenching, they demonstrated the presence of FCC and HCP phases absent the use of electric fields.

As device dimensions reduce to tens of nanometers to accommodate greater data density, the thermal resistance of the interfaces becomes comparable to the volumetric resistances [81]. Thermal boundary resistance (TBR) tends to be in the range of 1 to 100 m^2K/GW for most material boundaries. Assuming the TBR of GST-SiO_2 is roughly 10 m^2 K GW^{-1} and k_{SiO2} ~ 1.4 W m^{-1} K^{-1}, the boundary acts like a layer of SiO_2 with effective thickness t ~ 10 nm. As such, it is essential to characterize the TBRs between GST and electrode materials to accurately model devices of interest.

Early TBR measurements were performed by Kapitza during his experiments on thermal conduction between Cu and liquid He [82]. The first attempt to model this resistance interpreted phonon transmission at a material boundary as being similar to photon transmission and reflection between materials with different refractive indices. This Acoustic Mismatch Model (AMM) indicated that transmission of phonons was dependent upon the sound speed and density of the interacting materials. However, this model assumes a perfect planar interface, and is only accurate at temperatures below 10K, when phonon wavelength is much greater than the boundary roughness [83, 84]. Swartz and Pohl extended this model to higher temperatures, where higher frequency phonons scatter diffusely on defects and the rough material boundary [83]. However, this Diffuse Mismatch Model (DMM) is also limited, often under-predicting boundary resistance. As a result, experimental determination of TBR is imperative. Using AMM, the TBRs between a-GST and the electrode materials are 0.03 m^2 K GW^{-1} for C, 2.0 m^2 K GW^{-1} for Ti, and 0.9 m^2 K GW^{-1} for TiN at 300 K. The corresponding resistances for c-GST are 0.07, 0.88, and 1.9 m^2 K GW^{-1}. Studies on the TBR between GST and electrode

materials show data that exceed these estimates [34], implying that interfacial effects dominate over acoustic mismatch.

For PCM devices, Reifenberg et al. [85] demonstrated the importance of thermal boundary resistance. Yang et al. and Reifenberg et al. measured the dependence of thermal conductivity on the stoichiometry and thickness of GST, determining that concentration of Te and film height can drastically change the thermal properties of the material [65, 86]. Lyeo et al. measured the conductivity of GST with Time Domain Thermoreflectance Thermometry [30], yielding ~0.19 W m^{-1} K^{-1} for a-GST, ~0.57 W m^{-1} K^{-1} for c-GST, and ~1.58 W m^{-1} K^{-1} for h-GST. Giraud et al. measured the intrinsic thermal conductivity of GST insulated with ZnS:SiO_2 using the 3ω method [2]. They obtained thermal conductivities of ~0.24 W m^{-1} K^{-1} for a-GST and ~0.29 W m^{-1} K^{-1} for c-GST. Due to the unique crystallographic nature of the authors' samples, along with their decision to neglect GST-ZnS:SiO_2 TBR and spreading resistance, the measured thermal conductivities are low compared to other literature data.

Thermal boundary resistance depends on the interface qualities and phonon properties of each material. Electron-phonon interactions may contribute at metal/nonmetal interfaces [83], as section 2.3 will demonstrate. Approaching the Debye temperature, the effect of the phonon acoustic spectra and electron-phonon interaction on TBR is small compared to the effect of interface properties, such as grain boundaries, impurities, and surface defects. These latter properties depend on deposition method.

2.1 GST-Electrode Thermal Boundary Resistance

In this study, multi-layer stacks consisting of varying thicknesses of GST on electrode materials are prepared. Measuring the thickness dependence of the thermal resistance of the multi-layer GST-electrode material stacks provides a means to separate the intrinsic GST thermal conductivity from the GST-electrode TBR. A reflective layer of Ti forms a capping layer for all the samples. Nanosecond thermoreflectance measurements determine the total thermal resistance of the GST-electrode stacks. The results demonstrate the importance of sample processing in controlling thermal boundary

resistance. This data is essential for construction of future thermal models of PCM devices.

2.1.1 Sample Preparation

The multilayer samples were prepared by physical vapor deposition. Each sample consists of alternating layers of GST and one electrode material: Ti, TiN, or C. The GST layers vary in thickness between ~50 nm and 150 nm. The electrode materials have constant thickness targeted ~5 nm. The GST-C and low temperature $(GST\text{-}Ti)^{LT}$ samples were deposited at room temperature, leaving the GST in the as-deposited phase. The TiN layers in the $(GST\text{-}TiN)^{HT}$ stacks were reactively sputtered in a nitrogen-containing ambient environment using a titanium target. Electrical resistivity measurements indicate the GST films in the $(GST\text{-}TiN)^{HT}$ films partially crystallize into the FCC phase due to the elevated deposition temperature. The high temperature $(GST\text{-}Ti)^{HT}$ film is deposited above 135°C. Electrical resistivity measurements indicate the GST films in the high temperature $(GST\text{-}Ti)^{HT}$ stacks are deposited in the FCC phase. The thicknesses of all samples are confirmed using scanning electron microscope (SEM) images (fig. 2.3). Tables 2.1 and 2.2 show the stack thicknesses and deposition temperatures.

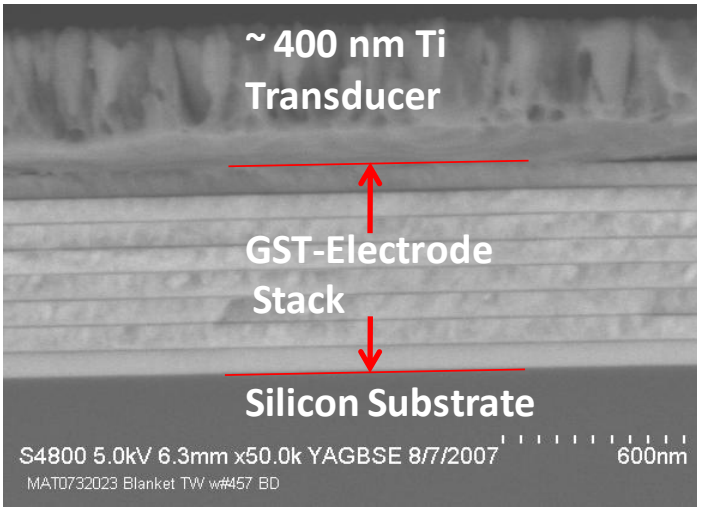

Fig. 2.3 Example GST-Electrode multilayer sample. Total stack thickness is ~ 680 nm, with a 400 nm Ti transducer layer.

Table 2.1 Thickness of GST and number of periods of GST-Electrode measured by SEM.

Sample	Stack 1 [nm] [# Periods]	Stack 2 [nm] [# Periods]	Stack 3 [nm] [# Periods]
(GST-C)[a]	305 (6)	649 (6)	930 (6)
(GST-C)[b]	643 (4)	639 (8)	629 (10)
(GST-TiN)^{HT}	270 (6)	520 (6)	680 (6)
(GST-Ti)^{LT}	322 (6)	633 (6)	970 (6)
(GST-Ti)^{LT}	335 (6)	623 (6)	890 (6)

Table 2.2 Chamber temperature during deposition of GST and electrode materials.

Sample	GST Deposition Temperature [^{o}C]	Electrode Deposition Temperature [^{o}C]
(GST-C)[a]	25	Not Regulated
(GST-C)[b]	25	Not Regulated
(GST-TiN)^{HT}	135	Not Regulated
(GST-Ti)^{LT}	25	Not Regulated
(GST-Ti)^{LT}	135	Not Regulated

2.1.2 Stack Resistor Model

The thermal conductivities of the stacks are extracted using a least squares fit of a solution of the three dimensional radially-symmetric heat diffusion equation for a multi-layered stack in response to a 6 ns surface heating pulse [48, 49]. Ambient temperature for the fit is 30 ^{o}C. Small changes in ambient temperature do not affect the fitting results because the thermal properties of the samples are not strong functions of temperature. The boundary condition between each layer is:

$$T_i(z_0) = T_{i+1}(z_0) + \frac{R_{i,i+1}}{\dot{q}_i} \tag{2.1}$$

where $R_{i,i+1}$ is the thermal boundary resistance. In this case, a single layer which includes both the interface and volumetric contributions to the thermal resistance models the behavior of the GST-Electrode stack. The data are fit with a single effective thermal conductivity of this layer. The heat capacity of GST is given by [87]. Although the solution takes into account thermal spreading, this effect is negligible and the heat transfer is one dimensional since the pump beam waist is significantly larger than the maximum thermal diffusion depth during the measurement. Since heat transfer is one dimensional, effective stack resistance can be interpreted in terms of a series of thermal resistances (fig. 2.4).

A trace is taken at ten different locations on the wafer. Averaging the fitted thermal conductivity from each trace reduces the effects of noise and film thickness variation. The standard deviation of thermal conductivity between individual traces makes up the error bars.

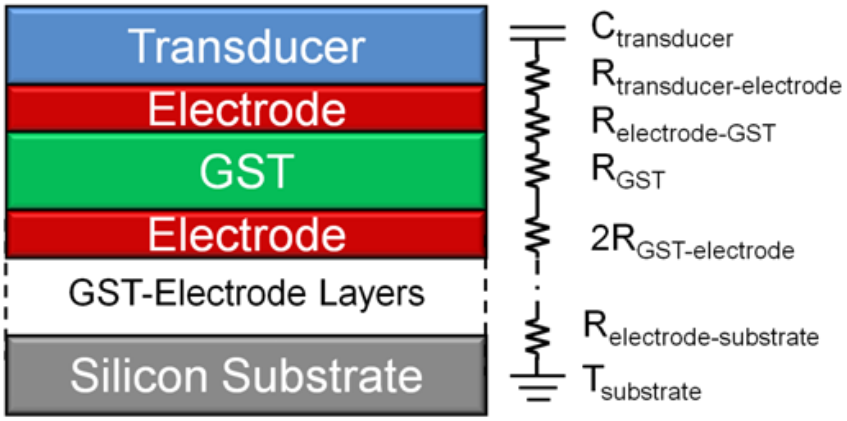

Fig. 2.4 Diagram of a 1-D multilayer resistance model. The intrinsic resistance of the transducer is negligible.

Within this 1-D framework, the thermal resistance of the stack increases linearly with GST thickness. The slope of stack resistance versus GST thickness determines the intrinsic GST conductivity. The zero-thickness value of total resistance becomes the total boundary resistance of the stack. Assuming that each boundary possesses the same resistance and that the electrode layers are thin enough so that their intrinsic resistance is

negligible, one may divide the zero-thickness thermal resistance by the total number of boundaries to determine the individual GST-electrode material TBR. The total resistance of the stack becomes:

$$R_{total} = \frac{t_{GST}}{k_{GST}} n + 2R_{GST-elec}(n+1) + \frac{t_{elec}}{k_{elec}}(n+1) + R_{trans-elec} + R_{elec-} \quad (2.2)$$

where t is material thickness, k is intrinsic thermal conductivity, and n is the number of layers in the stack. The thermoreflectance traces are fit starting from 100 ns after the peak, at which point the solution is insensitive to the transducer-electrode TBR. Further, since the characteristic decay time of the stack is significantly larger than the timescale of the measurement, the solution is also insensitive to the electrode-substrate TBR. Finally, since t_{elec} is small, the intrinsic electrode resistance can usually be neglected.

For the GST-C samples, the intrinsic resistance of the electrode material is too large to neglect even at such a small thickness. Assuming a thickness of 5 nm and a conductivity of 0.2 W m^{-1} K^{-1}, yields a volumetric resistance of 25 m^2 K GW^{-1}, which is on the order of most TBRs. Furthermore, the carbon thickness is difficult to determine due to its small size. Since each group of electrode samples is produced in the same batch run, one may assume that the electrode layer thickness is unknown but constant. As a result only the slope of the resistance-thickness curve is reliable. This determines only the intrinsic GST conductivity. To extract TBR, a set of samples with varying numbers of GST-electrode periods in each stack were deposited, maintaining a constant total GST material thickness. In this case, a plot of the total thermal resistances of these stacks against the numbers of GST-electrode period gives a straight line. The slope of this line determines the sum of GST-C TBR and carbon thermal resistance in each period of the stack.

Since the electrode layers in these samples are thin, there may be significant interdiffusion between the GST and electrode materials. As a result, the interface resistance may be due to both atomic disorder and an abrupt change in material properties [88]. Equation (2.2) assumes a discernible GST-electrode interface. Cross-sectional SEM data (fig. 2.3) of the samples demonstrate a noticeable material interface between the

GST and electrode layers. There is insufficient resolution to determine the electrode thickness or whether the electrode material forms a distinct interface with the surrounding GST. Since each GST layer sees two electrode boundaries, this analysis assumes two GST-electrode TBRs per layer.

2.1.3 Results

Figure 2.5 show the thermoreflectance results. For Carbon, TiN, and low temperature deposited $(GST\text{-}Ti)^{LT}$, the intrinsic GST conductivity ranges from 0.20 to 0.33 W m^{-1} K^{-1}. This is within the conductivity values reported in previous studies for amorphous GST [2, 30, 89]. The GST thermal conductivity values in the $(GST\text{-}Ti)^{LT}$ and $(GST\text{-}TiN)^{LT}$ stacks, are slightly higher than previous reports, indicating that a small degree of crystallization may be taking place during the deposition process. The intrinsic conductivity of GST for the $(GST\text{-}Ti)^{HT}$ sample is 0.69 W m^{-1} K^{-1}, higher than the results reported for the FCC phase. This suggests that partial crystallization into the HCP phase may be occurring [65, 89].

The GST-C TBR plus the intrinsic carbon resistance is 40 m^2 K GW^{-1}, as depicted in figure 2.5. Taking into account the reported 5 nm of carbon, this gives a TBR of 27.5 m^2 K GW^{-1}, with a potential error of ±6 m^2 K GW^{-1} due to uncertainty in carbon thickness [90]. This TBR corresponds to ~5 nm of carbon. The $(GST\text{-}Ti)^{LT}$ TBR is 49.8 m^2 K GW^{-1}, equivalent to ~1000 nm of Ti. This is reduced to 11.4 m^2 K GW^{-1} for $(GST\text{-}Ti)^{HT}$, equivalent to ~200 nm of Ti. The $(GST\text{-}TiN)^{HT}$ TBR is lowest of all, with 5.2 m^2 K GW^{-1}, equivalent to ~150 nm of TiN. Table 2.3 reports the collected data.

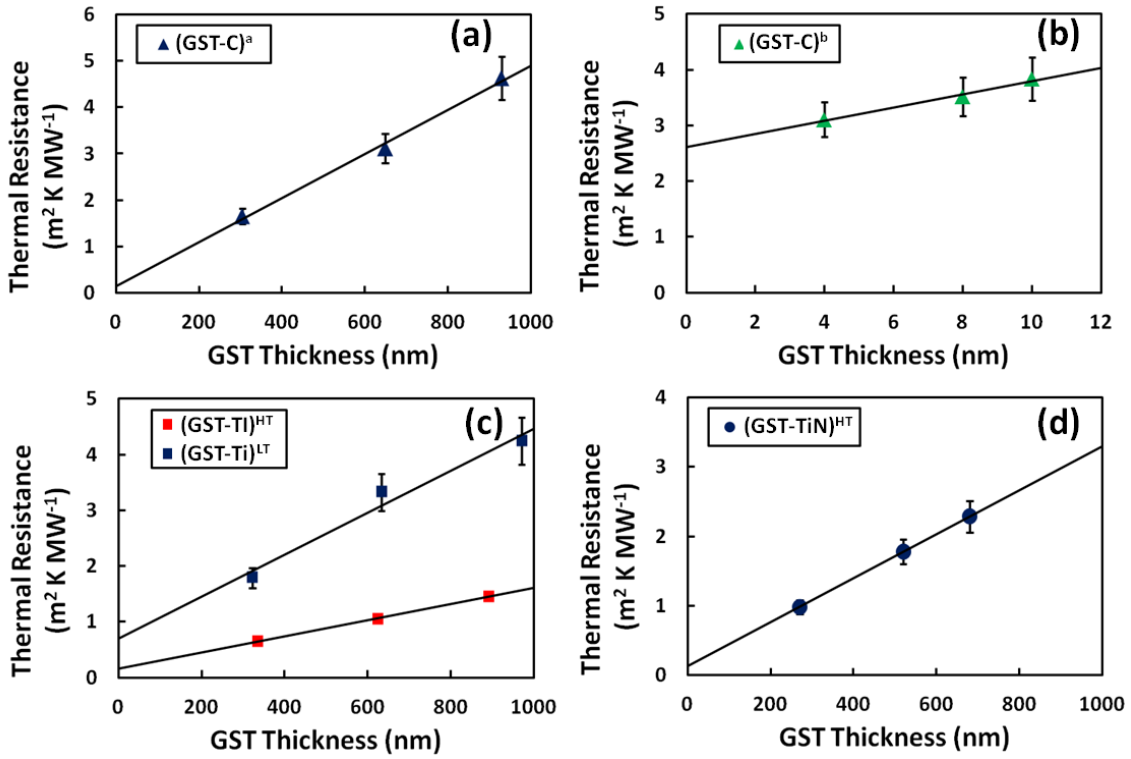

Fig. 2.5 Plot of total stack resistance versus thickness for (a) $(GST\text{-}C)^{a}$. Slope indicates GST conductivity is 0.20 W m^{-1} K^{-1}, (b) $(GST\text{-}C)^{b}$. Slope indicates GST-C TBR + Carbon resistance = 40 m^2 K GW^{-1}, (c) $(GST\text{-}Ti)^{LT}$ and high temperature deposited $(GST\text{-}Ti)^{HT}$. Slopes indicate GST conductivities are 0.27 and 0.69 W m^{-1} K^{-1} respectively. GST-Ti TBRs are 49.8 and 11.4 m^2 K GW^{-1} respectively, and (d) $(GST\text{-}TiN)^{HT}$. Slope indicates GST conductivity is 0.33 W m^{-1} K^{-1}. $(GST\text{-}TiN)^{HT}$ TBR is 5.2 m^2 K GW^{-1}

Table 2.3 Collected GST-Electrode results. a) Constant layer count. b) Constant stack thickness

Sample	Intrinsic k_{GST} [W m^{-1} K^{-1}]	TBR [m^2 K GW^{-1}]
$(GST\text{-}C)^{a}$	0.20 ± 0.01	N/A
$(GST\text{-}C)^{b}$	N/A	27.5 ± 6
$(GST\text{-}TiN)^{HT}$	0.33 ± 0.017	5.20 ± 0.25
$(GST\text{-}Ti)^{LT}$	0.27 ± 0.014	49.8 ± 2.5
$(GST\text{-}Ti)^{LT}$	0.69 ± 0.035	11.4 ± 0.6

The intrinsic conductivity of GST in the $(GST\text{-}C)^{a}$ stack is the lowest of all the samples. Due to the low temperature deposition procedure for carbon, no crystallization takes place in the GST. Since the GST-C TBR is moderately high compared to other material interface resistances, and since the intrinsic thermal resistance of carbon is high, a carbon electrode can impede the loss of heat from a PCM cell, resulting in a large thermal decay time. This may lower the programming current necessary to switch the device.

The $(GST\text{-}TiN)^{HT}$ sample has higher intrinsic GST conductivity due to the higher deposition temperature. This most likely causes partial formation of the FCC crystalline phase in the GST. High temperature deposition processes are acceptable because the device can be reset. Furthermore, the $(GST\text{-}TiN)^{HT}$ TBR is very small, resulting in a small thermal decay time. Reifenberg et al. report a room temperature $(GST\text{-}TiN)^{HT}$ TBR of ~ 26 m^2 K GW^{-1} for samples of GST between two layers of TiN [34]. This measurement, performed using picosecond TDTR, used samples with TiN thickness greater than 10 nm. These thicker TiN films may possess a higher degree of surface roughness, resulting in a larger TBR than reported here. The low TBR between GST and TiN implies a higher programming current necessary to switch the device.

For the $(GST\text{-}Ti)^{LT}$ stack, the intrinsic conductivity of the GST is slightly higher than expected for amorphous GST, indicating a small amount of crystallization may be occurring. The $(GST\text{-}Ti)^{HT}$ exhibits partial HCP crystallization. This is not an issue for device fabrication since the cell switches easily between the amorphous and crystalline states. The difference in TBR between the $(GST\text{-}Ti)^{LT}$ and $(GST\text{-}Ti)^{HT}$ stacks demonstrates the importance of deposition method on device performance. Depending on the temperature of deposition, the thermal decay time and programming current of the device change. A higher deposition temperature results in a lower thermal decay time for the device, implying a higher programming current is necessary. Accordingly, PCM designers must be careful to choose fabrication processes and electrode materials that will result in devices with desirable thermal properties.

2.2 Thermal Properties of Multilayer Electrodes

The switching behavior of a PCM cell depends upon several factors, including: device size [91], applied fields [92], and the temperature gradient developed at the electrode-device interface [91]. The latter property is influenced by the thermal resistances of the device. Reifenberg et al. demonstrated through coupled electrical-thermal simulations that the programming current of a GST-based device decreases as the total thermal resistance of the cell increases [91]. Further, Karpov and Kostylev showed that much of the heat generated during GST cell switching occurs in the GST bulk and at the electrode interface [93]. For this reason, one of the goals in PCM thermal design is to minimize heat loss from the cell. Heat loss through the electrode dominates in many PCM cell geometries. Electrode materials with low thermal conductivities and larger TBR can therefore reduce heat loss in PCM cells. The TBR is a function of several properties, including phonon spectra and interface quality [94, 95]. Previous work shows data for GST-electrode TBR in the range of 5 to 50 m^2 K GW^{-1} [35, 96]. However, as shown in the previous section, electrodes with low thermal conductivity may not have high TBR. For electrode materials such as C, Ti, and TiN, TBR becomes comparable to intrinsic thermal resistance when their thicknesses approach ~ 30 nm. As such, there may not be a single composition electrode material which is suitable for use at multiple thickness scales. Therefore, designers must consider new ways to utilize the GST-electrode TBR while increasing the intrinsic electrode thermal resistance.

In order to minimize the heat loss from a GST cell, a multilayer electrode stack was proposed. The presence of the material interfaces in these electrodes would contribute significantly to the total thermal resistance of the stack. Further, the bottom film of the stack can be chosen to maximize the GST-electrode TBR, which impedes heat loss from the PCM cell and reduces the programming current [91].

This section demonstrates measurements and assesses the importance of TBR in three prospective PCM electrode materials. Samples are measured as-deposited and after a 5 minute anneal at 400 ^{o}C. A picosecond thermoreflectance setup interrogates the thermal properties of the samples in an optical access oven. Multilayer stacks of electrode materials are measured to determine the electrode-electrode TBR for C-TiN and W-WN_x.

Temperature-dependent measurements of all samples determines thermal conductivity and TBR in the range of 25 to 400 ^{o}C.

2.2.1 Sample Preparation

All samples were deposited using magnetron sputtering. Tungsten deposition utilized DC power and argon plasma. Carbon deposition used pulsed-DC power at 90 kHz with argon plasma. TiN and WN_x were both deposited using DC power and reactive argon-nitrogen plasma with, respectively, pure titanium and pure tungsten sputtering targets. The multilayer samples underwent similar deposition, without air breaks in the C-TiN or W-WN_x layers.

Single-layer samples of each film ranged in thickness from 25-100 nm. The multilayer stacks consisted of 5 periods of W/WN_x (70 nm/100 nm) or C/TiN (11 nm/110 nm). A 50 nm aluminum layer acts as the transducer film. Annealed samples were held for 5 minutes at 400 ^{o}C, with ramp-up taking less than 60 minutes and cool down taking less than 30 minutes.

2.2.2 High Temperature TDTR

For the film compositions in this work, and at times scales below ~400 ps, the thermal decay time of the transducer layer is dependent on the heat capacitance of the film and the Al-electrode TBR, such that at short times, $\tau \sim R_{Al\text{-}electrode}C_{Al}$, where C_{Al} is the volumetric heat capacity multiplied by the aluminum film thickness. During this time period, the thermal decay behavior is sensitive to only the transducer-electrode TBR. As a result, the TBR is uniquely separable from the electrode thermal conductivity [35]. For the multilayer samples, the model fits an effective thermal resistance for each individual electrode layer. For the W-WN_x sample, this becomes an effective thermal conductivity for each electrode material type. The total thermal resistance of a W-WN_x pair is calculated, and the intrinsic thermal resistances of the WN_x and W layers are subtracted out, leaving a resistance equal to twice the W-WN_x TBR. For W, the intrinsic conductivity is obtained by scaling the bulk conductivity to account for boundary scattering. For the C-TiN sample, since the carbon layers are very thin, the model treats the stack as several layers of TiN with equal TBR between each layer. This TBR term

includes the intrinsic carbon resistance and the C-TiN TBR. Subtracting out the intrinsic C thermal resistance leaves a resistance equal to twice the C-TiN TBR.

2.2.3 Results

All single-layer samples exhibit a decrease in total area-normalized thermal resistance ($R_{total}=L_{electrode}/k_{electrode} + R_{Al\text{-}electrode} + R_{electrode\text{-}si}$) as temperature rises, with the as-deposited samples showing significant temperature hysteresis. After separating out the TBR terms from the total resistance, only the titanium nitride sample shows an increase in intrinsic thermal conductivity after annealing (fig. 2.6). This may be due to a decrease in defect density within the TiN film, resulting in a higher phonon mean free path. In all other cases, the thermal resistance decreases due to annealing of the material interfaces (Table 2.4). Conducting the same measurement on the annealed samples demonstrates the hysteresis effect is no longer visible (fig. 2.7). This indicates that the five minute anneal time is sufficient to promote temperature stability of single-layer electrode thermal properties. The data shown in figures 2.6 and 2.7, as well as table 2.4, form the fitting parameters for the multilayer stacks. Error due to signal noise is small. As a result, electrode thickness uncertainty controls the error bars.

Table 2.4 Thermal boundary resistances of single layer stacks.

Sample	$R_{Al\text{-}elec}$ [W m^{-1} K^{-1}]	$R_{Al\text{-}elec,annealed}$ [m^2 K GW^{-1}]	$R_{elec\text{-}Si}$ [m^2 K GW^{-1}]	$R_{elec\text{-}Si,annealed}$ [m^2 K GW^{-1}]
C	4.3	3.9	2.3	2.0
TiN	1.1	1.7	3.6	3.9
WN_x	4.4	3.3	8.8	6.6

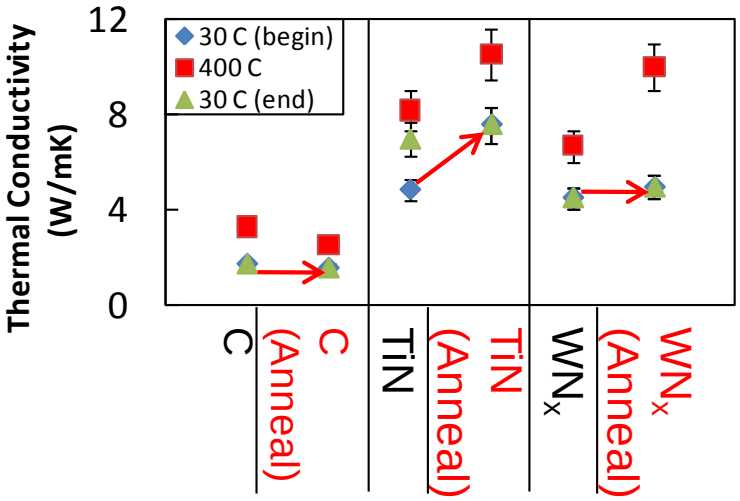

Fig. 2.6 Thermal conductivity of the single-layer electrode samples. The red arrows indicate the change of room temperature conductivity between the as-deposited and post-annealed samples. Error bars are due to uncertainty in sample thickness.

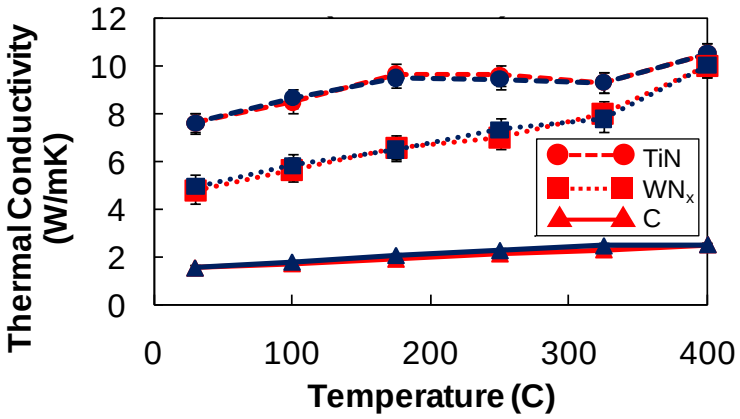

Fig. 2.7 Thermal conductivity of the post-annealed single-layer samples. The red (light) points indicate the heating curve, and the blue (dark) points indicate the cooling curve. Hysteresis effects are not visible for these samples.

Both annealing time and temperature impact the thermal conductivity of the TiN and WN_x films. Annealing these samples before conducting high temperature measurements results in a higher thermal conductivity at 400 ^{o} C than for the as-deposited films. This may be due to the annealed samples spending a greater total amount of time at elevated temperature. As a result, the annealed samples would have a lower dislocation density than the as-deposited samples, resulting in a higher thermal conductivity.

For the multilayer stacks, W-WN_x exhibited a small decrease in thermal boundary resistance due to annealing, from 3.9 m^2 K GW^{-1} to 3.6 m^2 K GW^{-1}, comparable to

roughly 20 nm of WN_x film at room temperature (fig. 2.8). The annealed sample showed no temperature hysteresis. The C-TiN multilayer, on the other hand, showed a significant increase in the apparent TBR after annealing, from 4.9 m^2 K GW^{-1} to 11.9 m^2 K GW^{-1}. This is comparable to roughly 40 nm and 100 nm, respectively, of TiN at room temperature. Since the carbon layers were roughly 10 nm thick, interdiffusion from the TiN layers at high temperature may have resulted in a highly disordered film rather than a solid interface [97]. Interdiffusion in this disordered layer would significantly decrease the phonon mean free path due to impurity scattering, resulting in a lower thermal conductivity. The measured thermal conductivity is therefore representative of an elementally heterogeneous film. The absence of a sharp material interface in this film implies the need for careful interpretation of the extracted TBR. For this reason, figure 2.8 defines an apparent TBR using the intrinsic carbon thermal conductivity determined from the single layer samples.

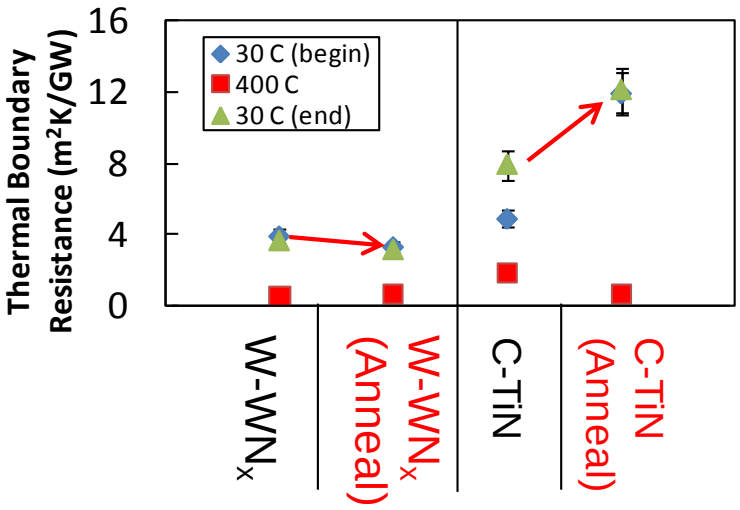

Fig. 2.8 Thermal boundary resistance electrode multilayer samples. The red arrows indicate the change of room temperature TBR between the as-deposited and post-annealed samples. Error bars are due to uncertainty in the thickness of the electrode films.

Although the electrode-electrode TBR decreases at high temperature, it remains an important contributor to electrode thermal resistance. For annealed W-WN_x, the TBR at 400C (0.5 m^2 K GW^{-1}) is equivalent to 5 nm of WN_x at the same temperature. For annealed C-TiN, the TBR at 400C (0.6 m^2 K GW^{-1}) is equivalent to 6 nm of TiN at the same temperature. In both cases, the TBR at high temperature accounts for ~ 10% of the

total resistance of the multilayer stack ($R_{total,multilayer} = L_{electrode,1}/k_{electrode,1} + L_{electrode,2}/k_{electrode,2} + 2R_{electrode,1\text{-}electrode,2}$).

These results demonstrate that multilayer stacks exhibit significant increases in thermal resistance relative to single material electrodes. This additional resistance can reduce the programming current in many PCM cell geometries. Specifically, C-TiN electrode stacks offer both high intrinsic resistance and high thermal boundary resistance. Annealing gives control over the thermal resistances of the PCM cell. It may also lead to further incorporation of titanium and nitrogen into the carbon layer. This makes it difficult to define a solid material interface. As such, the results presented here define an apparent boundary resistance based on the anticipated intrinsic thermal resistance of the carbon layer.

The improved thermal properties of these materials alone will not necessarily lead to a reduction in programming current. The PCM cell geometry and dimensions will influence whether the electrode material is the dominant path for heat loss from the GST cell. The device designer may choose to alter the periodicity of these multilayer materials in order to control the electrode thermal resistance. By using such design techniques with the above materials, one can control the thermal decay time of the memory cell, and therefore the programming current.

2.3 Electron and Phonon Thermal Transport in $Ge_2Sb_2Te_5$

In the amorphous and FCC phases, thermal conduction in GST is primarily phonon energy transport. However, in HCP-GST, electrons contribute to thermal conduction on the same order as phonons. This added energy transfer route affects not only the intrinsic thermal conductivity of the film, but the TBR as well. Existing models for TBR rely on the principle of acoustic [84] or diffuse [83] reflection of phonons at a material interface. Although there are theories that expand these models to include both electron and phonon conduction [98, 99], these models operate on the assumption that one of the materials involved completely restricts electron heat transfer. In the case of a PCM device, in which HCP-GST is in contact with an electrically-conductive electrode, such theories may not be appropriate for estimating TBR.

To understand the difference in GST-electrode TBR due to the contributions of electron and phonon conduction, we performed picosecond TDTR measurements on a TiN-GST-TiN stack subjected to annealing temperatures in the range of 25 ^{o}C to 300 ^{o}C. This temperature range allows us to extract the phase and annealing dependence of the GST thermal conductivity and GST-TiN TBR. For these measurements, we deposited two sets of samples. First, a 35 nm thick TiN film is deposited directly on a silicon wafer by reactive sputtering of a Ti target in nitrogen ambient. Then, either a 30 nm or a 167 nm thick GST film is deposited by radio frequency sputtering in argon ambient. The substrate temperature during the deposition is maintained at 25 ^{o}C. Then, an 80 nm thick TiN and a 50 nm thick Al films are deposited sequentially without breaking the vacuum. Finally, we anneal these samples at temperatures from 25 °C to 300 °C to induce crystallization in the GST films, and observe how crystallization affects both GST thermal conductivity and GST-TiN TBR.

2.3.1 Phonon Thermal Conduction in $Ge_2Sb_2Te_5$

The acoustic properties of FCC- and HCP-GST do not differ significantly. The volumetric heat capacities [2] and average phonon velocities [30] of the two phases differ by less than 3%. Further, the phonon mean free path (MFP) in GST (< 1 nm) is significantly less than the average grain size (20-30 nm) [100]. As a result, grain growth due to sample annealing does not affect the average phonon MFP. Since we obtain thermal conductivity (k_p) from heat capacity (C), carrier velocity (v_p), and average MFP (λ_p), where $k_p = \frac{1}{3} C v_p \lambda_p$, it is unlikely that the phonon thermal conductivity differs significantly between FCC- and HCP-GST. As a result, we can define a crystalline GST phonon conductivity, $k_{p,FCC/HCP}$. However, the thermal conductivity of HCP-GST is roughly 4 times that of FCC-GST. The difference in thermal conductivity between the two phases of crystalline GST comes from a dramatic increase in the hole concentration and mobility in HCP-GST [30]. This results in an expected electron thermal conductivity of ~ 1.1 W m^{-1} K^{-1}, which we define as $k_{e-,HCP}$. This accounts for ~ 75% of the total thermal conductivity of HCP-GST (fig. 2.9).

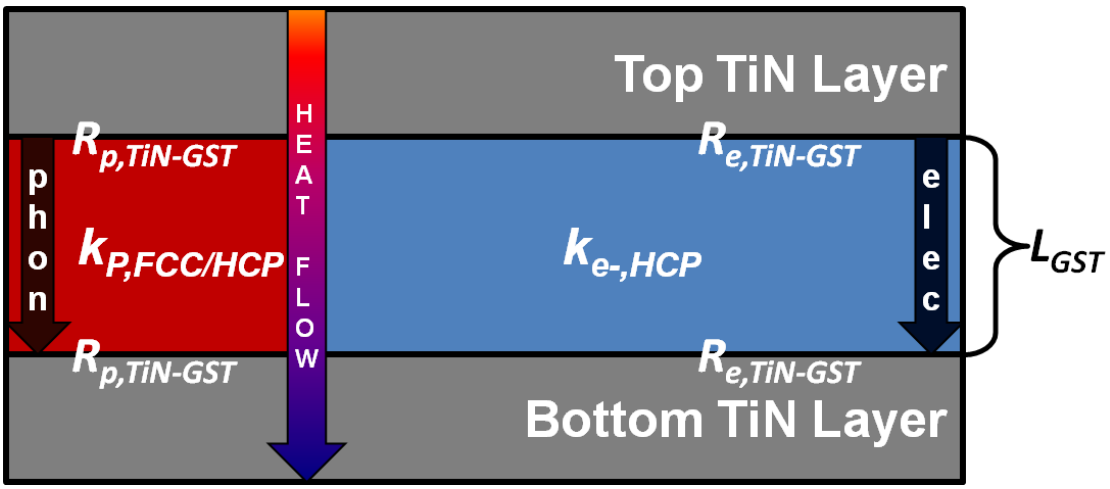

Fig. 2.9. The red and blue regions indicate the relative contributions of phonons and electrons, respectively, to thermal conductivity in HCP-GST. The phonon and electrons components of TBR are indicated as well.

The additional energy transfer route offered by electrons in HCP-GST does more than increase the intrinsic thermal conductivity of the film. It also offers an additional mechanism for energy transfer across the GST-electrode interface. Electron interface conduction occurs in parallel with phonon interface conduction. As a result, even though FCC- and HCP-GST have similar acoustic properties, one might anticipate a reduction in the GST-TiN TBR for HCP-GST due to the addition of electrons as interfacial energy carriers.

2.3.2 Experimental Method

To access the thermal properties shown in figure 2.9, we must limit the thermal measurement region to the TiN-GST-TiN sandwich structure. We achieve this using picosecond TDTR to temporally confine the measurement. The thermal properties at different points within the stack affect different time domains of the thermal decay trace (fig. 2.10). These domains correspond to different thermal penetration depths, which are determined by the measurement time scale and the thermal time constant of different regions within the sample. The thermal time constant of the Al transducer controls the behavior of the first 0.5 ns after the arrival of the pump beam (Region I). This time constant includes the total capacitance of the transducer, the intrinsic Al thermal resistance, and the Al-TiN TBR. Since the intrinsic resistance of the 50 nm Al layer is

small, and since the heat capacity is well known, we extract the Al-TiN TBR (3 m^2 K GW^{-1}). From ~0.5 ns to ~2.5 ns after the pump pulse arrives, the thermal resistance of the top TiN layer and underlying GST dictate the decay behavior (Region II). Since the thermal conductivity of TiN is well-characterized [51], we extract a combination of the intrinsic GST thermal resistance and the GST-TiN TBR. Lastly, the thermal decay behavior from ~2.5 ns to before the arrival of the next pump pulse is sensitive to the total resistance of the TiN-GST-TiN stack (Region III). Our knowledge of the TiN thermal conductivity allows us to obtain the combination of the intrinsic GST thermal resistance and both GST-TiN TBRs. Under the assumption that TBR does not differ significantly for the two GST-TiN interfaces, and using the results from Region II, we separate out the intrinsic GST thermal conductivity. Transmission electron microcopy validated that roughness and phase distribution near top and bottom interfaces are nearly identical for $Ge_2Sb_2Te_5$ films that are deposited as amorphous phase and interfaced with same materials at the top and the bottom [100]. This supports the assumption of a similar GST-TiN TBR for both interfaces.

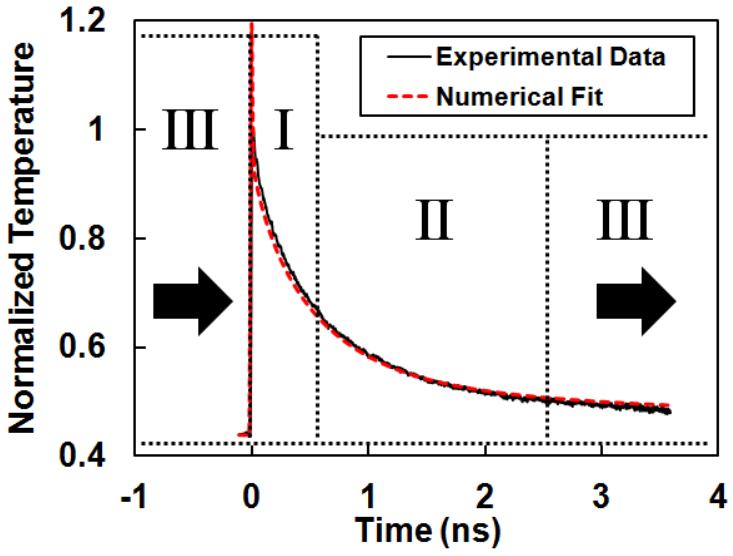

Fig. 2.10. Representative thermal decay trace (with temperature normalized by the peak experimental value) for the 167 nm GST sandwich structure. Each temporal domain (I, II, and III) is sensitive to a different set of thermal properties within the GST-TiN GST stack. I) Al-TiN TBR. II)Top TiN-GST TBR and GST thermal conductivity. III) Both TiN-GST TBRs and GST thermal conductivity.

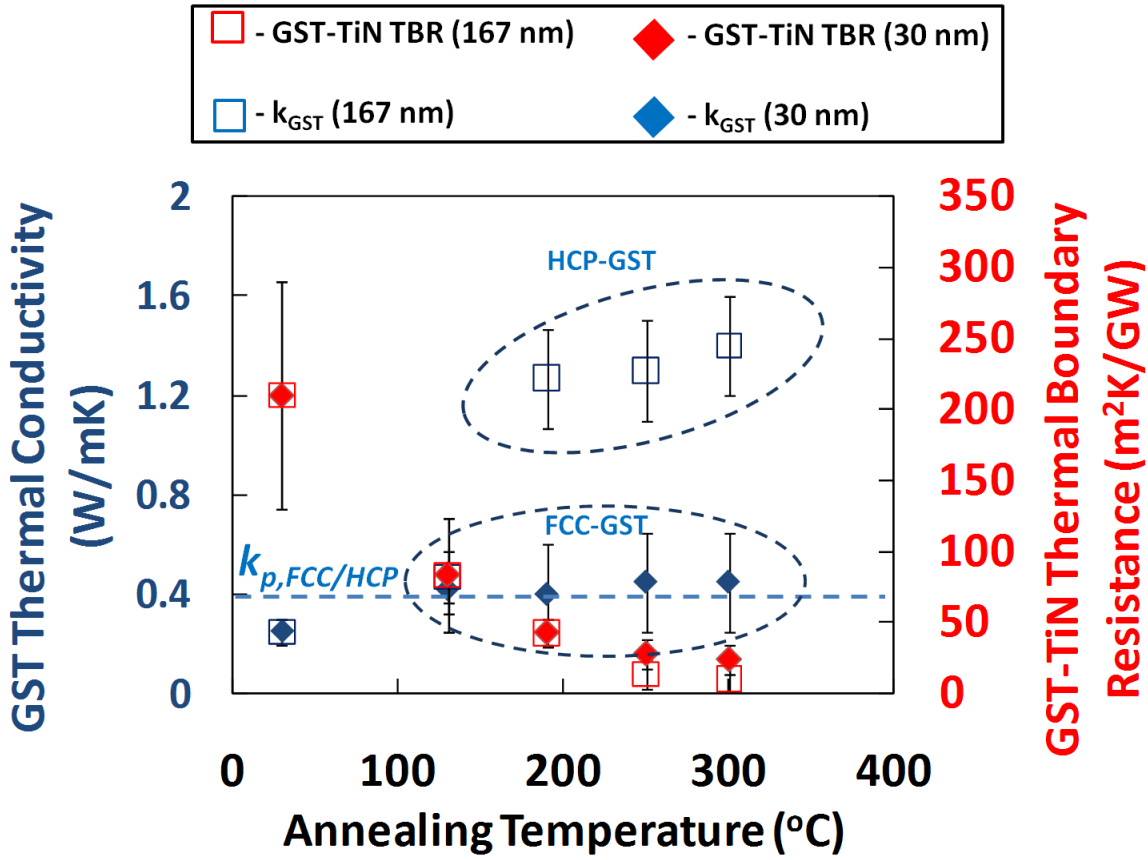

Fig. 2.11. GST thermal conductivity and GST-TiN TBR as a function of annealing temperature for both the 30 nm (diamond markers) and 167 nm (square markers) samples. The phonon contribution to HCP- and FCC-GST conductivity ($k_{p,FCC/HCP}$) is indicated with a dotted line.

2.3.3 Results

Figure 2.11 reports the GST thermal conductivity and GST-TiN TBR as a function of annealing temperature for both the 30 nm and 167 nm GST films. From the data, we see that thermal conductivity and TBR for both film thicknesses match up when annealed at temperatures less than 190 ^{o}C. However, past this point, the 167 nm film thermal conductivity rapidly increases while the 30 nm film thermal conductivity remains around $k_{p,FCC/HCP}$. X-ray diffraction analysis of the samples demonstrates that the 30 nm film remained in the FCC phase, while the 167 nm film switched to HCP. Even annealing to 300 ^{o}C did not cause the 30 nm film to crystallize into HCP. For both films, however, we saw a decrease in TBR with annealing temperature past 190 ^{o}C. Further, the TBR decreased faster for the HCP film than for the FCC film. After annealing at 300 ^{o}C, the

GST-TiN TBR was found to be 10.6 ± 10 m^2 K GW^{-1} for the 167 nm film and 24 ± 10 m^2 K GW^{-1} for the 30 nm film. The 30 nm results agree with data reported by Reifenberg et al. for FCC-GST [34]. As a comparison, the diffuse mismatch model of TBR using measured heat capacity [101]:

$$R_{pp} = \left(\frac{\sum_j c_{2,j}^{-2}}{12\left(\sum_j c_{1,j}^{-2} + \sum_j c_{2,j}^{-2}\right)} c_{1,d}^3 \sum_j c_{2,j}^{-2} \right)^{-1} C_1(T)^{-1} \tag{2.3}$$

predicts a GST-TiN TBR of 15 m^2 K GW^{-1} for the FCC phase and 13 m^2 K GW^{-1} for the HCP phase. In the above equation, $c_{i,j}$ is the sound speed in material i for phonon mode j, $c_{i,d}$ is the polarization averaged sound speed in material i, and $C_1(T)$ is the volumetric heat capacity in material 1 at temperature T.

The large error bars present in our TBR results make it difficult to discern whether electrons are aiding in interface transport or if structural changes are taking place at the interface (i.e. reduction in phase impurities or defects). Further measurements on the GST-TiN interface using a Cross-Bridge Kelvin Resistor [102, 103] and a linear transfer length method demonstrated an electrical contact resistance of 84 ± 8 Ω μm^2 for the FCC film annealed at 300 ^oC and 7 ± 2 Ω μm^2 for the HCP film annealed at 300 ^oC. Applying the Wiedemann-Franz-Lorenz (WFL) law at the interface to these results [98], we find the GST-TiN electron TBR is 11500 ± 1100 m^2 K GW^{-1} for FCC-GST and 950 ± 300 m^2 K GW^{-1} for HCP-GST. Even though the electron TBR drops by an order of magnitude from FCC to HCP, and even though electrons account for 75% of the thermal energy transfer in HCP-GST, the electron TBR it is still 2-3 orders of magnitude higher than the phonon TBR. This indicates our results on GST-TiN TBR are primarily from phonon interface conduction.

Eliminating electrons as interface energy carriers, however, does not necessarily eliminate electrons from contributing to interface conduction. If an electron emits a phonon which carries thermal energy across the interface, it can still reduce the TBR. The addition of phonons to the interface is equivalent to increasing the heat capacity in equation (2.3). If more carriers are available, heat capacity increases, and the TBR decreases. Using this approach, we can rule out electron-phonon coupling as the source

of the TBR reduction. Assuming instantaneous electron-phonon coupling at the interface (maximizing the potential benefit from adding electrons as carriers), we find the heat capacity becomes:

$$C_1(T) = C_e(T) + C_p(T) = \gamma T + \frac{12\pi^4}{5} n_a k_B \left(\frac{T}{\theta_D}\right)^3 \quad (2.4)$$

where $C_p(T)$ is the phonon heat capacity, $C_e(T)$ is the electron heat capacity, γ is the Sommerfeld parameter, n_a is the number density of the material, k_B is Boltzmann's constant, and θ_D is the Debye temperature. The phonon heat capacity in GST at room temperature is ~1.3x10^6 J m^{-3} K^{-1}. The Sommerfeld parameter is on the order of 10 J m^{-3} K^{-2}, meaning that electron heat capacity is ~3x10^3 J m^{-3} K^{-1} at room temperature. With this value, even if every electron in the HCP-GST film could instantaneously couple its energy to a phonon as it reached the interface, it would not have a significant effect on the heat capacity or TBR. Therefore, we can rule out electrons as interface energy carriers, implying that the difference in GST-TiN TBR between the FCC and HCP films annealed above 190 ^{o}C is likely related to structural changes at the interface.

In summary, this section identifies the contributions of electrons and phonons to heat conduction between the phase change material GST and a TiN electrode. We annealed samples of TiN-GST-TiN from room temperature to 300 ^{o}C, and observed that the thinner sample remained in the FCC phase while the thicker sample switched to HCP. Since both films were subjected to the same anneal conditions, and since FCC- and HCP-GST have similar acoustic properties, we were able to measure the respective contributions of electrons and phonons to heat conduction both intrinsically and at the GST-TiN interface. We showed HCP-GST experiences a significant reduction in TBR compared to FCC-GST annealed at the same temperature, but there is no significant electron thermal transport across the interface. Even if the electrons couple their energy to phonons which subsequently cross the interface, the additional carriers have a negligible effect on the total TBR. This information enhances our understanding of the thermal processes at play in all three phases of a GST-TiN interface, enabling greater control over the switching properties of a phase change memory cell.

Chapter 3
Diamond Substrates for High Electron Mobility Transistors

High electron mobility transistors (HEMT) based on GaN semiconducting layers offer a variety of challenges related to fabrication, design, and thermal management. An AlGaN-GaN heterojunction creates a highly conductive 2-dimensional electron gas (2DEG) confined between semiconducting layers [104]. This high electron mobility layer arises due to band bending at the AlGaN-GaN interface, where the conduction band briefly dips below the Fermi level [105]. By depositing source and drain structures contacting the 2DEG and a gate structure on top of the AlGaN layer, one can manipulate the electron layer in a similar manner to Si-based field effect transistors (FET). However, such transistors are capable of faster response times and higher AC operating frequencies than Si-based FETs [106]. The wide bandgap and high breakdown voltage of the AlGaN-GaN heterojunction allow greater power to be pumped through the device [107], and the high thermal conductivity substrates facilitate thermal management of such large power densities [106]. This ability to operate faster at higher power than Si-based FETs makes HEMT devices attractive for applications involving amplification of radio-frequency and microwave radiation [106, 108].

Due to the large power densities present in HEMT devices, thermal management is a critical issue. Because the substrate is a key contributor to the total thermal resistance, considerable attention is paid to substrate selection. The current preferred substrate is SiC, with diamond substrates being proposed to allow for even greater power

densities. A transition layer, based on AlN, usually sits between the HEMT structure and the substrate in order to promote the growth of high-quality GaN buffer films (fig. 3.1) [109].

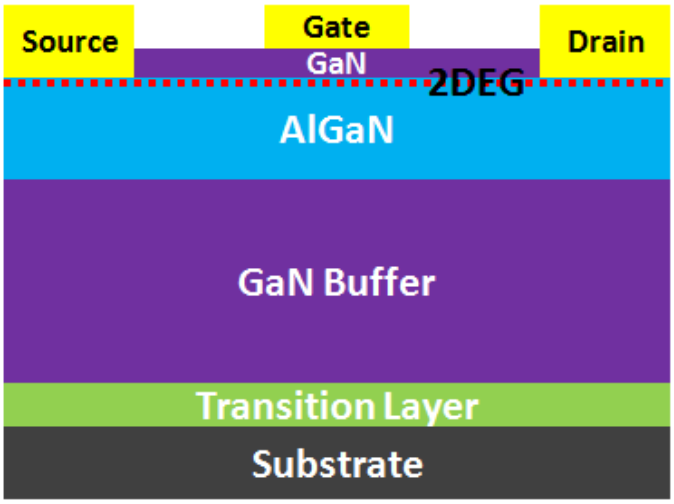

Fig. 3.1 A representative HEMT structure based on the AlGaN/GaN heterojunction.

3.1 Thermal Spreading Analysis for Comparison of SiC and Diamond Substrates

Since the buffer layer and substrate are high quality crystalline films with much lower dislocation and impurity density than the transition layer, it is likely that the dominant thermal resistances in the HEMT system will be that of the disordered low-quality buffer region near the transition layer, and the buffer-substrate interface. The latter resistance, expressed as:

$$R_{tran} = R_{GaN-tran} + \frac{d_{tran}}{k_{tran}} + R_{tran-sub} \tag{3.1}$$

includes the GaN-transition layer thermal boundary resistance ($R_{GaN\text{-}tran}$), the intrinsic thermal resistance of the transition layer due to the thickness (d_{tran}) and thermal conductivity (k_{tran}) of the transition layer, and the transition layer-substrate thermal boundary resistance ($R_{tran\text{-}sub}$). The TBR components of R_{tran} are due to two main factors. First, the acoustic impedance mismatch between the two materials at an interface produces an effect similar to Snell's Law, where phonons transmit or reflect with a

probability determined by the mismatch [83, 84]. The Diffuse Mismatch Model expresses this transmissivity as [83]:

$$\alpha_{1\to 2} = \frac{\sum_j c_{2,j}^{-2}}{\sum_j c_{1,j}^{-2} + \sum_j c_{2,j}^{-2}} \tag{3.2}$$

where $\alpha_{1\to 2}$ is the probability a phonon will transmit from material 1 to material 2 and $c_{i,j}$ is the sound speed in material i for polarization j. Using this result, one can calculate TBR using the simplified relation [101]:

$$R_{1\to 2} = \left(\frac{\alpha_{1\to 2}}{12} c_{1,d}^3 \sum_j c_{1,j}^{-2} \right)^{-1} C_1(T)^{-1} \tag{3.3}$$

where $c_{1,d}$ is the polarization-averaged sound velocity in material 1 and $C_1(T)$ is the temperature-dependent volumetric heat capacity. Second, the presence of impurities, defects, or small grains near the interface may significantly reduce the mean free path of nearby energy carriers. This increases the thermal resistance beyond the value expressed in equation (3.3).

The transition layer resistance complicates the discussion of minimizing the thermal resistance between the HEMT device and the cooling solution. As mentioned before, diamond substrates, with thermal conductivities reported to be on the order of 2000 W m^{-1} K^{-1} [110], are seen as an appropriate replacement for existing SiC substrates. However, if the total resistance of the transition layer is large enough, it can outweigh the thermal resistance improvements offered by using a diamond substrate.

For example, let us compare the thermal resistances of a hotspot on a GaN/SiC or GaN/Diamond structure using a simple heat spreading analysis. In this approach, assume a hotspot of varying width (w) and length (L) on top of the GaN/Substrate stack. The spreading resistance for such a hotspot on an arbitrary substrate is given by [111]:

$$R_{spreading} = \frac{1}{Sk_{sub}} = \frac{1}{2\sqrt{\frac{wL}{\pi}} k_{sub}} \tag{3.4}$$

where S is a shape factor determined by the heating geometry and k_{sub} is the thermal conductivity of the substrate. Between the GaN and substrate layers is a thermal boundary resistance. This TBR impedes heat flow and affects the healing length of the hotspot within the GaN layer [112]:

$$L_h = \sqrt{d_{GaN} k_{GaN} \left(\frac{d_{sub}}{k_{sub}} + R_c \right)} \tag{3.5}$$

where d_{GaN} is the thickness of the GaN layer, k_{GaN} is the thermal conductivity, and R_c is the TBR between the GaN and substrate. This healing length dictates the area over which heat diffuses from the interface into the substrate. Using this information, the total thermal resistance experienced by the hotspot is given by:

$$R_{total} = \frac{1}{2\sqrt{\frac{wL}{\pi}} k_{GaN}} + \frac{R_c}{(w + 2L_h)L} + \frac{1}{2\sqrt{\frac{(w + 2L_h)L}{\pi}} k_{sub}} \tag{3.6}$$

The first term in this sum will be the same for SiC and diamond substrates. Comparisons of different GaN-substrate combinations will focus on the last two terms.

For example, consider a hotspot generated by a HEMT gate with length 100x its width (fig. 3.2). For transition layer resistances above 20 m^2K/GW, the combined substrate and boundary thermal resistance for device widths on the order of 10 nm is larger for diamond than for SiC. This situation would arise if: 1) more transition layer material is required to handle the lattice mismatch between diamond and GaN, 2) the mismatch in acoustic properties between the two films produces a much larger thermal boundary resistance, or 3) the defect density within the transition layer is higher due to mismatch stresses.

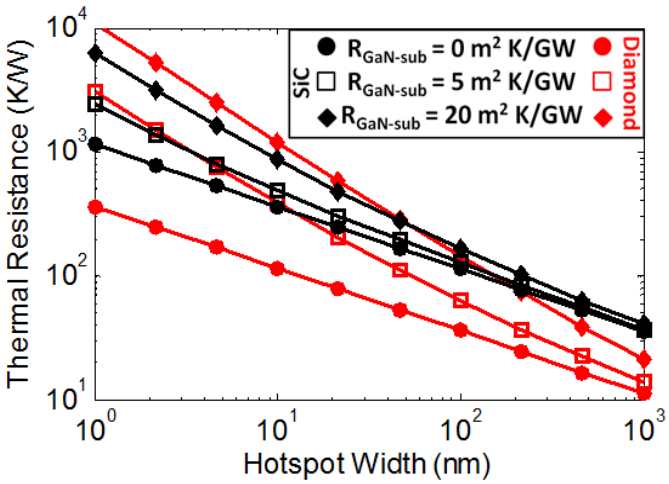

Fig. 3.2 Substrate and boundary thermal resistance experienced by HEMT gates of varying width with fixed aspect ratio. The simulated sample consists of 1000 nm GaN on diamond/SiC.

Although work exists in measuring R_{tran} for SiC substrates [14, 16, 17, 113], no such measurements have been performed for diamond. This section presents picosecond TDTR and nanosecond TTR measurements of a diamond on poly-AlN system. From these measurements, the intrinsic thermal conductivity of the diamond, the anisotropy of the diamond thermal conductivity, and the thermal interface resistance (TIR) experienced by diamond on poly-AlN are extracted. The presence of a low-quality layer AlN layer near the interface prevents us from referring to the diamond-AlN resistance as a TBR, since some degree of intrinsic conduction is involved. Comparing the diamond-AlN TIR to the transition layer resistance measured in GaN-SiC systems, this analysis shows $R_{tran-sub}$ and the intrinsic transition layer resistance may be the most significant contributor to R_{tran} for GaN on diamond.

3.2 Thermal Properties of Diamond on Poly-AlN

Extracting the thermal properties of a thin diamond film is not a trivial task. Since these films may have conductivities on the order of 2000 W m^{-1} K^{-1} [110, 114], it becomes difficult to separate their intrinsic thermal resistances from the boundary resistances [115]. In order to access the intrinsic resistance of the diamond film independently of the TBR, the measurement must be confined to the film region of interest. As the regime map in figure 1.2 demonstrates, there are several temporal

measurement regimes capable of accessing the thermal properties of a wide range of diamond film thicknesses. In order to obtain both total film resistance and individual TBRs, a combination of nanosecond- and picosecond- scale optical techniques were used.

3.2.1 Thermal Anisotropy Extraction

NTR and picosecond TDTR operate on significantly different time scales, but utilize the same physical principle to measure the temperature decay of a heated metal transducer on a stack of thin film materials. Since the NTR pump beam is much larger than the thickness of the diamond film, thermal spreading is negligible, and conduction is effectively 1-D. However, since the picosecond TDTR pump beam is of the same order as the film thickness, a 2-D radially-symmetric model is used [49].

In simulating heat diffusion through multilayer stacks, it is important to consider whether the thermal conductivity anisotropy of the film significantly affects the measurement. When the thickness of the film is of the same order as the width of the heating source, such spreading effects are non-negligible. Further, the thickness-dependent columnar grain structure of diamond films impedes the mean free path (MFP) of phonons in the lateral direction, reducing the lateral thermal conductivity [110, 115]. Since the $1/e^2$ pump beam waist in our experiment is 10 μm, only 7x the thickness of the film, thermal spreading effects are non-negligible. To counteract this, microscope objectives of varying magnification are used to control the width of the pump and probe beams (fig. 3.3). This allows tuning of the sensitivity of the measurement to lateral thermal conduction. The wider pump beam data gives the cross-plane thermal conductivity of the sample. This result is used with the thinner pump beam data to determine the lateral thermal conductivity of the sample. Combining both of these results with NTR measurements of total film resistance uniquely extracts the cross-plane and lateral diamond thermal conductivity, the Al-diamond TBR, and the diamond-AlN TIR.

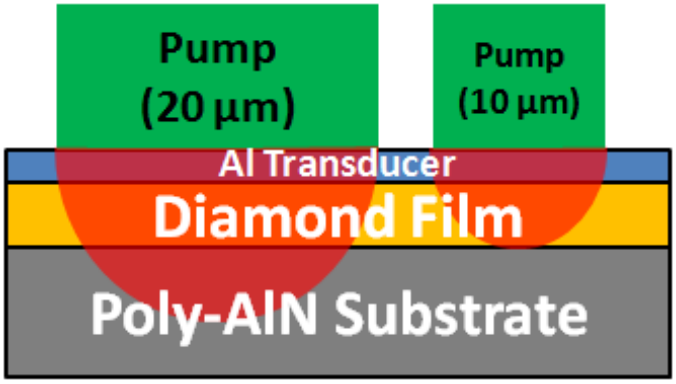

Fig. 3.3 Wider heat sources are less sensitive to thermal spreading resistance in the diamond film. As such, varying pump beam widths can control the measurement sensitivity to lateral thermal properties.

3.2.2 Sample Preparation

The sample design goal for this experiment was to mimic the diamond-AlN interface in a HEMT device while placing that interface within the thermal penetration depth of the measurement technique. Further, in order to access the thermal properties of the diamond film, direct contact between the transducer and diamond layers was required. The samples therefore consisted of a poly-AlN substrate which had been chemically-mechanically polished (CMP) to create a smooth growth surface. This resulted in a ~ 100 nm damaged AlN region at the interface. Subsequently, 1.4 µm and 1.7 µm of diamond were CVD-grown on the AlN substrate (fig. 3.4). The picosecond TDTR sample (1.4 µm diamond) received a 50 nm Al transducer, while the NTR sample (1.7 µm diamond) received a significantly thicker transducer.

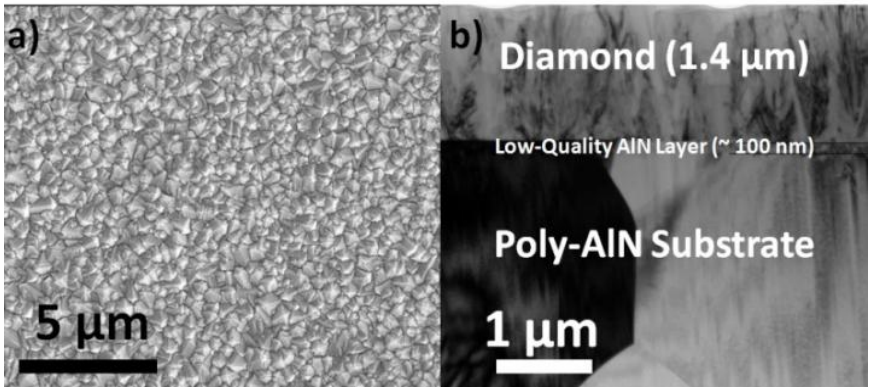

Fig. 3.4 a) Top-down view of the diamond film. Average grain width is ~ 0.5 µm. b) Cross-sectional view of the diamond on poly-AlN sample.

3.2.3 Results

The NTR measurements help extract the total effective cross-plane thermal conductivity (k_{eff}) of the diamond film. This value, 57.4 W m^{-1} K^{-1}, includes both the intrinsic resistance of the diamond and the diamond-AlN TIR. Since the timescale of the measurement is much longer than the characteristic decay length of the diamond film, this technique is incapable of separating the intrinsic and boundary resistance components. Instead, this result determines a range of possible values for intrinsic diamond thermal conductivity (k_{diam}) and diamond-AlN TIR ($R_{AlN\text{-}diam}$). Using $R_{eff} = d_{diam}/k_{eff}$ as the total thermal resistance of the film, k_{diam} and $R_{AlN\text{-}diam}$ are related by:

$$k_{diam} = \frac{d_{diam}}{R_{eff} - R_{AlN-diam}} \tag{3.7}$$

Figure 3.5 plots the value of $R_{AlN\text{-}diam}$ as a function of k_{diam}.

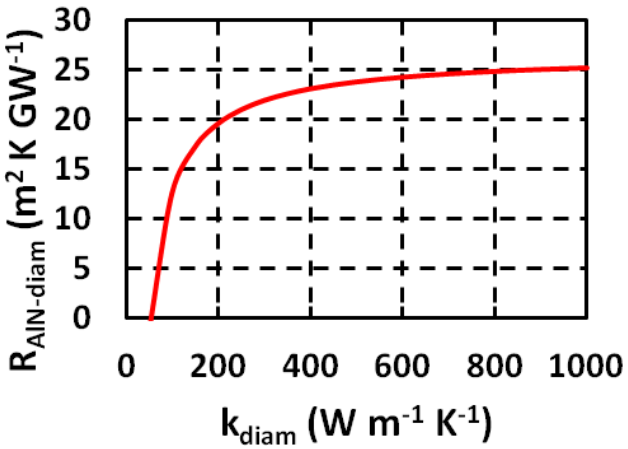

Fig. 3.5 Nanosecond thermoreflectance reveals the total cross-plane thermal resistance of the diamond film to be 26.6 m^2 K GW^{-1}. This plot demonstrates the range of possible diamond thermal conductivities and AlN-diamond TIRs (obtained using equation (3.7)) given this data.

Although the NTR data does not allow separation of these two resistances, the results form a constraint for the picosecond TDTR results. In this case, the fitting algorithm numerically solves for k_{diam} and $R_{AlN\text{-}diam}$, using equation (3.7) to link the two values. This model, in combination with the varying beam waist data, yields k_{diam} = 300 ± 40 W m^{-1} K^{-1} in the cross-plane direction, with an anisotropy of k_x/k_z = 0.75 ± 0.05. Further, the results show $R_{Al\text{-}diam}$ = 10.4 ± 0.5 m^2 K GW^{-1} and $R_{AlN\text{-}diam}$ = 19.7 ± 1.0 m^2 K

GW^{-1} (fig. 3.6). The uncertainty bars in these results are due to the existence of multiple possible combinations of k_{diam} and $R_{AlN\text{-}diam}$ which fit the picosecond TDTR data and satisfy the constraint of equation (3.7). Past measurements on the thermal properties of diamond films on silicon showed similar results for diamond-substrate TBRs [115] and intrinsic diamond thermal conductivity [110].

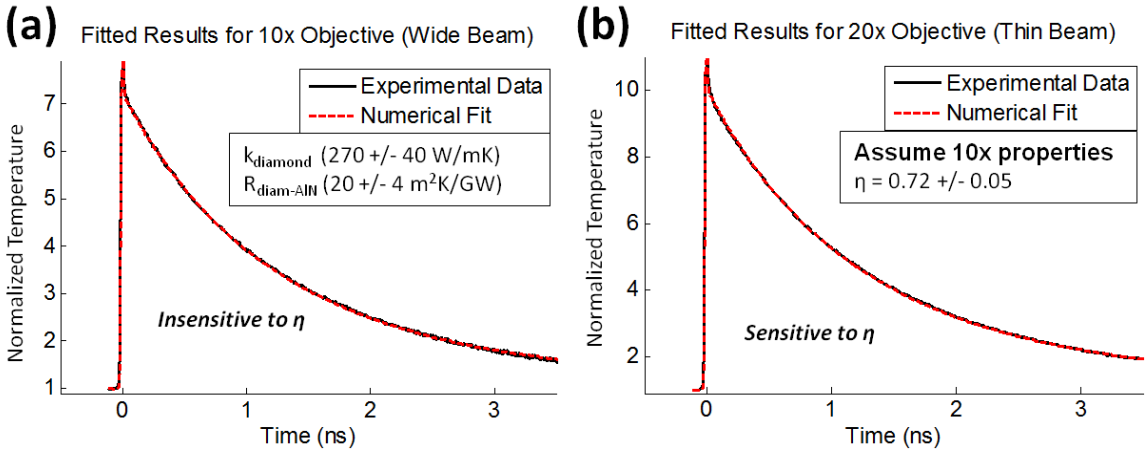

Fig. 3.6 Thermal decay traces for the diamond on AlN samples using (a) a 10x objective and (b) a 20x objective. The fitted results are shown in the boxes below the legends. From these results, the diamond thermal conductivity anisotropy is ~ 0.75 ± 0.05.

Since the diamond layer is significantly thicker than the low-quality AlN layer, and the separation between the transducer and AlN layers is quite large, the heat capacitance of the diamond overwhelms that of the AlN layer. While the high diamond thermal conductivity prevents this from significantly impeding the measurement's sensitivity to the properties of the AlN film, it does make it difficult to separate the diamond-AlN TBR from the intrinsic resistance of the low-quality AlN film. However, by comparing these results to similar work for GaN on SiC, one can evaluate the performance of a GaN-diamond interface [14, 16, 113].

Manoi et al. report the thermal interface resistance trend between GaN and SiC, with room temperature results ranging from 5 to 30 m^2 K GW^{-1}. Specifically, for an AlN nucleation layer of 70 nm thickness between GaN and SiC, room temperature TIR ranges from 20 to 25 m^2 K GW^{-1} [113]. They further demonstrate that this resistance scales with nucleation layer defect density. The diamond-AlN TIR measured here is similar to the

results of [113]. Although our structure lacks the GaN-transition layer TBR, this value is likely significantly smaller than what is reported here.

This diamond-AlN TIR contributes significantly to the total transition layer resistance. There are three potential causes for this large resistance: grain boundary scattering, defect scattering, and acoustic impedance mismatch. First, the grain size in CVD diamond depends strongly on the thickness of the film [115]. Near the diamond growth surface is a layer of very small diamond grains, upon which the larger columnar grains grow. The presence of the CMP-damaged layer further impedes the growth of larger grains. These small grains significantly reduce the phonon mean free path, resulting in a thin region of low thermal conductivity near the interface. Since the region is thin compared to the total thickness of the diamond film, the increased scattering resistance appears as a TBR. Second, the high defect density of the CMP-damaged region significantly reduces the mean free path of phonons in transition layer. Finally, the phonon transmissivity at an interface depends on the relative acoustic properties of the two films [83]. Since the CMP step significantly damaged the AlN near the diamond-AlN interface, the resulting 100 nm layer is likely far more compliant than the original poly-AlN substrate. As a result, the sound velocity mismatch between the transition layer and diamond will be high. This significantly lowers phonon transmissivity at the interface and increases TBR.

In order to improve the performance of the diamond substrate, the above contributions to TIR must be addressed. All three scattering sources can be reduced through the use of single-crystal AlN nucleation layers. Grain boundary scattering, defect scattering, and reduced phonon transmissivity all stem from the presence of the damaged AlN layer. A high-quality, single-crystal AlN film would provide a better growth surface for the diamond film, improve the phonon mean free path within the transition layer, and enhance phonon transmissivity at the diamond-AlN interface.

The performance of diamond in HEMT applications depends on both the intrinsic and interface thermal resistances of the substrate. Several phenomena govern the interface resistance, including grain boundary scattering, defect scattering, and acoustic impedance mismatch. If these three components contribute to a transition layer resistance

in excess of 5 m^2 K GW^{-1}, diamond loses the advantage over traditional SiC substrates. Time-domain and transient thermoreflectance techniques quantified the diamond-AlN TIR at 19.7 m^2 K GW^{-1}. Although this value exceeds the limit for which diamond is more effective than SiC, higher quality growth surfaces should significantly reduce the diamond-AlN TIR, potentially making such substrates optimal choices for HEMT thermal management.

3.3 Thermal Conduction Nonhomogeneity of Suspended Diamond Films

Diamond has long been a material of interest in the spreading of heat from high power electronic devices. Since the 1980's chemical vapor deposition of diamond has become well established [116-121] and has led to routine deposition of polycrystalline and nanocrystalline diamond thin films. An unmet challenge is to integrate diamond materials into high power device structures in order to take advantage the diamond's high thermal conductivity. Unique to diamond thin film deposition is the need for a seed layer to nucleate film growth on a foreign substrate. In this work, the seeds are nanodiamonds (typically 5-10 nm diamond particles) spread at roughly 10^{12} seeds/cm^2 on the silicon substrate before growth. During the initial stage of deposition, the seed layer coalesces into a continuous film. The deposited film is fully coalesced at 300nm thickness. Beyond the initial coalescence layer, there is predominantly columnar growth normal to the silicon-diamond interface [121].

Diamond is viewed as a promising potential successor to Si and SiC as a thermal spreader for high electron mobility transistors (HEMT) based on GaN [122-126]. Theoretically, single-crystal diamond offers thermal conductivity up to 3300 W m^{-1} K^{-1} at room temperature [114, 127, 128]. Even when polycrystalline diamond film thickness is less than several hundred micrometers, cross-plane thermal conductivity remains on the order of 1000 W m^{-1} K^{-1} at room temperature [110, 129]. However, several factors can impede the mean free path of phonons in diamond, reducing the intrinsic thermal conductivity. These include impurity scattering, grain boundary scattering, and interface scattering [110, 115, 129, 130]. At the initial stage of diamond thin film deposition, these scattering sites are abundant, significantly reducing thermal conductivity (fig. 3.7) [130].

If the thermal resistance due to the film coalescence layer is sufficiently large, diamond thin films with a coalescence layer between the bulk diamond film and the thermal load may not hold a thermal advantage over Si or SiC [131, 132].

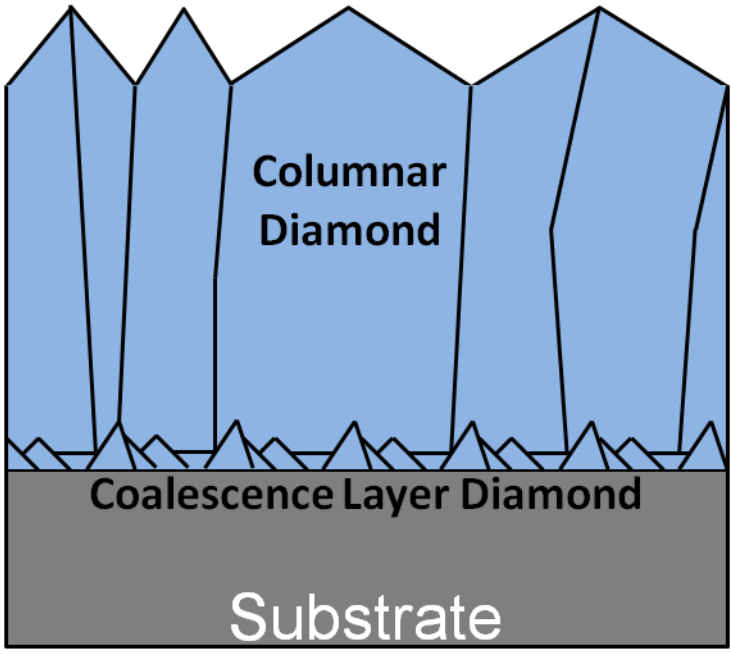

Fig. 3.7 Grain structure sketch for diamond grown on a substrate. The nucleate grains in the coalescence layer are significantly smaller than the large, columnar grains which grow on top. This increases the scattering site density near the interface, lowering thermal conductivity.

This work presents picosecond time-domain thermoreflectance (TDTR) measurements on suspended nanocrystalline diamond films from 0.5 μm to 5.6 μm in thickness. By probing both sides of the suspended film, we capture the cross-plane thermal conductivity of both the coalescence region (k_C) and the high-quality columnar grain (k_{HQ}) regions. Using these results with a two-layer heat diffusion model of the diamond film, we estimate the thickness of the low conductivity coalescence layer and compare the thermal resistances of the coalescence versus high-quality regions. This analysis demonstrates that the coalescence region can be a substantial contributor to thermal resistance in a diamond thin film.

3.3.1 Dual-Sided Thermoreflectance Technique

Since diamond is highly thermally conductive, the temporal resolution of picosecond TDTR is insufficient to separate the diamond film coalescence layer thermal resistance from the diamond-silicon TBR [132]. In order to do so, we require direct optical access to the diamond coalescence layer. This involves removal of the silicon substrate to allow deposition of a metal transducer directly on the seeded surface of the coalescence region. To accomplish this, we deposited three nanocrystalline diamond films on silicon substrates of thicknesses 0.5 μm, 1.0 μm, and 5.6 μm. The silicon substrates were selectively etched to produce a suspended diamond thin film roughly 5 mm in diameter. A 50 nm Al transducer layer was deposited on each side of the suspended diamond film (fig. 3.8).

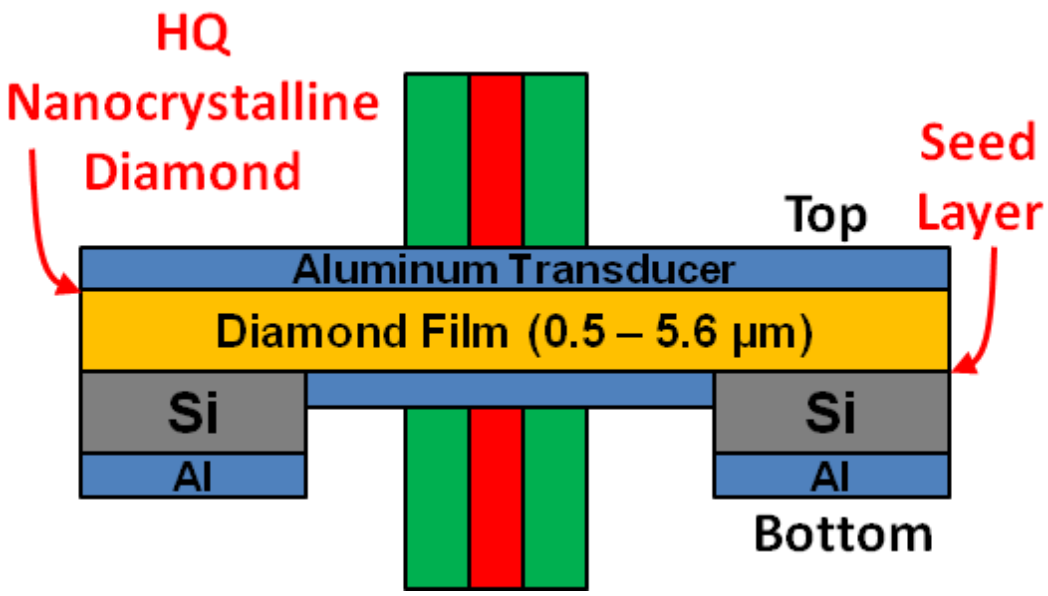

Fig. 3.8 Cross-sectional diagram of the suspended diamond film sample showing the Al transducer interface with the seeding/coalescence layer and with the high-quality (HQ) nanocrystalline diamond surface. Note that silicon has been etched to give access to the seeded surface of the diamond film where film coalescence occurs. The Al transducer layer is 50 nm thick, and the etched hole in silicon is ~ 5 mm in diameter. The red and green areas (color image available online) indicate the probe and pump beams, respectively.

When extracting TDTR data, one has both an in-phase and out-of-phase thermoreflectance response. These data are combined to create signal and phase components. The general rule for these data is that the signal component is more sensitive

to the thermal conductivity of the film of interest than to its heat capacity, while the opposite is true for the phase component. The exception to this rule occurs when: 1) the characteristic thermal decay time of the film of interest is less than the measurement time scale, and 2) the film is effectively insulated during the measurement time scale. If both of these are satisfied, the measurement behaves similarly to a calorimeter, where the temperature decay of the transducer film depends primarily on the heat capacity of the film of interest.

3.3.2 Results

The 0.5 μm thick diamond film is an excellent demonstration of this scenario. Usually, picosecond TDTR is capable of uniquely separating the transducer-film TBR from the film thermal conductivity. However, in this case, our model is not able to find a unique solution for the thermal decay. Rather, we obtain an effective thermal resistance for the diamond film of 20 ± 2.0 m^2 K GW^{-1}, which can be expressed as:

$$R_{eff} = R_{Al-diam} + \frac{d_{diam}}{k_C} \tag{3.8}$$

where R_{eff} is the effective resistance of the diamond film, $R_{Al\text{-}diam}$ is the aluminum-diamond TBR, and d_{diam} is the thickness of the diamond film. We convert this to an effective thermal conductivity of the diamond layer by dividing the film thickness by the resistance. This gives a $k_{eff,C}$ of ~ 25 W m^{-1} K^{-1}. Since the previously reported diamond heat capacity [133] is ~ 2.15×10^6 J m^{-3} K^{-1}, this translates to a total thermal diffusivity of ~ 1.16×10^{-5} m^2 s^{-1}. The characteristic thermal decay time of the diamond, determined via:

$$\tau_{diam} = \frac{d_{diam}^2}{\alpha_{eff}} \tag{3.9}$$

where α_{eff} is the effective thermal diffusivity, is ~ 22 ns. The characteristic timescale of the heating event, however, is given by the inverse of the 5 MHz pump modulation frequency. This translates to a heating timescale of 200 ns, significantly greater than τ_{diam}. Therefore, although measurements on this sample are insensitive to the difference between intrinsic and thermal boundary resistance, we can uniquely extract the diamond heat capacity. The fitted heat capacity, 1.98×10^6 J m^{-3} K^{-1}, is similar to previous literature results [133].

In order to separate out k_C and $R_{Al\text{-}diam}$ from the effective thermal resistance, we use the 1.0 μm thick diamond film. While τ_{diam} for this film (~56 ns) is still less than the timescale of the measurement, we have sufficient sensitivity to separate the transducer-film TBR from the intrinsic film thermal conductivity. Modeling the system as 50 nm Al on 1.0 μm diamond, we extract a TBR of 13.5 ± 1.0 m^2 K GW^{-1} between the Al transducer and the diamond coalescence layer. Further, we find a cross-plane thermal conductivity of 80 ± 10 W m^{-1} K^{-1} for the diamond coalescence layer. By plugging these results into equation (3.8), and setting d_{diam} to 0.5 μm, we obtain a total thermal resistance that agrees with the value measured from the 0.5 μm diamond sample. Comparing the results with Touzelbaev et al's model of local diamond thermal conductivity indicates an average coalescence layer grain size of 100-200 nm [130].

We determine the thickness of the coalescence layer using the 5.6 μm diamond film. Picosecond TDTR measurements on the top side of the diamond reveal an Al-diamond TBR of 10.7 ± 1.0 m^2 K GW^{-1}, smaller than for the Al-coalescence layer interface. Since TBR is highly dependent on surface cleanliness, this difference may be due to impurities left behind by the etching process on the bottom diamond film surface. Assuming the heat capacity measured from the 0.5 μm sample, and using a one-layer model of 50 nm Al on 5.6 μm diamond, we find a cross-plane thermal conductivity of 1350 ± 200 W m^{-1} K^{-1} for the high-quality diamond (fig. 3.9). It is worth noting that the result of the numerical fit for this sample remains the same even assuming a diamond thickness as low as 2.5 μm. This implies the top side measurement may be insensitive to the coalescence layer properties.

To confirm this assertion, we performed TDTR on the bottom of the same sample. Figure 3.10 demonstrates the difference in the thermoreflectance curves for the two measurements, showing a significantly slower thermal decay through the coalescence-layer. Using the coalescence layer diamond data from the 5.6μm thick film, we created a two-layer model of heat conduction through the suspended film. This model assumes 50 nm of Al on a diamond coalescence layer with unknown thickness, d_C, on a high-quality diamond layer of thickness d_{HQ} = 5.6 μm-d_C. Assuming k_C = 80 W m^{-1} K^{-1} and k_{HQ} = 1350 W m^{-1} K^{-1}, we fit for the coalescence layer thickness and find d_C = 0.76 ± 0.1 μm.

The thickness of the high quality diamond layer, therefore, is ~4.84 μm, thick enough to render the top side measurements insensitive to the thermal properties of the coalescence layer diamond. This validates the one-layer assumption used for the top side measurement of the 5.6 μm sample.

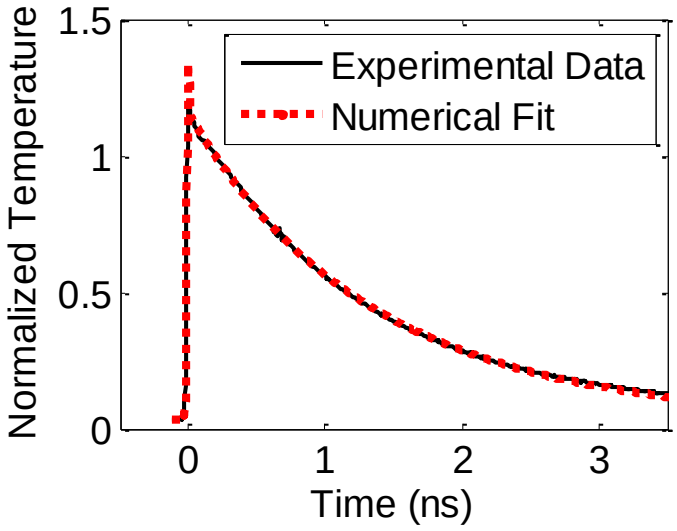

Fig. 3.9 Picosecond TDTR data (solid line) and numerical fit (dotted line) for the top side measurement of the 5.6 μm diamond film. The fit corresponds to an Al-diamond TBR of 10.7 ± 1.0 m^2 K GW^{-1} and a diamond thermal conductivity of 1350 ± 200 W m^{-1} K^{-1}.

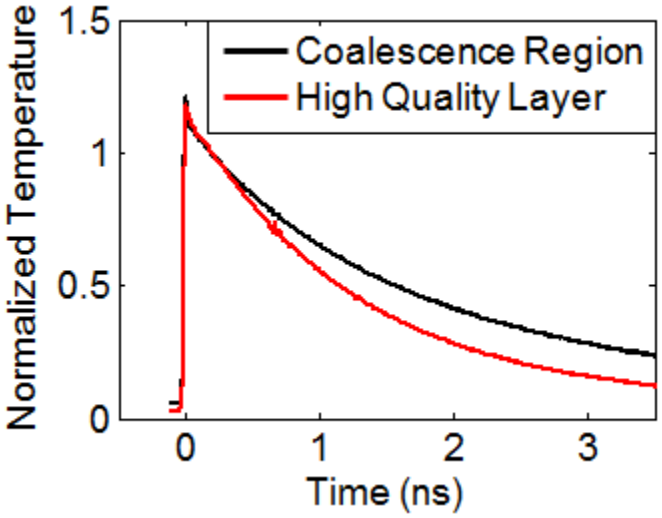

Fig. 3.10 Comparison of picosecond TDTR curves from the coalescence and high quality layers of the 5.6 μm diamond sample. The larger, higher quality diamond grains on the top surface result in a higher thermal conductivity than for the bottom. This is evidenced by the faster thermal decay shown for the high quality layer.

The thermal properties of the diamond film coalescence layer have a drastic effect on the total thermal resistance of the film. Using the results obtained in this paper, we find, for a 5.6 μm diamond film, that the coalescence layer thermal resistance ($R_C = d_C/k_C$) is ~ 9.5 ± 1.4 m^2 K GW^{-1}. This is significantly larger than the thermal resistance of the rest of the diamond film (~ 3.6 ± 0.6 m^2 K GW^{-1}). In fact, the 0.76 μm coalescence layer has a thermal resistance equivalent to ~ 12.8 μm of high quality diamond.

This work demonstrates thermal conductivity inhomogeneity in nanocrystalline diamond films. The properties of the coalescence layer were measured using a dual-sided picosecond TDTR measurement. This technique extracted the thermal conductivity of the coalescence layer, the high quality diamond layer, and the heat capacity of the suspended films. From these results, we estimate the coalescence layer thickness and calculate the thermal resistance contributions of both regions of the diamond film. The additional coalescence layer thermal resistance is significant. Further research into nanocrystalline diamond nucleation and growth may improve the coalescence layer thermal properties, reducing the total thermal resistance and enhancing the thermal performance of integrated nanocrystalline diamond thermal spreaders for HEMT applications.

Chapter 4

Multilayer Extreme Ultraviolet Mirrors

Extreme ultraviolet lithography (EUVL) is a promising technique for scaling microelectronic devices beyond the 22 nm node [134, 135]. The wavelength of the optical radiation used (~13.5 nm) significantly improves the diffraction-limited resolution with respect to lithographic techniques in the Deep-UV range. Few materials or material combinations are capable of reflecting such EUV wavelengths, and optics lifetime is challenging. Mirrors must withstand photon energies on the order of 90 eV, which is substantially larger than the ionization energies of many of the materials used for optical components (e.g. 34 eV/particle for the third Si ionization energy). Periodic multilayers offer a way to circumvent these issues. Unlike single-material mirrors, these structures consist of multiple bilayers of materials with varying indices of refraction [136]. By carefully controlling the material properties and thicknesses, one can use constructive interference to create highly reflective surfaces at a given wavelength [137, 138]. In the case of EUV wavelengths, such stacks consist of ~ 6.9 nm bilayers composed of alternating layers of molybdenum and amorphous silicon.

While much previous research has been published on the optical performance of Mo/Si-coated masks and mirrors [134-137, 139], there is currently no rigorous information about their thermal properties and temperature fields resulting from radiation absorption. Considering that many experiments demonstrated that damage can occur in these materials due to long-term/high-temperature radiation exposure [140-142], a detailed understanding of their thermal properties is appropriate at this time. However, nanoscale thermal transport effects in the Mo/Si multilayer stack complicate this task.

Interface scattering within the mirror structure significantly reduces the mean free path (MFP) of the thermal energy carriers. This reduces the film thermal conductivity below what we expect for bulk Mo and a-Si. Further, interface scattering affects cross-plane MFP considerably more than in-plane, which can result in very significant thermal conductivity anisotropy. Lastly, although thermal conduction in bulk Mo is electron-dominated, the low thickness of the Mo film and the presence of the dielectric a-Si layers restricts the electron mean free path, changing the relative contributions of electrons and phonons to heat conduction, particularly in the through-plane direction [143]. These factors impede thermal conduction through the Mo/Si stacks, resulting in higher operating temperatures. This can increase the risk of degradation in mirror reflectivity.

During fabrication of the Mo/Si multilayer, a thin layer of a-$MoSi_2$ forms at each interface [140]. Over the lifetime of the material, constant exposure to elevated temperatures will cause this layer to crystallize [141], after which Mo and Si will interdiffuse further [140-142]. Mirror temperature governs the rate of diffusion, given by [136, 141]:

$$D = D_0 \exp\left(-\frac{E_\alpha}{k_B T}\right) \tag{4.1}$$

where D_0 is the temperature-independent interdiffusion coefficient, E_α is the interdiffusion activation energy, and k_B is Boltzmann's constant. The thickness of the interdiffused region increases with time, given by [141]:

$$w^2(t) = 2Dt + w^2(0) \tag{4.2}$$

where w is the thickness of the interdiffused region and t is time. During this process, the higher-density c-$MoSi_2$ film consumes the lower-density a-Si layer. This process, known as compaction, shrinks the stack periodicity and causes the centroid of the reflectance spectra to shift towards lower wavelengths. This results in a rapid drop in reflectance at 13.5 nm (fig. 4.1). Since EUV source lifetimes are in excess of 10^9 pulses [144], and since a reflectance drop of 1% marks the end of mirror lifetime [136], the allowed operating temperature of the mirror must be limited. The thermal properties of the mirror,

in turn, limit the fluence that can be tolerated while keeping temperatures below this threshold.

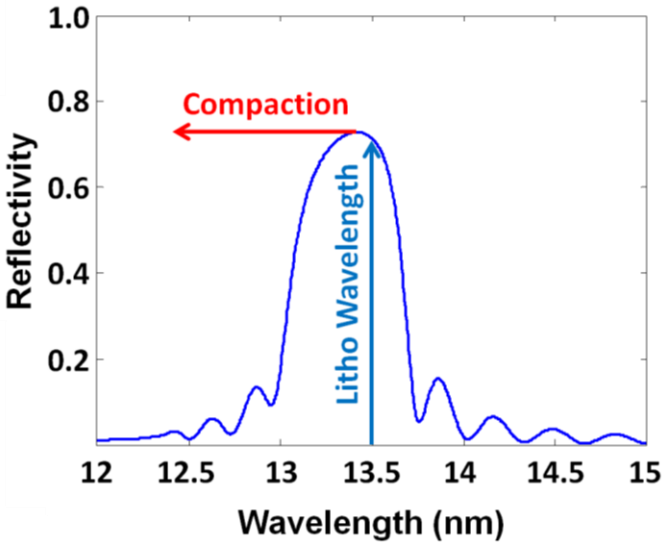

Fig. 4.1 Reflectance spectra of a multilayer mirror consisting of 40 periods of $Mo_{0.4}/Si_{0.6}$. The spectra was calculated using the algorithm reported by D.L. Windt [145]. As compaction proceeds, the centroid shifts towards lower wavelengths (indicated by the red arrow), and the reflectivity at the 13.5 nm lithography wavelength drops.

This work measures the thermal properties of thin film mirror materials for use in simulations and reliability predictions for EUV mirrors. In addition to measuring the thermal properties of the multilayer Mo/Si stack, we also report the thermal conductivities and boundary resistances offered by the capping and absorber layers on the mirror surface. To accomplish this, we apply both picosecond time-domain thermoreflectance (TDTR) and frequency-domain electrical thermometry (the 3ω method) with bridges of varying width down to 50 nm on a variety of thin film samples, including: 1) the TaN absorber, 2) the interdiffused $MoSi_2$ region, and 3) the multilayer Mo/Si stack. The final section of this chapter assesses the impact of the measured properties on the total thermal resistance and temperature rise experienced at an EUV spot on a mirror structure.

4.1 High Temperature Thermal Properties of TaN

Tantalum Nitride is common as a diffusion barrier film in magnetoresistive random access memory [146-148]. Such diffusion barrier films are essential for

preventing intermixing between thin functional films. Recently, TaN has become the preferred absorber material for EUV masks. This absorber layer rests on a Ruthenium-capped Mo-Si material that forms the resonant reflector for EUV light. Both magnetoresistance random access memory and EUV mask applications involve high heat flux densities within the TaN layer and surrounding materials. Accurate thermal property data are therefore needed for thermal simulation of devices using this material to ensure they do not succumb to heat-related damage. Although the electrical properties of TaN are well cataloged [146], there are few data in the literature on its thermal properties, and essentially no data for the thermal conductivity of thin films.

This section presents cross-plane electrical conductivity and picosecond time-domain thermoreflectance (TDTR) measurements on TaN films from 50 to 100 nm in thickness. The in-plane electrical conductivity data estimates the electron contribution to TaN thermal conductivity. Combining this result with the minimum phonon thermal conductivity of TaN offers an estimate of total in-plane thermal conductivity. The TDTR data includes the thermal boundary resistance (TBR) between Al and TaN ($R_{Al\text{-}TaN}$), and the out-of-plane intrinsic thermal conductivity (k_{TaN}). We compare the measured k_{TaN} with the in-plane k_{TaN} estimate obtained from electrical measurements and minimum phonon thermal conductivity theory.

High-temperature TDTR measurements extract the TaN intrinsic thermal conductivity, as well as the Al-TaN TBRs. During these measurements, the samples remain housed in an optical access oven pumped to vacuum. Temperature ramps are in 100 K increments, with a 15 minute hold at each level before measurement.

4.1.1 Electron Size Effect and Minimum Phonon Conductivity

Three samples of varying TaN thickness were prepared: 50 nm, 75 nm, and 100 nm. Half of each sample was coated with 50 nm Al for optical measurements, while the remaining half was left uncovered for electrical sheet resistance measurements. Although TEM images and nanobeam diffraction data show the morphology of the films to be the same (fig. 4.2), electrical measurements demonstrated thickness-dependent electrical resistivity [149]. In determining k_{TaN} using the principle of thickness dependent thermal

resistance with samples of varying thickness, one usually assumes the intrinsic film thermal conductivity does not vary between samples. This analysis neglects any potential reductions in thermal conductivity due to size effects in the film. These effects can include increased scattering rates on film boundaries or on regions of higher imperfection density. Since the mean free path (MFP) of electrons in TaN can be ~ 25 nm, such scattering effects may complicate calculation of the cross-plane thermal conductivity of our films [146]. Primarily, the intrinsic thermal conductivity of the 50 nm film may be lower than that of the 100 nm film due to such effects. As a result, the thickness-independent solution may lead to inaccuracies in the out-of-plane k_{TaN}. It is therefore critical to determine how size effects modify the thermal behavior of these films.

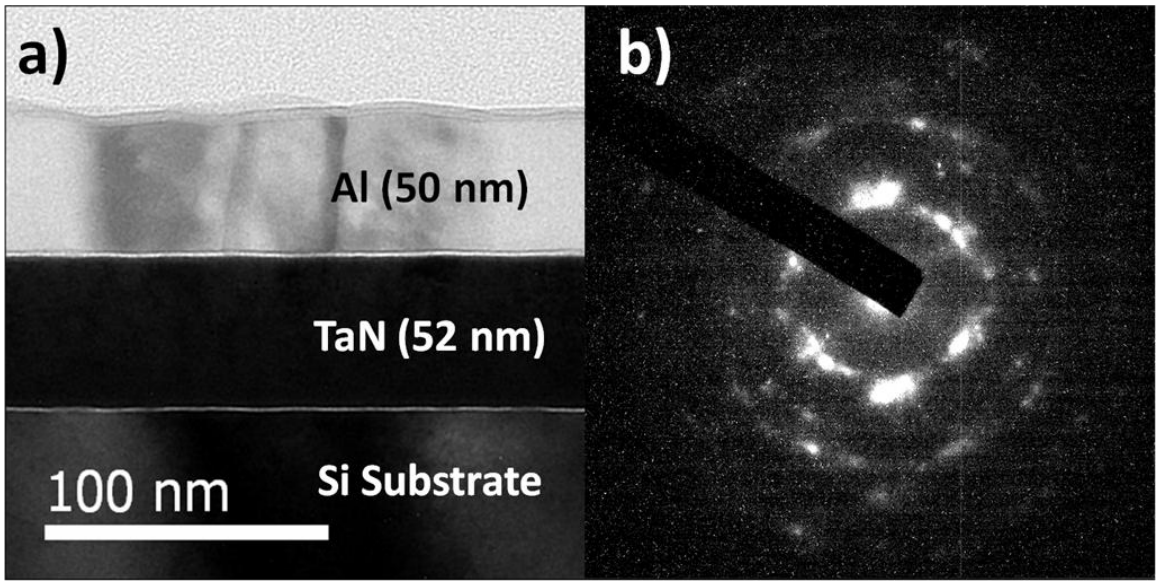

Fig. 4.2 (a) Cross-sectional TEM of Al on TaN on Si. The targeted TaN thickness is 50 nm. (b) Nanobeam diffraction shows the structure to be a mix of polycrystalline and amorphous TaN. The diffraction patterns are similar for all three thicknesses of TaN, implying that average grain size is not thickness dependent at this scale.

In order to account for size effects in electron thermal conduction, sheet resistance measurements of the 50 to 100 nm films were performed. These measurements demonstrate thickness-dependence in the lateral electrical conductivity (σ_{lat}) of the film (fig. 4.3). Line of Sight analysis extracts, absent of boundary scattering effects and assuming similar morphology for all samples, the average electron MFP. For a medium with completely diffuse interfaces, this relation becomes [150]:

$$\frac{\sigma_{lat}}{\sigma_{bulk}} = 1 - \frac{3}{2\delta}\int_1^{\infty}\left(\frac{1}{\xi^3} - \frac{1}{\xi^5}\right)(1 - \exp(-\delta\xi))d\xi \tag{4.3}$$

where σ_{bulk} is bulk TaN electrical conductivity assuming the same morphology as the thin films, and δ is the ratio of film thickness, d, to bulk electron MFP, λ_e. Fitting equation (4.3) to the measured thickness dependent in-plane electrical conductivity for δ yields a bulk electron MFP of 30 nm (fig. 4.3). Using a simple Matthiesen's rule approach ($\frac{1}{\lambda} = \frac{1}{\lambda_e} + \frac{1}{d}$), this result indicates that the cross-plane electron thermal conductivity of the 50 nm film (given by $k_e = \frac{1}{3}C_e v_f \lambda$, where C_e is the volumetric electron heat capacity and v_f is the Fermi velocity) may be 20% less than that of the 100 nm film. Since the measurement temperatures are greater than half the Debye temperature of TaN [151], the WFL law provides a reasonable estimate of the electron thermal conductivity. This value ranges from 2.8 to 3.1 W m^{-1} K^{-1} for the 50 to 100 nm samples.

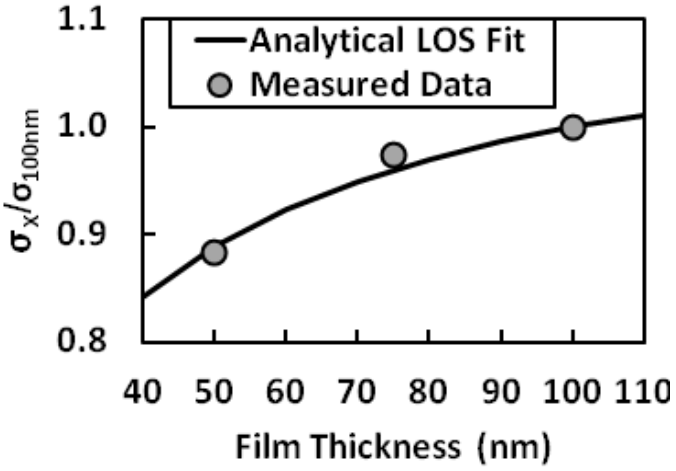

Fig. 4.3 Plot of electrical conductivity ratios between the 50, 75, and 100 nm TaN thin films. These ratios, in combination with equation (4.3), predict electron MFP. The above plot shows the best fit result (λ_e = 30 nm).

Since the TaN microstructure consists of a mixture of both crystalline and amorphous phases [152], minimum thermal conductivity theory offers a practical estimate of phonon thermal conductivity ($k_{p,min}$) [153]. In this analysis, the carrier MFP is equal to interatomic spacing in TaN. The relation:

$$k_{p,min} = \frac{1}{3}C_p v_p \lambda_p \tag{4.4}$$

where C_p is the volumetric heat capacity [154], v_p is the average phonon velocity [154], and λ_p is the average phonon MFP calculated from TaN density [154], gives the minimum phonon thermal conductivity. This gives $k_{p,min}$ ~ 1.4 W m^{-1} K^{-1} at 300 K. By summing the contributions from both electrons and phonons, and assuming isotropic conduction, the intrinsic thermal cross-plane conductivity of TaN at room temperature becomes ~ 4.0 – 4.3 W m^{-1} K^{-1} for the 50 to 100 nm films.

4.1.2 Experimental Method

In order to extract k_{TaN} from our TDTR measurements, we solve the radially-symmetric heat diffusion equation for conduction through the material stack and fit the solution to the experimental thermal response data [48, 49]. Since the measurement for each individual film is only sensitive to the lumped thermal resistance of the TaN layer and $R_{TaN\text{-}Si}$, one can separate the TaN volumetric resistance from $R_{TaN\text{-}Si}$ by simultaneously fitting the thermal properties of all three samples to extract an accurate measure of the out-of-plane k_{TaN}. Since the pump and probe beams in this technique are roughly 100 times wider than the thickness of the TaN films, the measurement is insensitive to the in-plane k_{TaN}. Although it is valid to assume that the TBRs are constant for all three samples at each temperature, the same assumption is not true for k_{TaN}. One can account for the size effect by modeling k_{TaN} as a combination of minimum phonon conductivity and thickness-dependent electron thermal conductivity:

$$k_{TaN}(d) = k_{p,min} + \frac{1}{3} C_e v_f \left(\frac{1}{\lambda_e} + \frac{1}{d} \right) \tag{4.5}$$

where C_e is the electron volumetric heat capacity, v_f is the Fermi velocity, and λ_e is the electron MFP. Fitting for the product of C_e and v_f returns a thickness-dependent result for k_{TaN}.

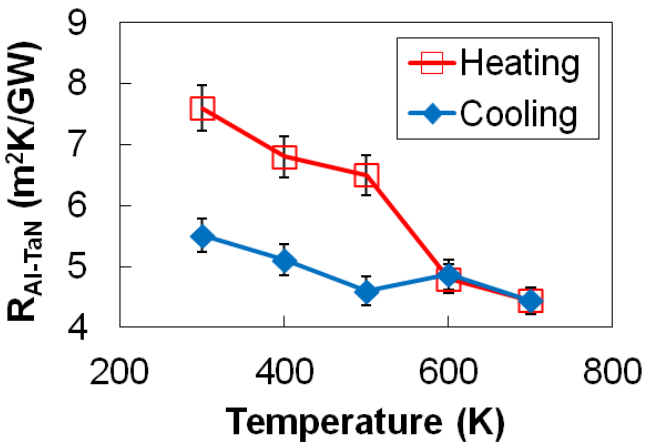

Fig. 4.4 Temperature-dependent Al-TaN TBR. The open squares represent the heating curve, and the closed diamonds represent the cooling curve. Note that $R_{Al\text{-}TaN}$ drops after heating above 600 K, demonstrating improvement in interface quality.

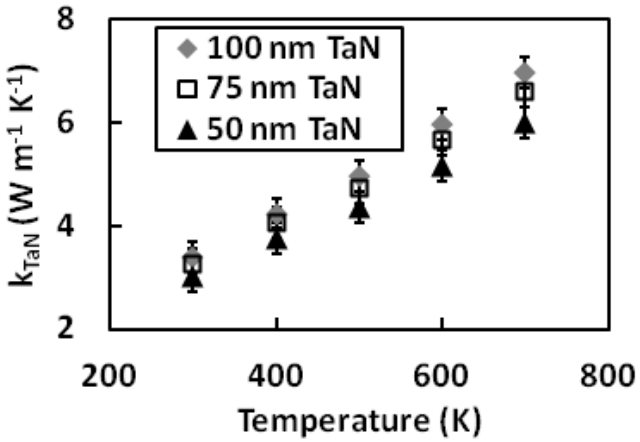

Fig. 4.5 Temperature-dependent intrinsic out-of-plane thermal conductivity of TaN for the 50 to 100 nm samples.

4.1.3 Results

Figures 4.4 and 4.5 report the results for $R_{Al\text{-}TaN}$ and k_{TaN}. Although the Al-TaN TBR decreases significantly after being heated, the heating and cooling curves for the TaN intrinsic thermal conductivity show no significant difference. This smooth temperature dependence of the thermal conductivity suggests that TaN is structurally stable up to 700 K. As Ono et al. demonstrated, a marked increase in the electrical resistance of a material accompanies increased species diffusion from the surrounding layers [155]. This change is due to increased impurity density in the material of interest, which reduces electron MFP. Because electrons are a major thermal energy conductor in

TaN, the structural failure of the film would similarly correspond to a substantial increase in thermal resistance. Given that the measurements show no significant drop in out-of-plane k_{TaN}, it can be assumed that the TaN layer is structurally stable up to 700 K. Further, it is doubtful that the hysteresis shown in figure 4.4 is due to species diffusion between Al and TaN, as this typically increases TBR due to the presence of a disordered material layer [88]. Rather, the results imply that interface annealing may reduce the dislocation density between the two films, lowering the interfacial carrier scattering rate.

At 300 K, the measured intrinsic thermal conductivity of TaN ranges from 3.0 to 3.4 W m^{-1} K^{-1} for the 50 to 100 nm samples, lower than predicted from the Wiedemann-Franz-Lorenz law and minimum thermal conductivity theory. This is likely due to the earlier assumptions of isotropic electron conduction. Lateral electron conduction is less susceptible to boundary scattering than cross-plane conduction. As a result, the theoretical prediction of cross-plane conductivity gives a larger result than observed. This disparity decreases for thicker TaN films. To account for this, a more rigorous theoretical treatment including both electron and phonon conduction is necessary. This suggests a Boltzmann Transport approach, which may be excessive in terms of constructing thermal models for systems containing TaN. For the purposes of creating such models, the data presented in this paper accurately represent the thermal behavior of these films.

4.2 Thermal Properties of the Mo/Si Multilayer and MoSi2 Intermetallic

The multilayer mirror/mask structure consists of four separate parts: substrate, multilayer, capping layer, and absorber (fig. 4.6 (a)). The structure is then coated with additional metal and dielectric layers as required by the specific measurement technique. The substrate acts as a mechanical support and provides a heat diffusion path from the multilayer to the heat sink. In a mirror application, low thermal expansion materials such as quartz serve as the substrate. However, silicon was used instead to improve heat diffusion from the multilayer during measurement.

The multilayer mirror stack sits directly on the substrate. The complete mirror structure consists of a 6.9 nm/bilayer stack (fig. 4.6 (b)). Each period contains 2.2 nm of

a-Si, 2.6 nm of Poly-Mo, and 2.0 nm of interdiffused a-$MoSi_2$. The thickness of the interdiffused layer varies depending on the temperature history of the multilayer and whether the surface was a-Si deposited on Poly-Mo (0.7 nm) or vice versa (1.3 nm). Several papers have noted the variation in interdiffusion layer thickness [140-142, 156]. Zubarev et al. argued that the crystalline nature of the Mo film make it difficult for silicon atoms to diffuse in during deposition [142]. However, as Mo is deposited, the covalent bonds in the a-Si layer are easily broken, resulting in a thicker a-$MoSi_2$ layer.

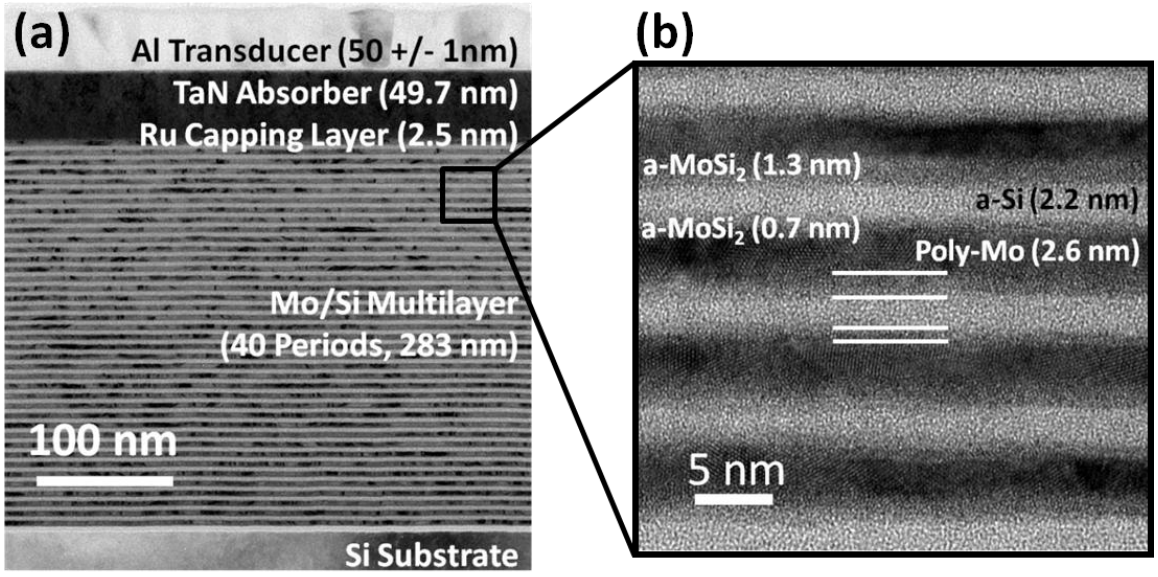

Fig. 4.6 Cross-sectional TEM of: (a) a Mo/Si-based mirror sample, consisting of substrate, multilayers, capping layer, absorber, and Al transducer layer, and (b) the Mo/Si bilayer mirror structure. The white lines in the center indicate (top-down) the Poly-Mo/a-$MoSi_2$, a-$MoSi_2$/a-Si, a-Si/a-$MoSi_2$, and a-$MoSi_2$/Poly-Mo interfaces.

Since the Mo/Si multilayer structure is not stable in air, an Ru capping layer coats the multilayer mirror material [157]. The purpose of this layer is to minimize oxidation in the mirror material without adversely affecting the stress profile or reflectivity in the multilayer [139, 158, 159]. Yan et al. demonstrated that a 2 nm Ru layer maximizes the reflectivity of the stack while offering protection against oxidation [159].The last film in the EUV mask stack is the absorber. This film must be capable of absorbing electromagnetic radiation in the range of extreme UV to soft X-rays. Further, it must not exert undue stress upon the rest of the mirror structure. Au, W, Ta, and TaN are common

absorber film selections [160, 161]. TaN offers low stress [161], an amorphous/poly-crystalline structure [146, 149, 161], and good absorption properties in EUV [161].

The complete mirror structure is more complex – and therefore poses greater challenges for minimizing the uncertainty - than many structures measured using both picosecond TDTR and the 3w method. In order to accurately model the thermal resistance experienced by an EUV pulse, one must account for the thermal resistances of the TaN absorber, the Ru capping layer, and the Mo/Si multilayer stack. This becomes even more complex when one accounts for the thermal boundary resistances between the Ru capping layer and the Mo/Si mirror, and the impact of the a-$MoSi_2$ interdiffused region. To address these tasks, several simpler structures were designed to mimic the individual films, interfaces, and interdiffused regions within the EUVL mask structure.

4.2.1 Sample Design

In order to understand the thermal behavior of the Mo/Si multilayer stack, one must extract three critical thermal properties: cross plane thermal conductivity, in-plane thermal conductivity, and the thermal resistance contribution of the capping layer. We therefore fabricated samples containing 40 periods of Mo/Si on silicon. Half of the samples were left uncapped for 3ω measurements of cross-plane and in-plane thermal conductivity. The remaining samples received 50 nm coatings of Al or Ru for optical thermoreflectance measurements. Both materials are excellent thermoreflectance transducers [33], and allow direct measurement of the Ru-Mo/Si and Al-Mo/Si TBRs. Two Mo/Si ratios were selected for measurement: 0.4/0.6 and 0.6/0.4. In both cases, the total thickness of each bilayer remained 6.9 nm.

The $MoSi_2$ samples were prepared by co-sputtering Mo and Si onto a Si wafer at 300 K. The targeted sample thicknesses were 100, 200, and 250 nm. The thicknesses were chosen to avoid size effect issues in measuring thermal conductivity. Since these films were co-sputtered at room temperature, the $MoSi_2$ layers were amorphous. Subsequently, a 50 nm Al transducer layer was deposited on half of the $MoSi_2$ wafer for thermoreflectance measurements. The other half was left uncoated for electrical conductivity measurements.

4.2.2 Experimental Methods

Many techniques exist to extract thermal properties at nanometer length scales. Such methods rely on measuring the temperature response of a material to heat input. These methods achieve high thermal resistance resolutions by confining their heat inputs either temporally or spatially. Examples of temporal confinement techniques include time-domain thermoreflectance [49, 50] and the 3ω technique [1]. In these examples, a heating pulse or high-frequency heating signal confines the measured region to the thermal penetration depth of the sample. This depth is defined by:

$$d_{thermal} = \sqrt{\alpha\tau} \tag{4.6}$$

where α is the thermal diffusivity of the heated film, and τ is the characteristic time of the heating event. For a heating event, this could be roughly defined as the full-width half maximum (FWHM) of the pulse. For a high-frequency measurement, τ is defined as the heating period. Spatial confinement, on the other hand, restricts the depth of heating by using varying widths of heater structures. Examples of this include steady-state electrical thermometry measurements [8, 162] based on structures similar to the 3ω technique. Spatial confinement also allows one to extract in-plane thermal properties without the use of a suspended structure [100]. These techniques are grouped into the more general categories of optical and electrical thermometry. The methodology behind TDTR has been explained earlier in this work, so this section shall focus on the electrical techniques involved.

Frequency-domain electrical thermometry, known as the 3ω technique [1], measures the two-dimensional thermal conductivity of a Mo/Si multilayer sample. The metal patterns consist of 5 nm of titanium as an adhesion layer and 55 nm of gold as heater bridges. Electron-beam lithography fabricates the fine structures of the heaters with line widths varying from 50 nm to 5 μm (fig. 4.7). When an AC current with frequency ω flows through the heater bridge, the voltage signal across it contains a 3rd harmonic (3ω) component due to Joule heating and the linear relationship between temperature and electrical resistivity of the metal heater. The amplitude of the 3ω component contains information of the thermal conductivity of underlying materials.

Wide heaters (5 μm) generate nearly one-dimensional heat conduction through the multilayer stack, which are sensitive to the out-of-plane thermal conductivity. Narrow heaters (50nm) induce two-dimensional heat transfer within a shallow region near the top, and capture the in-plane thermal conductivity. Since the Mo/Si multilayer stack is conductive with an electrical conductivity of $1.86\times10^{6}\ \Omega^{-1}\ m^{-1}$, an amorphous Al_2O_3 layer on the top provides electrical insulation. A reference sample with identical structures absent the Mo/Si multilayers is also prepared. The reference sample facilitates the separation of the contribution of Mo/Si multilayers to the measured total thermal resistance. The electrical measurements are performed at room temperature to minimize the interdiffusion between Mo and Si layers.

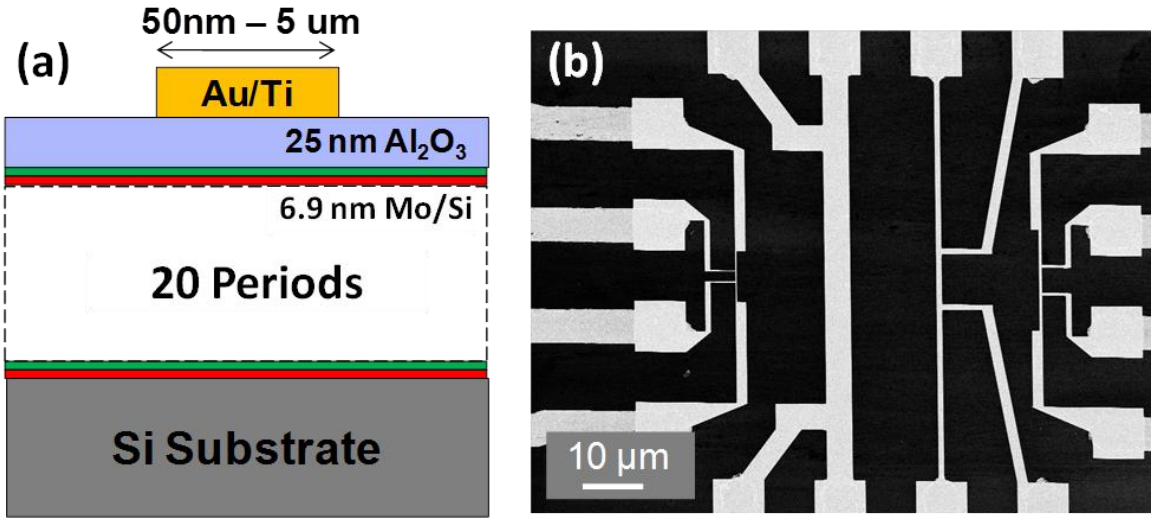

Fig. 4.7 Patterned heater bridges for electrical thermometry. (a) Sample schematic. The 25 Al2O3 layer provides insulation between the heater bridge and the Mo/Si multilayer. (b) Scanning electron microscope image of the patterned heater bridges with widths varying from 50nm to 5μm (not all widths are shown in this micrograph).

4.2.3 Multilayer Mo/Si Thermal Properties

The TaN and $MoSi_2$ samples were measured for a temperature range of 300 K to 700 K. Since the Mo/Si films are prone to interdiffusion at elevated temperatures, these samples were restricted to room temperature measurements. Table I reports a summary of the room temperature thermal property data obtained using TDTR and 3ω methods. The TaN data from Bozorg-Grayeli et al. [149] are also reported here.

Table 4.1 Thermal properties of the components of the Mo/Si multilayer mirror system measured at 300K using TDTR and 3ω techniques. k_{film} represents the measured thermal conductivity in the cross-plane direction. The 3ω $Mo_{0.4}/Si_{0.6}$ case notes the measured anisotropy ratio. The superscript, 'a', indicates that the range of values is due to annealing of the interface. The superscript, 'b', indicates that the range of values is due to size effects in the samples.

Sample	Technique	$R_{trans\text{-}film}$ [m^2 K GW^{-1}]	k_{film} [W m^{-1} K^{-1}]	$R_{film\text{-}si}$ [m^2 K GW^{-1}]
Al on TaN[149]	TDTR	5.5 – 7.6[a] (± 0.2)	3.0 – 3.4[b] (± 0.3)	N/A
Al on $Mo_{0.4}/Si_{0.6}$	TDTR	6.0 ± 0.2	1.1 ± 0.1	N/A
	3ω	N/A	1.2 ± 0.07 (η = 13 ± 2)	N/A
Ru on $Mo_{0.4}/Si_{0.6}$	TDTR	1.5 ± 0.1	1.1 ± 0.1	N/A
Al on $Mo_{0.6}/Si_{0.4}$	TDTR	6.9 ± 0.3	1.4 ± 0.1	N/A
Al on a-$MoSi_2$	TDTR	5.1 ± 1.0	1.7 ± 0.2	5.3 ± 0.5
Al on c-$MoSi_2$	TDTR	5.1 ± 1.0	2.8 ± 0.3	14.5 ± 2.0

Picosecond TDTR and 3ω measurements extracted the cross-plane thermal conductivity of the $Mo_{0.4}/Si_{0.6}$ multilayer, respectively, as 1.1 ± 0.1 W m^{-1} K^{-1} to 1.2 ± 0.07 W m^{-1} K^{-1}. The cross-plane conductivity of the $Mo_{0.6}/Si_{0.4}$ sample is slightly higher at 1.4 ± 0.1 W m^{-1} K^{-1}. This is due to the increased ratio of Mo, which is a more effective thermal conductor than a-Si. Li et al's recently-published nonequilibrium model of phonon-electron heat conduction through Mo/Si multilayers shows similar results [163], predicting thermal conductivities of 1.3 W m^{-1} K^{-1} for $Mo_{0.4}Si_{0.6}$ and 1.49 W m^{-1} K^{-1} for $Mo_{0.6}/Si_{0.4}$. Comparing the measured resistance of the bilayers to the values anticipated from bulk thermal properties reveals the effect of reduced film dimensions and TBR. Using a series resistor model with the bulk thermal properties of Mo, a-Si [164], and the measured thermal properties of a-$MoSi_2$, $Mo_{0.4}/Si_{0.6}$ gives a conductivity ~ 2.0 W m^{-1} K^{-1}. The thermal resistance of this ideal bilayer is ~ 2.8 m^2 K GW^{-1} lower than the measured result. Applying the series resistor model with bulk Mo, a-Si, and a-$MoSi_2$ properties to the $Mo_{0.6}/Si_{0.4}$ sample gives thermal conductivity ~ 4.9 W m^{-1} K^{-1}. This results in a

bilayer resistance ~ 3.5 m^2 K GW^{-1} lower than the measured result. There are several potential causes for this difference. The presence of multiple nanometer-scale layers in close proximity suggest that reduced energy carrier mean free path, frequent electron-phonon energy conversion, and ballistic heat conduction may contribute to the increased thermal resistance.

Because the 3ω measurement uses heater bridges with widths of 5 μm or thinner while the TDTR setup uses a 10 μm wide pump beam, it is more sensitive to thermal spreading in the film. Using narrow heater bridges with widths of 50-100 nm, which are more sensitive to the in-plane thermal conductivity, we find the thermal conductivity anisotropy ratio $\eta = k_{in-plane}/k_{out-of-plane} = 13 \pm 2$ for $Mo_{0.4}/Si_{0.6}$. The highly anisotropic thermal conductivities of the Mo/Si multilayers confirm that the frequent interfaces significantly impede the thermal transport in the out-of-plane direction. Li et al. speculate that samples consisting of higher Mo ratios will not exhibit significantly different anisotropy ratios [163].

TDTR measurements allow direct access to the transducer-film TBR. Using an Al transducer, the Al-Mo/Si TBR is 6.0 ± 0.2 m^2 K GW^{-1} for $Mo_{0.4}/Si_{0.6}$ and 6.9 ± 0.3 m^2 K GW^{-1} for $Mo_{0.6}/Si_{0.4}$. Using a Ru transducer to mimic the capping layer, the transducer-Mo/Si TBR decreases to 1.5 ± 0.1 m^2 K GW^{-1}. While this value is significantly lower than the TBR caused by Al, it still greatly affects the thermal resistance offered by the 2.5 nm Ru capping layer.

4.2.4 High Temperature $MoSi_2$ Thermal Properties

Since roughly one-third of the Mo/Si multilayer stack consists of an interdiffused layer, the thermal properties of a-$MoSi_2$ contribute significantly to the properties shown above. Room temperature measurements of the in-plane electrical conductivity of a-$MoSi_2$ returned a conductivity of 1.6 $m\Omega^{-1}$ cm^{-1}. Using the WFL law, this translates to an expected electron thermal conductivity of 1.2 W m^{-1} K^{-1}. Further, using the $MoSi_2$ density along with minimum thermal conductivity theory [153] estimates a phonon thermal conductivity of 1.6 W m^{-1} K^{-1}. The high temperature thermal properties of the $MoSi_2$ films are accessed using an optical access oven pumped to vacuum. The oven was

pumped down to vacuum to prevent oxidation of the transducer films. $R_{Al\text{-}MoSi2}$, k_{MoSi2}, and $R_{MoSi2\text{-}Si}$ were measured from 300 K to 700 K. Temperature ramps are performed at intervals of 100 K at a rate of 50 K/min, with a 30 minute hold at each temperature. The measurement requires ~ 15 minutes for each temperature. As a result, the total measurement time was ~ 7 hours.

During this process, k_{MoSi2} increased from 1.7 W m^{-1} K^{-1} to 2.8 W m^{-1} K^{-1} (fig. 4.8(a)). The increase in k_{MoSi2} was due to the crystallization of the samples (fig. 4.9). Previous measurements on sputtered $MoSi_2$ thin films have shown that annealing significantly increases electrical conductivity [165]. Chow et al. demonstrated a 6-fold increase in electrical conductivity after a 1-hour anneal at 900 ^oC, attributing this change to recrystallization of the film into tetragonal $MoSi_2$ [165]. Although crystallization can also increase the sound velocity and phonon mean free path relative to an amorphous film, the magnitude of the electrical conductivity change is significantly greater. As such, the majority of the thermal conductivity increase is likely due to improved electronic conduction. Subsequent high-temperature measurements of the heated films showed no change in thermal properties (fig. 4.8(b)), indicating that the samples were fully crystallized. The thermal conductivity of the interdiffused film in the multilayer is likely significantly below this value due to reduced carrier mean free path.

The $MoSi_2$-Si TBR increases significantly during the annealing process (fig. 4.10(a)), though it remains stable during subsequent high-temperature measurements (fig. 4.10(b)). This is due to the presence of interfacial stresses during the initial heating, resulting in delamination at the $MoSi_2$-Si interface. Such stresses may be due to mismatch in the lattice parameters [166, 167] or coefficients of thermal expansion [166, 168] of the two films. The TEM images of the crystallized $MoSi_2$ seem to confirm the delamination, showing small regions at the interface where the c-$MoSi_2$ and Si do not appear to be in contact. Figure 8 compares the film-substrate interfaces for amorphous and crystalline $MoSi_2$. The a-$MoSi_2$ in Figure 4.11(a) conforms to the Si substrate, while the c-$MoSi_2$ in Figure 4.11(b) shows detachment. Although the Al-$MoSi_2$ interface becomes rougher after annealing, it does not show any delamination, nor does it demonstrate an increase in TBR. This implies that the Al transducer deforms to relax the interface stresses.

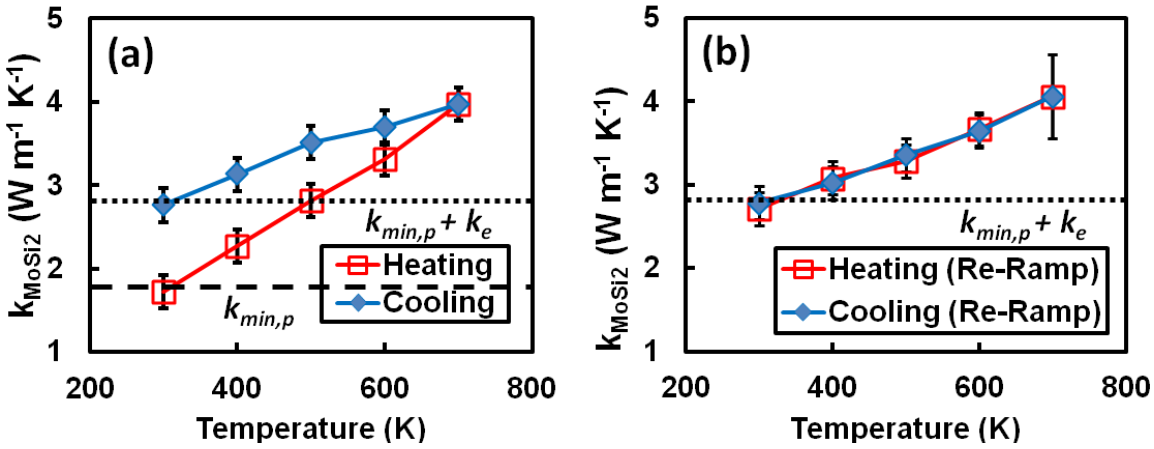

Fig. 4.8 Thermal conductivity of $MoSi_2$. Image (a) shows the first temperature ramp, and (b) shows the subsequent re-ramp. The thermal conductivity hysteresis in (a) is due to crystallization of the $MoSi_2$ film. In (b), the film has been fully crystallized, so no hysteresis effects are visible. The dotted lines indicate the estimated thermal conductivities obtained from the minimum thermal conductivity model ($k_{min,p}$) and from WFL estimates (k_e)

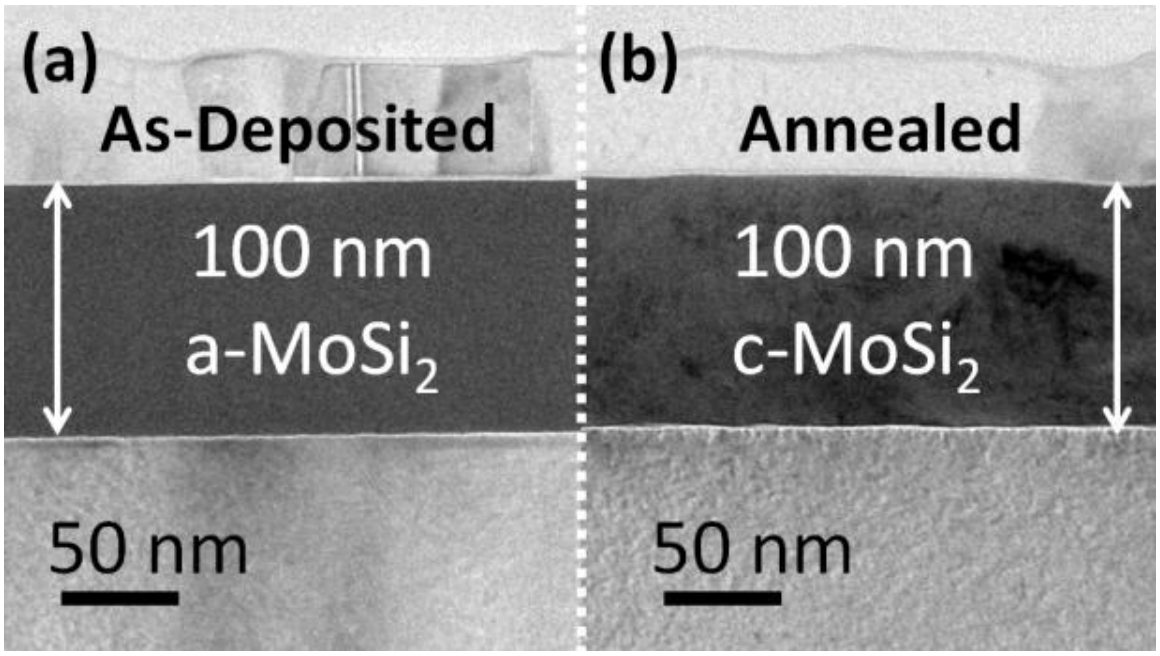

Fig. 4.9 Cross-sectional TEM images of the 100 nm as-deposited (a) and annealed (700 K) (b) $MoSi_2$ films, including transducer layer and substrate. (a) is completely amorphous, while (b) shows crystallization. Crystallization does not change the thickness of the film.

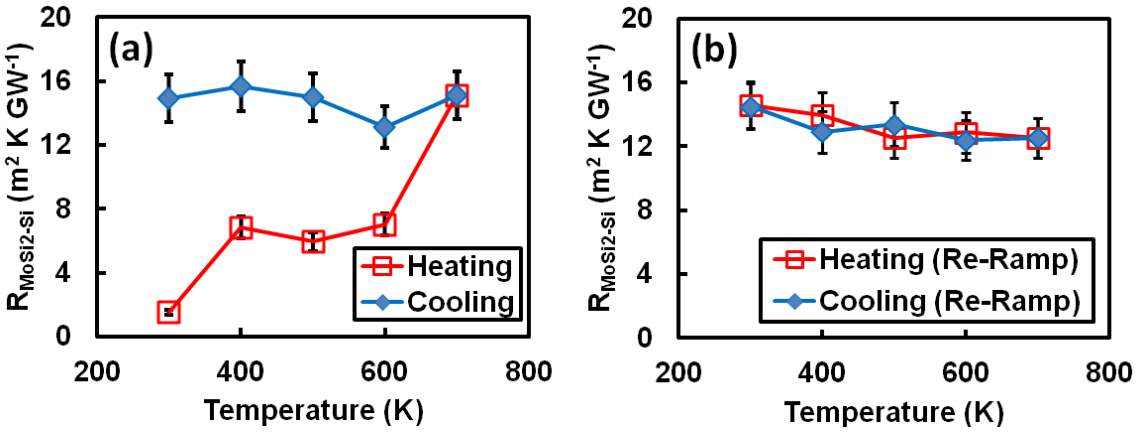

Fig. 4.10 Thermal boundary resistance between $MoSi_2$ and Si. Image (a) shows the first temperature ramp, and (b) shows the subsequent re-ramp. The TBR hysteresis in (a) is due to heating of the $MoSi_2$ film. This process creates interface stresses, resulting in delamination. In (b), the film has been fully crystallized, and demonstrates no additional hysteresis in TBR.

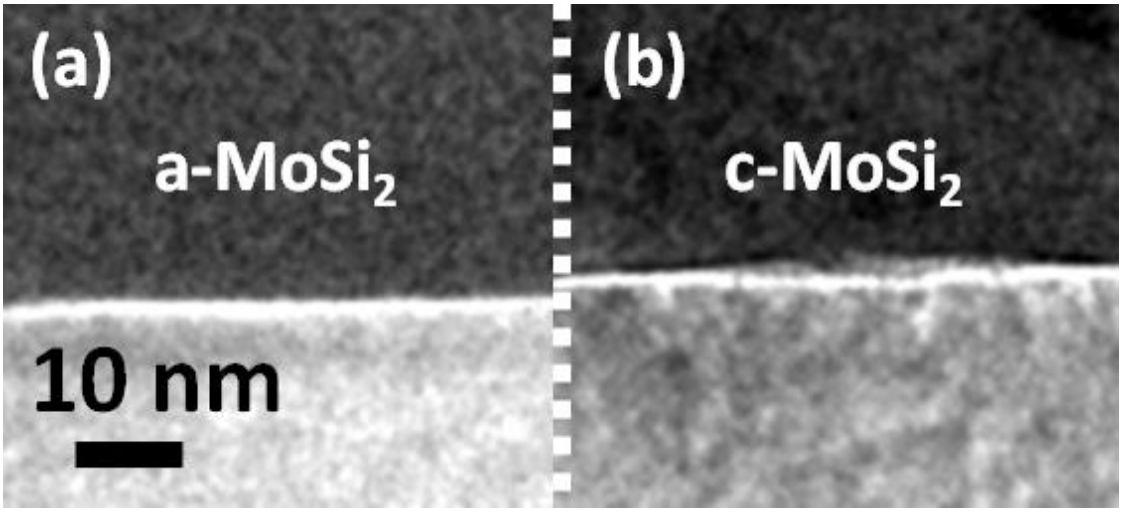

Fig. 4.11 Cross-sectional TEM images of the $MoSi_2$-Si interface for the (a) as-deposited and (b) annealed $MoSi_2$ films. While (a) demonstrates that the a-$MoSi_2$ conforms to the Si surface, (b) shows local deformed regions where c-$MoSi_2$ and Si do not seem to be in contact. This may be responsible for the increase in $R_{MoSi2\text{-}Si}$ upon annealing.

4.3 Damage Threshold Predictions for EUV Mirrors

High temperatures can significantly degrade the performance of EUV optics due to accelerated Mo-Si interdiffusion, resulting in loss of EUV reflectivity and machine downtime. It is critical, therefore, to determine an upper limit for EUV exposure which maximizes the usable lifetime of the optics. In this section, we demonstrate a finite

element thermal simulation of a multilayer Mo/Si mirror on a SiO_2 substrate. The temperature response in the model is used in combination with the Arrhenius equations for interdiffusion between Mo and Si to predict when mirror reflectivity at 13.5 nm degrades by 1%.

Before beginning any analysis, we must first define the point at which an EUV mirror is "damaged". Multiple authors have defined this damage threshold differently. Allain et al. define mirror damage as the point at which the collector optics become contaminated by debris from Sn- or Xe-based EUV sources [169]. Such contamination drops EUV reflectance by anywhere from 19% to 49%, depending on the energy of the contaminating particles. Barkusky et al. define the mirror damage threshold as the energy level which caused ablation [170]. For this damage mechanism, the peak temperature of the multilayer must be high enough to instantly vaporize a-Si, creating a visible crater in the mirror film. Surface damage was seen for fluences of 0.8-1.7 J cm^{-2} over a 8.8 ns pulse. Bender et al. also defined a visible damage threshold, though the damage mechanism was delamination of the multilayer rather than ablation [171]. In this case, the damage was seen for fluences of 0.26-0.5 J cm^{-2}. Khorsand et al. defined a third damage threshold condition [172]. Here, the film was damaged at a fluence of only 45 mJ cm^{-2} due to significant intermixing of the Mo and a-Si layers. The density of the resulting intermetallic was greater than the density of the consumed a-Si, resulting in compaction of the multilayer. Although Khorsand et al's measurements used ~10 fs EUV pulses, damage did not occur until significantly after the pulse was applied.

All of these damage thresholds were determined for a single EUV pulse. Louis et al. set a significantly lower threshold, suggesting that over 30,000 hours of operation, the mirror reflectance at 13.5 nm should not degrade by more than 1% [136]. As Louis et al. note, EUV projection optics can have 6 or more mirrors in place to control the beam. Assuming each mirror has a reflectivity of 65%, only 7.5% of the original EUV fluence incident on the mask actually reaches the wafer. If each mirror experiences a 1% drop in reflectivity, 7.1% of the original signal remains. This change is not acceptable in an industry where every photon counts. Therefore, this study defines damage as the point at which mirror reflectance at 13.5 nm degrades by 1%.

Ablation, melting, and delamination occur for EUV fluences of 0.1-1.0 J cm^{-2} over a ~10 ns pulse [170, 171]. These fluences induce temperatures on the order of the melting point of amorphous silicon (~1400 K [173]), and cause reflectance drops significantly greater than 1%. Compaction, however, occurs at lower temperatures and over longer timescales. Even if the EUV fluence is low enough to avoid ablation, melting, and delamination, the compaction that takes place over the lifetime of the mirror would still cause a 1% reflectance drop. Therefore, compaction is the damage mechanism which sets the upper limit for EUV fluence on a multilayer mirror. In this section, we use a finite element thermal model to determine the temperature response of a multilayer Mo/Si mirror on SiO_2 to EUV pulses of varying pulsewidth. We predict the compaction damage threshold of a mirror for both single and multiple EUV pulses. Rather than Louis et al's 30,000 hour requirement [136], we use the expected lifetime of an EUV source (10^9 pulses) to define mirror lifetime under the multiple pulse condition [144].

4.3.1 Predicting Compaction Damage

The wavelength of the reflectance peak of a Mo/Si multilayer relates directly to the periodicity of the stack. As this periodicity decreases, so does the peak reflectance wavelength. Using a MATLAB adaptation of the multilayer reflectance algorithm developed by Windt [145], the optical properties of Mo, Si, and the Ru capping layer [174], and the geometry shown in figure 4.7, we find shrinking the bilayer by 7 pm reduces reflectance at 13.5 nm by 1%. We therefore define 7 pm of compaction per bilayer as the damage threshold.

Multilayer compaction is driven by the formation of $MoSi_2$ due to interdiffusion between the Mo and a-Si films. Heating the mirror above room temperature accelerates this process. Holloway et al. [140], Rosen et al. [141], and Zubarev et al. [142] characterized the interdiffusion rate using an Arrhenius model (equations (4.1) and (4.2)). In particular, Rosen et al. reported an activation energy of 2.4 eV and a diffusion coefficient of 50-100 $cm^2\ s^{-1}$ for the Mo on a-Si interface [141]. The diffusion coefficient for the a-Si on Mo interface is roughly 10 times smaller than that of the Mo on a-Si interface [141], and the latent $MoSi_2$ grown on this interface during deposition does not

expand at elevated temperatures [140]. Our analysis, therefore, only considers interdiffusion for the Mo on a-Si interface.

According to Nedelcu, the formation of 1.0 nm of $MoSi_2$ consumes 1.0 nm of a-Si and 0.4 nm of Mo, causing 0.4 pm of compaction [175]. Therefore, to obtain 7 pm of compaction, the $MoSi_2$ layer must grow by 17.5 pm, consuming 24.5 pm of Mo and a-Si. We define this damage threshold condition via:

$$w_f^2(\tau) = \int_0^t 2D_0 \exp\left(-\frac{E_\alpha}{k_B T(t')}\right) dt' \tag{4.7}$$

where w_f is the thickness of the grown $MoSi_2$ interlayer, τ is the simulated mirror lifetime, and all other parameters are as described in equation (4.1).

4.3.2 Single Pulse Damage Threshold

When considering the temperature response of the mirror under pulsed optical loading, there are two timescales of interest: single-pulse and 10^9-pulse. These timescales, in turn, depend upon the pulse width and repetition rate of the EUV source. Pulsewidths for EUV sources tend to be ~ 1 ns – 1 μs, with repetition rates from 1 Hz to 100 KHz [144, 170, 171, 176, 177]. For laser produced plasmas, the pulsewidth and repetition rate of the pump laser controls these properties. For discharge produced plasmas, the governing factors are the current rise time and oscillation frequency. For single pulse simulations, we select a pulsewidth range of 1 ns to 1 μs. The thermal penetration depth at these timescales, given by equation (4.6) assuming a SiO_2 substrate, is less than 10 μm. Considering EUV source beams are ~ 100 μm in diameter, this indicates that thermal diffusion during a single pulse is effectively 1-D.

The 1-D thermal model is built in COMSOL, and consists of a two-layer structure of 283 nm Mo/Si multilayer on a 1 cm SiO_2 substrate. The Mo/Si layer has a cross-plane thermal conductivity of 1.1 W m^{-1} K^{-1}, and the SiO_2 substrate has a thermal conductivity of 1.38 W m^{-1} K^{-1}. Heat is deposited in the Mo/Si layer according to the relation:

$$I(z) = I_0 e^{-z/\alpha} \tag{4.8}$$

where I_0 is the optical intensity at the top of the Mo/Si, α is the optical absorption depth at 13.5 nm in Mo/Si, and z indicates depth into the film. For the multilayer mirror, the optical penetration depth at EUV is ~93 nm [170]. Equation (4.8) is an approximation of the intensity profile in the multilayer. The actual profile is significantly more complex. Applying the Windt algorithm to find the intensity distribution [145], we show that the Ru and Mo layers absorb nearly all of the optical energy while the Si layers are essentially transparent (fig. 4.12). However, it takes less than 40 ps for the heat deposited within a single Mo layer to diffuse through the neighboring Si film. While this timescale is long enough to be of concern for fs-scale damage mechanisms [172], it is too short to impact compaction, since the heat redistributes within the pulsewidth. Therefore, we use equation (4.8) within our simulation to approximate the heating density within the multilayer mirror. We plug the maximum temperature (at the top of the multilayer) as a function of time into (4.7) and fit for the pulse fluence which results in damage after 1 pulse (fig. 4.13).

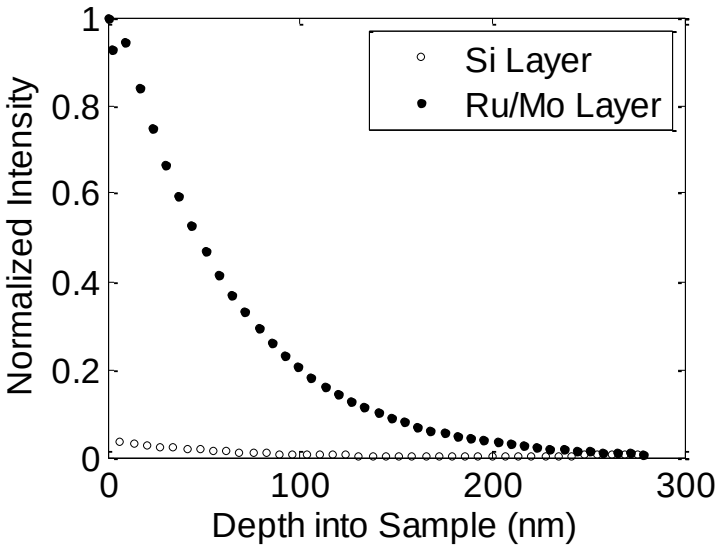

Fig. 4.12 Normalized intensity profile in the $Mo_{0.4}/Si_{0.6}$ multilayer mirror for a 40 bilayer structure. The Ru and Mo layers absorb nearly all of the heat, while the Si layers are effectively transparent. However, since the bilayer is extremely thin, the heat redistributes in the bilayer within 40 ps.

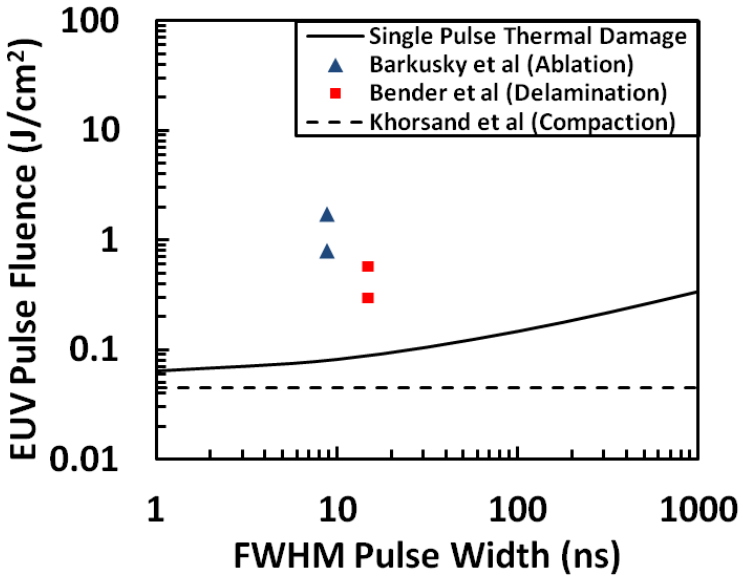

Fig. 4.13 Comparison of simulated damage threshold for a multilayer Mo/Si mirror with experimental results from Barkusky et al. [170], Bender et al. [171], and Khorsand et al. [172]. The results from Khorsand et al. are indicated by the dotted line since the authors noted that damage did not occur until significantly after the pulse was applied. The solid line indicates the compaction damage threshold.

The simulated damage threshold is a strong function of pulse width. Shorter pulses cause higher peak intensities under the same EUV fluence. This, in turn, causes higher peak temperatures and accelerated compaction. The damage thresholds measured by Barkusky et al. and Bender et al. are significantly higher than our simulated results due to their selection of ablation and delamination as damage mechanisms [170, 171]. Khorsand et al. define compaction as their damage condition, demonstrating a threshold EUV fluence similar to our result [172]. While their pulse width was only ~10 fs long, damage did not occur until significantly after the application of the pump. This delay was the result of: 1) the time required by electrons in the Mo layers to thermalize with the lattice, and 2) the time required for the heat in the Mo layers to diffuse outwards. Our simulation defines a damage threshold range of 64 mJ cm^{-2} at 1 ns to 338 mJ cm^{-2} at 1 μs. This value decreases significantly if we apply multiple pulses, especially for repetition rates which do not allow recovery of the multilayer and substrate to room temperature

.

4.3.3 Multiple Pulse Damage Threshold

For longer timescales, i.e. 10^9 pulses, we cannot assume 1-D heat spreading. In this case, if the repetition rate is high enough such that temperature does not fully recover between pulses, we must account for the steady state temperature rise. To do so, we simulate a 100 μm diameter beam on a 1 cm glass substrate. We account for the reflectivity of the multilayer coating by absorbing only 35% of the incident energy. Since the thermal penetration depth is significantly larger than the coating thickness, we neglect the multilayer thermal resistance in favor of the substrate spreading resistance. We confirm this assumption using the spreading resistance model for conduction from a heated disk to a semi-infinite material [178]:

$$R_{sub} = \frac{1}{2Dk_{SiO2}} \tag{4.9}$$

where D is the diameter of the beam and k_{SiO2} is the thermal conductivity of the quartz substrate. Since EUV source beams are cylindrical rather than Gaussian in profile, equation (4.9) offers an accurate representation of the substrate thermal resistance at long times. Using this formula, we find a substrate resistance of 3.57 K mW^{-1}. The multilayer thermal resistance is given by:

$$R_{film} = \frac{4L_{film}}{\pi D^2 k_{film}} \tag{4.10}$$

where L_{film} is the multilayer thickness and k_{film} is the multilayer thermal conductivity. The film resistance is 0.033 K mW^{-1}, and is therefore negligible compared to the spreading resistance.

The 3-D spreading model built within COMSOL consists of a 100 μm cylindrical heating source on a 10 cm wide and 1 cm thick SiO_2 substrate. We simulate a heat sink at room temperature at the lower surface of the substrate and apply a heating intensity based on the repetition rate and pulse energy of our source:

$$I_{abs} = I_{total}(1 - R) = f_{RR}E_{pulse}(1 - R) \tag{4.11}$$

where I_{abs} is the absorbed optical intensity, I_{total} is the total optical intensity incident on the multilayer, f_{RR} is the repetition rate of the EUV source, E_{pulse} is the pulse fluence, and R is the reflectivity of the multilayer. After calculating the steady state temperature, the pulsed temperature response of the multilayer becomes:

$$T_{MP}(t) = T_{ss} + T_{SP}(t) - T_{SP}(0) \tag{4.12}$$

where T_{MP} is the multiple pulse temperature response of the multilayer, T_{SP} is the single pulse temperature response of the multilayer, and T_{SS} is the steady state temperature of the substrate. We plug T_{MP} into equation (4.7), and determine the EUV fluence which would cause damage after 10^9 pulses. Here, we simulate two different repetition rates: 1) the pulses are adequately spaced to allow the multilayer to fully recover to room temperature, and 2) a 100 KHz repetition rate. As figure 4.14 demonstrates, the full recovery damage threshold depends on pulsewidth, implying that the majority of compaction occurs during the short temperature peaks. However, the 100 KHz case shows little dependence on repetition rate, implying that the steady state temperature rise applied over the lifetime of the mirror is most responsible for compaction.

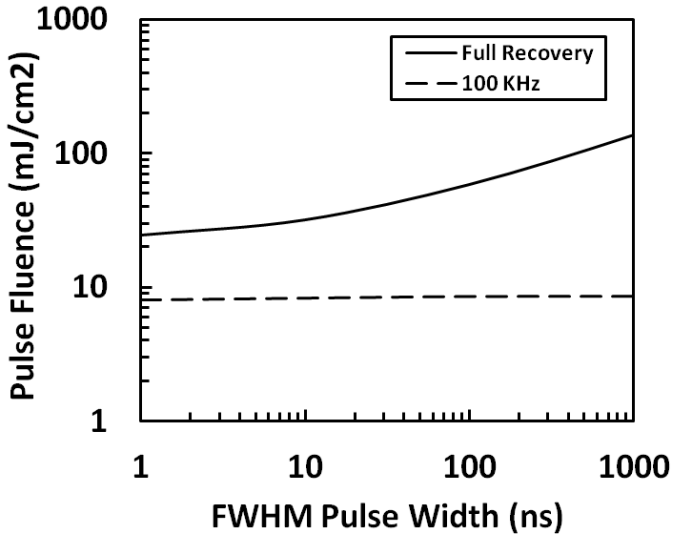

Fig. 4.14 Comparison of simulated damage threshold for a multilayer Mo/Si mirror undergoing 10^9 EUV pulses. The damage threshold decreases for higher repetition rates, down to ~ 8 mJ cm^{-2} for 100 KHz. The pulse width dependence of the damage threshold also decreases at high repetition rates due to thermal storage between pulses.

4.3.3 Conclusions on Multilayer Mirror Damage

Multilayer compaction is the damage mechanism of most concern for an EUV mirror. While not as immediately apparent as ablation or delamination, compaction sets the ceiling for EUV fluence on a multilayer mirror. This damage mechanism depends on both the timescale and temperature rise of a heating event. For single pulse damage, the short heating period induces damage mainly during the high peak temperature. For this reason, the single pulse damage threshold is highly dependent on the pulsewidth of the source. Over multiple pulses, however, thermal storage raises the temperature of the multilayer in between doses. Although the multilayer temperature is not as high as for a single pulse, the heating timescale is significantly longer, resulting in compaction damage. For this reason, as one moves to higher repetition rate sources, the damage threshold of the multilayer mirror becomes less dependent on pulsewidth and more dependent on the time-averaged EUV intensity.

Chapter 5
Conclusions

The work shown in this dissertation used ultrafast thermoreflectance to enhance our understanding of the thermal processes at work in three classes of next generation technologies: phase change memories, high electron mobility transistors, and extreme ultraviolet mirrors. This chapter summarizes the contributions of these results to the field, and provides a few selected avenues for future nanoscale heat transfer research

5.1 Phase Change Memory

Knowledge of the thermal properties of phase change memory materials is crucial to the design and operation of such devices. In this work, we first demonstrated the use of nanosecond thermoreflectance to extract the thermal conductivity of the phase change material GST and the thermal boundary resistance between GST and four electrode materials: C, TiN, low temperature deposited Ti, and high temperature deposited Ti. Although NTR was capable of extracting the intrinsic GST thermal conductivity, the timescale of the measurement was too large to directly measure the GST-electrode TBR. We therefore designed samples consisting of multilayer GST-electrode stacks with varying GST thickness, and used the relation between thermal resistance and thickness to extract both the intrinsic GST thermal conductivity and GST-electrode TBR. In doing so, we found that low temperature deposited Ti offered the highest GST-electrode, followed by C. However, amorphous carbon is known to have a significantly lower thermal conductivity than Ti. Since a low total electrode thermal resistance is desired to minimize heat loss from a PCM cell, this complicates the electrode selection. For an electrode less

than 30 nm in thickness, low temperature deposited titanium offers a higher total thermal resistance than carbon. However, if the electrode is more than 30 nm thick, the intrinsic carbon thermal resistance outweighs the TBR.

To determine if we could engineer an electrode to offer both low intrinsic conductivity and high GST-electrode TBR, we analyzed two multilayer electrode films. One consisted of a bilayer C/TiN structure, while the other consisted of W/WN_x. We used picosecond thermoreflectance measurements of single film C, TiN, and WN_x from room temperature to 400 ^{o}C to extract the thermal properties of the individual films. We combined these results with TDTR measurements on the multilayer stacks, and subtracted out the intrinsic resistances to determine the C-TiN and W-WN_x TBRs. These results showed a high C-TiN TBR, implying that one could design a multilayer C-TiN electrode with a desired periodicity to sensitively control the total electrode thermal resistance.

The total thermal resistance of the GST-electrode system also depends on the energy carriers involved in heat transfer. In the case of amorphous or FCC-GST, the primary energy carriers are lattice vibrations. However, in HCP-GST, electrons and phonons contribute on the same order to thermal conductivity. As such, electrons may offer a second energy transfer route at the interface between GST and an electrode, potentially reducing the TBR below predictions based on phonon scattering. We examined this principle by annealing a sandwich structure of TiN-GST-TiN with two thicknesses of GST. Although both exposed to the same temperatures for the same time, the thicker sample crystallized into HCP-GST while the thinner sample remained FCC. The HCP sample showed a lower TBR than the FCC sample, even though both were annealed at the same condition. However, electrical resistivity measurements found the electron boundary resistance to be several orders of magnitude higher than the phonon boundary resistance. Further, by analyzing the additional phonon energy generated through electron-phonon coupling at the interface, we eliminated the possibility of electrons affecting TBR at the HCP GST-TiN interface. We therefore ascribed the difference in TBR to structural differences between the FCC and HCP interfaces.

5.2 Diamond Substrates for High Electron Mobility Transistors

High electron mobility transistors must operate under power densities significantly greater than for commercial processors. High thermal conductivity diamond films are seen as potential successor substrates for HEMTs. However, excessive substrate-GaN TBR can negate the benefits of a diamond substrate. Further, the high density of scattering sites in the diamond coalescence region may significantly reduce the thermal conductivity of the substrate. Using a thermal spreading model for a HEMT hot spot on GaN on substrate, we demonstrated a TBR criterion to determine when diamond should be used as a substrate in place of SiC.

To see if a diamond film could satisfy this criterion, we measured the thermal properties of a diamond on poly-AlN structure using picosecond thermoreflectance. Varying magnification objective lenses controlled the sensitivity of the technique to 3D heat spreading in the thick diamond film. Using the lower magnification objective, we determined the diamond thermal conductivity and diamond-AlN interface resistance. From the higher magnification objective, we determined the thermal anisotropy factor of the diamond film. The low quality poly-AlN growth surface inhibited the growth of larger diamond grains, resulting in a low diamond thermal conductivity and high diamond-AlN interface resistance.

The diamond coalescence region can add significant thermal resistance to a diamond-GaN interface. We extracted the thermal properties of this coalescence region using TDTR measurements on both surfaces of a suspended diamond thin film. In doing so, we demonstrated significantly lower thermal conductivity in the coalescence region than in the high-quality columnar grain diamond. Further, using the properties of both regions along with a two-layer heat diffusion model, we determined the thickness of the coalescence region, and found it to be less than 1 μm. The thermal resistance of the coalescence region is equivalent to ~12 μm of high-quality diamond.

5.3 Extreme Ultraviolet Mirrors

Extreme Ultraviolet lithography enables the next several nodes of Moore's law. The mirrors and masks in EUV tools, based on multilayers of Mo and a-Si, are

susceptible to damage at high temperatures over extended periods of time. In particular, the thermally-driven interdiffusion between Mo and Si results in compaction of the bilayer, shifting the reflectance peak wavelength down and reducing the reflectivity at the 13.5 nm lithography wavelength. This work determined the thermal properties the materials involved in an EUV mirror/mask structure, and used the results to calculate an EUV damage threshold for single-pulse and multiple-pulse operation.

Electrical resistivity measurements on the TaN masking material showed thickness dependence for films 50-100 nm thick. Using this thickness dependence, we extracted the electron mean free path in the film absent boundary scattering. Combining this result with TDTR measurements of tantalum nitride at high temperature revealed the temperature- and thickness-dependent TaN thermal conductivity.

TDTR also extracted the temperature-dependent thermal properties of the amorphous and crystalline phase of the $MoSi_2$ intermetallic formed during compaction. Crystallization significantly increased the thermal conductivity of $MoSi_2$, likely due to improved electron conductivity in the film. We also observed a large increase in the $MoSi_2$-substrate TBR after annealing the film. This increase remained after subsequent anneals. Cross-sectional TEMs revealed this to be due to detachment at the $MoSi_2$-substrate interface.

The thermal properties of the Mo/Si multilayer measured here were significantly lower than previously assumed in the literature. Multiple nanometer-scale layers in close proximity suggest that this reduction comes from lower energy carrier mean free path, frequent electron-phonon energy conversion, and ballistic heat conduction in the bilayers.

Using these results, we created a thermal model for the temperature response of a mirror heated by an EUV pulse. From this temperature profile, we predicted the compaction damage threshold of an EUV mirror subjected to: 1) a single EUV pulse, and 2) 10^9 EUV pulses. The single-pulse damage threshold is significantly more sensitive to the pulsewidth than the multiple-pulse damage threshold. This illustrates that, at shorter timescales, compaction is more dependent on the high peak temperature. At longer timescales, thermal storage raises the multilayer temperature between pulses. Although

this temperature is lower than the peak, it is applied for a significantly longer time, resulting in compaction damage.

5.4 Suggestions for Future Research

Ultrafast thermoreflectance is a versatile technique which can extract thermal properties at nanometer length scales using minimal preparation. However, actual device geometries are significantly more complex than the structures measured here, especially in the context of PCM. Lateral confinement of PCM cells can significantly impede thermal conduction in the device due to phonon boundary scattering. Further, while much is known about the thermal and electrical properties of phase change memory materials, comparatively little work exists on these properties during phase change. Because phase change processes occur on timescales shorter than the resolution of most measurement techniques, these properties are difficult to measure. Lastly, efforts to understand the molten properties of phase change materials are hampered by the enormous mechanical stresses exerted by the liquid phase on the surrounding materials. For these reasons, we propose a Nanosecond Thermal Platform which integrates electrical, optical, and thermal switching methods to extract the thermal properties, electrical properties, and phase change behavior of spatially confined GST on timescales ~10 ns.

Although the large thermal time constant of an oven precludes the possibility of measuring electrical phenomena during phase change, structures such as those proposed by Lee et al. [179] offer ways to thermally or electrically switch a PCM device on timescales approaching those seen in electrical and optical switching (Fig. 5.1). The Micro-Thermal Stage (MTS) measures electrical and thermal conductivity changes down to 10 μs timescales. The thermal mass of the MTS heater, though significantly smaller than any other thermal heating method, restricts the thermal time constant to a 10 μs floor. While this is sufficient for drift measurements, switching-induced electrical conductivity changes are only resolvable on timescales less than 100 ns, which cannot be achieved using electrical heating methods.

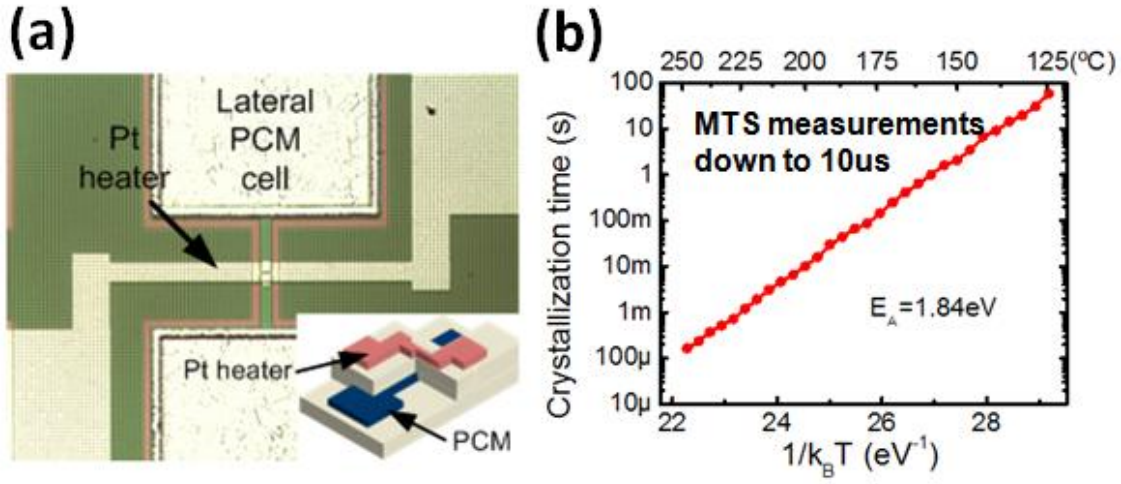

Fig. 5.1. (a) Top-down and cross-sectional view of the MTS electrothermal test bed. (b) This structure is capable of resolving changes in electrical and thermal properties on timescales approaching 10 µs.

We propose a Nanosecond Thermal Platform (NTP) to circumvent the thermal mass issues posed by electrically-heating PC materials. This technique uses a lateral PCM cell which allows optical access to the GST layer through a transparent oxide coating (Fig. 5.2). A Q-switched Nd:YAG laser will pump the GST with a ~10 ns optical pulse, rapidly inducing phase change. Figure 5.3 illustrates the optical reflectance change vs. time for a proof-of-concept measurement performed using a 6 ns pulse on a 150 nm blanket GST film. The thermal time constant of the decay is significantly smaller than for the MTS structure, allowing direct measurement of the crystallization and amorphization processes. Further, the rapid heating and cooling of the GST in the NTP structure also allows electrical conductivity measurements of the molten state without subjecting the rest of the structure to extended periods of mechanical stress. The NTP structure also allows for the opposite measurement to be performed. In this case, the GST layer is electrically pumped and optically probed. This technique may be used to optically determine the phase content of the GST layer as a function of cycling life.

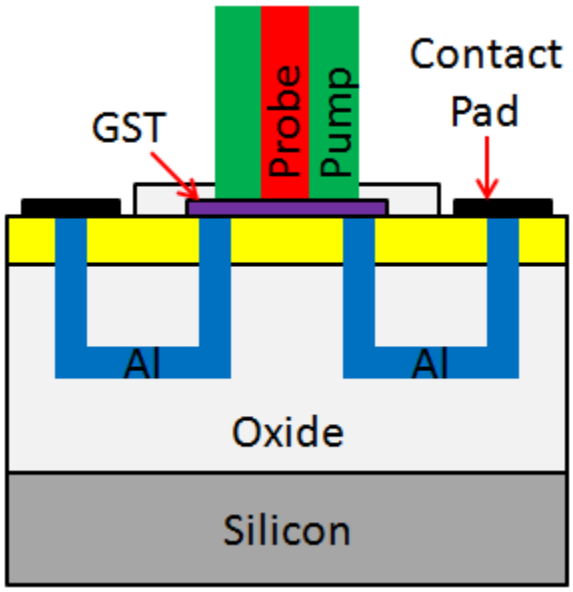

Fig. 5.2. Cross-sectional view of the NTP. The oxide coating allows optical access from a pump or probe laser to either heat the GST or probe its reflective properties. Simultaneous electrical probing/pumping takes place through the contact pads.

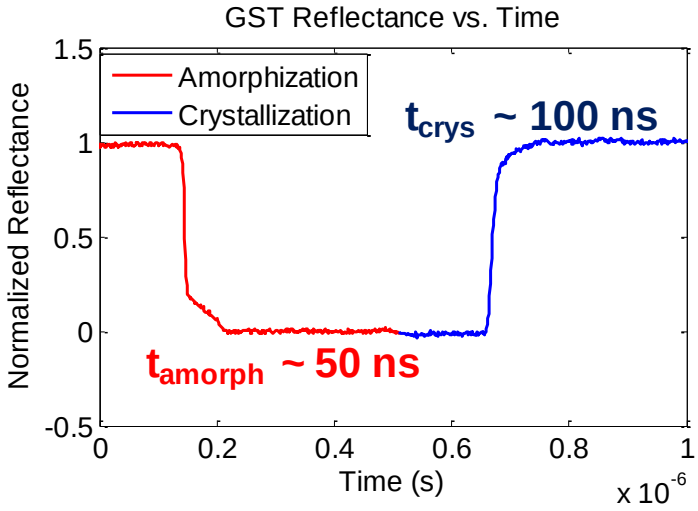

Fig. 5.3. Normalized reflectance of a 150 nm blanket GST film after 6 ns optical pulse to amorphize and crystallize the film, where 0 indicates complete amorphization and 1 indicates complete crystallization. The total process takes place over ~ 100 ns. The thermal mass of the MTS prevents resolution of this change, but it is resolvable with the NTP.

5.5 Final Thoughts

Ultrafast thermoreflectance allows us to gain a greater understanding of thermal properties at nanometer length scales. This data allows designers to make informed decisions regarding materials, geometries, and operating conditions of their devices. As heat fluxes within semiconductor devices continue to climb higher, this knowledge will become even more critical. We must therefore continue to drive innovation in both experimental and analytical techniques to keep pace with the rapidly expanding landscape of nanoscale thermal physics.

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