THERMAL CONDUCTION PHENOMENA IN NANOSTRUCTURED SEMICONDUCTOR DEVICES AND MATERIALS

A DISSERTATION

SUBMITTED TO THE DEPARTMENT OF MECHANICAL ENGINEERING

AND THE COMMITTEE ON GRADUATE STUDIES

OF STANFORD UNIVERSITY

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS

FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY

Zijian Li

August 2012

This dissertation is online at: http://purl.stanford.edu/yj710pk3626

I certify that I have read this dissertation and that, in my opinion, it is fully adequate in scope and quality as a dissertation for the degree of Doctor of Philosophy.

Kenneth Goodson, Primary Adviser

I certify that I have read this dissertation and that, in my opinion, it is fully adequate in scope and quality as a dissertation for the degree of Doctor of Philosophy.

Mehdi Asheghi

I certify that I have read this dissertation and that, in my opinion, it is fully adequate in scope and quality as a dissertation for the degree of Doctor of Philosophy.

Philip Wong

Approved for the Stanford University Committee on Graduate Studies.

Patricia J. Gumport, Vice Provost Graduate Education

This signature page was generated electronically upon submission of this dissertation in electronic format. An original signed hard copy of the signature page is on file in University Archives.

Abstract

Thermal phenomena have become very important in a variety of nanostructured semiconductor devices and materials. The reduced dimensions and large interface densities lead to complex thermal phenomena which do not occur in bulk materials and larger devices. Successful designs of high-performance semiconductor devices, including phase change memory (PCM) and high electron mobility transistors (HEMT), rely on the accurate thermal characterization of thin film materials and improved understanding of nanoscale energy transport physics. This thesis addresses nanoscale thermal transport problems relevant for three promising electronics technologies.

The first part of this work investigates thermal conduction phenomena in phase change memory. A combination of frequency-domain electrical thermometry and suspended microstructure design are used to measure the in- and out-of-plane thermal conductivities of thin-film $Ge_2Sb_2Te_5$ in the amorphous and crystalline phases. The preferential grain orientation and mixed phase distribution lead to a reduced in-plane thermal conductivity that is 60% – 80% of the out-of-plane value. Anisotropic heat conduction benefits PCM devices by reducing the programming current and mitigating the thermal disturbance to adjacent cells. A fully coupled electrothermal simulation unveils the detailed transient phase distribution during a programming operation, enabling more efficient structural designs for multilevel memory operation.

This research extends the thermal characterization and modeling techniques to diamond-based high electron mobility transistors. The high thermal conductivity of the diamond provides superior thermal performance and allows for up to 10x higher power density. Nanoheaters down to 50 nm wide are patterned by electron-beam lithography in order to measure the thermal resistance experienced by the single transistor channel, the multi-gate configuration, and the device package. The thermal resistance data reveals the critical role of thermal interface between the GaN device

layer and the diamond substrate. This work established a criterion for the diamond technology to be viable in HEMT applications. Specifically, the thermal interface resistance needs to be less than 30 m^2K/GW.

The lengthscales of thermal conduction studied in this research are further scaled down to a few nanometers in the final portion of this work. This work measures the thermal properties of the mirror material for extreme ultra-violet (EUV) lithography as the next-generation semiconductor manufacturing technology. The thermal transport across the interfaces of drastically different materials, such as the Mo/Si multilayers (2.8 nm / 4.1 nm), is important in the performance and reliability of the EUV mirrors. This work demonstrates strong anisotropy in the thermal conductivities of the multilayers, where the in-plane conductivity is 13 times higher than the out-of-plane value, owing to the high density of metal-semiconductor interfaces. This research reveals that thermal conduction in such periodic multilayer composites is largely determined by the nonequilibrium electron-phonon physics. A new model indicates that two additional mechanisms – quasi-ballistic phonon transport normal to the metal film and inelastic electron-interface scattering – can also impact conduction in metal-dielectric multilayers with period below 10 nm, the critical length scale for the EUV mirrors.

Acknowledgments

I am indebted to the many individuals whose support and encouragement made this dissertation possible. I am deeply grateful to my advisor, Professor Kenneth Goodson, for giving me the opportunity and autonomy to pursue my research interests throughout my Ph.D. program. I am immensely indebted to his encouragement, support and patience, especially at times when my research entered difficult phases. I benefited greatly from the opportunity that Professor Goodson provided me to participate in multiple interdisciplinary projects and collaborate with researchers both within and outside Stanford. I would like to thank Professor Mehdi Asheghi for his support and guidance for all my research projects. I greatly enjoyed our numerous discussions which generated some of the best ideas for solving practical problems. Throughout my years at Stanford, I had the privilege to work with Professor Philip Wong on phase change memory. His expertise in semiconductor physics and modern memory devices opened my eyes and helped shape my interest at the intersection of mechanical and electrical regimes. Besides research, I cherish his invaluable advice on my personal and professional development from which I have benefited greatly. I thank members of my dissertation defense committee: Professor James Harris of the Department of Electrical Engineering, Professor Sindy Tang of the Department of Mechanical Engineering, and Professor Alberto Salleo of the Department of Materials Science and Engineering. I highly appreciate their constructive challenges to my thesis research and their valuable feedback which enlightened me on the many interdisciplinary applications of the nanoscale heat transfer. I would like to acknowledge the close collaborations with many individuals on various aspects of this work. I thank John Reifenberg for his mentorship when I first joined the lab. It has been my honor to work with Jaeho Lee, Elah Bozorg-Grayeli, Rakesh Jeyasingh, and Jungwan Cho on our projects for the past several years. I extend my special thanks to Takashi Kodama who helped with the nanofabrication of many samples. I also owe many thanks to my fellow group members for their support, input, and collaborative

spirit: Matt Panzer, Jeremy Rowlette, Chen Fang, Milnus David, Julie Steinbrenner, Patricia Gharagozloo, SangBum Kim, Yoonjin Won, Amy Marconnet, Joe Miler, Yuan Gao, Saniya LeBlanc, Shilpi Roy, Sri Lingamneni, Michael Barako, Lewis Hom, Woosung Park, Aditya Sood, Si Tan, Scott Fong, and Ethan Ahn. The phase change memory team at Intel Corporation provided invaluable technical guidance and industrial perspectives, and special thanks to Kuo-Wei Chang, John Kalb, Davide Mantegazza, and Gianpaolo Spadini for the continued partnership over the past years. I would also like to thank Gil Delgado, Matthew Panzer, Alexander Pokrovsky, and Daniel Wack at KLA-Tencor Corporation for providing the samples and technical critics for the molybdenum/silicon multilayers project. In addition, I am grateful to the collaboration with Group4 Labs, Raytheon, and Northrop Grumman on the fundamental research on the high electron mobility transistors. Over the past years, CC Gichane-Bell and Linda Huber have helped me tremendously for all the administrative needs with great kindness and patience. I am also grateful to the Stanford Graduate Fellowship which made my study at Stanford possible, and NSF, SRC, DARPA, Intel, and KLA-Tencor for additional financial support. Finally, I would like to extend my wholehearted thanks to all my friends who have made my life at Stanford so colorful and memorable. I cannot thank family enough for their unconditional love and unwavering support which have inspired me every single day.

Table of Contents

List of Tables

List of Figures

Number *Page*

Chapter 1: Introduction

1.1 Motivation

Thermal conduction has become a critical consideration in the design and operation of many micro- and nanodevices. Advances in semiconductor devices over the past decade have generated a variety of unique structural and material properties in the nanometer length scales. The rapid reduction in the size of semiconductor devices requires improved understanding of heat conduction mechanisms involving complex nanostructures and interfaces. Classical heat transfer theory is largely based on a thermal equilibrium approach and an assumption of continuum behavior. At the nanoscale, however, the transfer of thermal energy may not be an equilibrium process and materials can exhibit non-continuum behavior. This is especially important when the device size or material structural characteristic lengths approach the mean free paths of the corresponding energy carriers (electrons and phonons), or when the timescale of interest is on the order of the thermal relaxation time of the energy carriers. In addition, progress in the design and synthesis of nanostructured materials has provided an opportunity to engineer the electrical, thermal, and phase change properties on the nanometer length scale in order to achieve unique device performance which is unattainable at longer length scales. Therefore, detailed studies of nanoscale heat transfer mechanisms are of fundamental importance to the continued development of nanostructured semiconductor materials and devices.

Three types of thermal transport problems are of particular interest for semiconductor nanodevices and materials. One is to utilize and manipulate the highly localized, intense heat flux in the nanodevices for applications such as data storage and energy conversion. Examples include phase change memory [1-3] and thermoelectric devices [4-6]. Another important area lies in the thermal management of semiconductor devices. Specifically, the continued scaling down of integrated circuits and increasing power density of electronic chips require advanced technology to remove the heat efficiently from the near-junction region where the characteristic

length scale ranges from several nanometer to several micrometer [7, 8]. Finally, the fundamental physics of the nanoscale thermal conduction and its impact on nanostructured materials have received increasing attention. For examples, nanometer sized hot spots can degrade the material and reduce device reliability due to localized thermal expansion [9] or atomic diffusion between the adjacent materials [10]. This thesis makes experimental and theoretical progresses in these areas in the context of specific applications including phase change memory, high electron mobility transistors, and ultrathin Mo/Si multilayer for extreme ultraviolet mirrors.

1.2 Nanoscale Heat Transfer

1.2.1 Thermal Transport Theories

In this work, heat transfer in solids is studied at two levels of detail and rigor: classical heat diffusion theory and kinetic theory. Classical heat diffusion theory, while less detailed, is often sufficiently rigorous for many thermal transport problems. Fourier's Law states that the heat flux in a certain direction is proportional to the negative temperature gradient along that direction:

$$\vec{q}'' = -\vec{k} \cdot \nabla T \,, \tag{1}$$

where T is the local temperature, $\vec{q}''$ is the heat flux, and $\vec{k}$ is the thermal conductivity of the medium. The application of the Fourier's Law to a three-dimensional medium without internal heat generation yields the classical heat diffusion equation:

$$\frac{1}{D}\frac{\partial T}{\partial t} = \eta\left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2}\right) + \frac{\partial^2 T}{\partial z^2}, \tag{2}$$

where D is the thermal diffusivity, t is time, and x, y, z are the dimensional coordinates. Because thin films in nanodevices often have different thermal conductivities along the in- and out-of-plane directions, the heat diffusion equation is modified with an anisotropy ratio $\eta = k_x/k_z$. Equation (2) is useful for bulk materials, as well as in thin film materials as long as the characteristic length scale is much larger

than the mean free path of the heat carriers. When using this classical heat transfer approach, details of energy carriers (phonons, electrons) are lumped together into the macroscopic properties (*e.g. D, k,* and η). The thermal modeling for the multibit phase change memory (Chapter 3) is mainly based on classical heat diffusion theory because the characteristic dimensions of the device (tens to hundreds of nanometers) are much larger than the phonon mean free path in the phase change material (~1 nm).

Kinetic theory, a more detailed treatment of thermal transport, considers the microscopic behavior and interactions of the energy carriers [11]. Electrons and phonons travel with known velocities and scatter with each other, and at a variety of imperfections including dopants, material defects, phase and grain boundaries, and material interfaces as shown in Figure 1. The mean free path describes the average distance that an energy carrier travels between two scattering events. Classical heat diffusion theory is no longer applicable when the characteristic length scale of the device becomes comparable or smaller than the mean free paths of the relevant heat carriers. For this reason, the theoretical modeling of most nanostructured materials in this thesis is built on the platform of the kinetic theory. The Boltzmann transport equation (BTE), derived from kinetic theory, keeps track of the number balance of the energy carriers and the scattering events in order to model thermal transport. This work mainly studies heat transfer in nanostructures in the absence of external electric forces, in which case the BTE can be written as [12]:

$$\frac{\partial f}{\partial t} + \mathbf{v} \cdot \nabla_{\mathbf{r}} f = \left(\frac{\partial f}{\partial t} \right)_{\text{scat}}, \tag{3}$$

where f is the distribution function of the particles, $\mathbf{v}$ is the group velocity vector, and the subscript $\mathbf{r}$ denotes the physical space. The BTE provides a powerful tool to study the detailed transport behavior of electrons and phonons within a medium [13-16] and also the heat transfer behavior across material boundaries [17, 18].

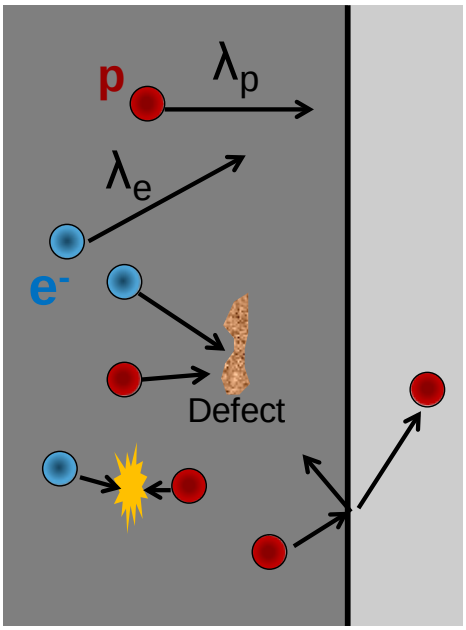


Figure 1. Schematic of the energy carriers in solids and their interactions. Phonons (P) and electrons (e^-) are the relevant heat carriers in the solids, and their mean free paths (λ_p and λ_e) describe the average distance the carriers travel between scattering events. Nanomaterials and nanostructures often feature characteristic length scales that are smaller than the mean free path, a situation where the classical heat diffusion theory is no longer applicable.

1.2.2 Thermal Interface Resistance

Thermal interface resistances are increasingly important as device dimensions scales down, and they can become the dominant contributor of the overall thermal resistance of nanostructured devices [19-21]. The thermal interface resistance between solids, R_b, is defined as

$$R_b = \frac{\Delta T}{q''} \tag{4}$$

where ΔT is the temperature drop across the interface. The term "interface" in this thesis is a broad concept and covers a variety of interfaces. One of the most common

interfaces is the material boundary which is formed by putting two media into contact, as shown in Figure 2(a). Electrons or phonons must travel from one material, across the interface, and into the other side in order for the heat to flow. Energy exchange between heat carriers is required if the dominant carriers are different in the two adjacent media, which introduces an additional resistance to the heat flow [14, 22-24]. Another type of interface involves the boundary between different crystalline phases, which occurs in some phase change materials (Figure 2(b)). For example, $Ge_2Sb_2Te_5$ film can have a mixture of crystalline and amorphous phases under certain annealing conditions [25, 26]. If the crystalline grains are preferentially oriented in the out-of-plane direction, the phonons traveling in the in-plane direction scatter more frequently at the grain boundaries. The inhomogeneity of the material structure can cause anisotropic thermal conductivities along the two directions. A third type of interface studied in this work is, in fact, an interfacial layer connection two functional materials. One example is the GaN high electron mobility transistor (HEMT) with diamond substrate [27, 28]. The high thermal conductivity of diamond makes it attractive for cooling of HEMT devices. However, an adhesion layer is required between the diamond substrate and the GaN due to the fabrication process. Figure 2(c) shows the transmission electron microscope (TEM) image of region near the GaN-diamond interface. Measuring the thermal resistance associated with the thin layers of disordered adhesive material helps improve the effectiveness of the thermal management for the HEMT devices. For clarity of discussion, this dissertation uses the term “thermal boundary resistance (TBR)” for the first two types of interfaces where the two functional materials are in direct contact, and uses the term “effective thermal interface resistance” to denote the third type of interface where another thin adhesion layer is involved.

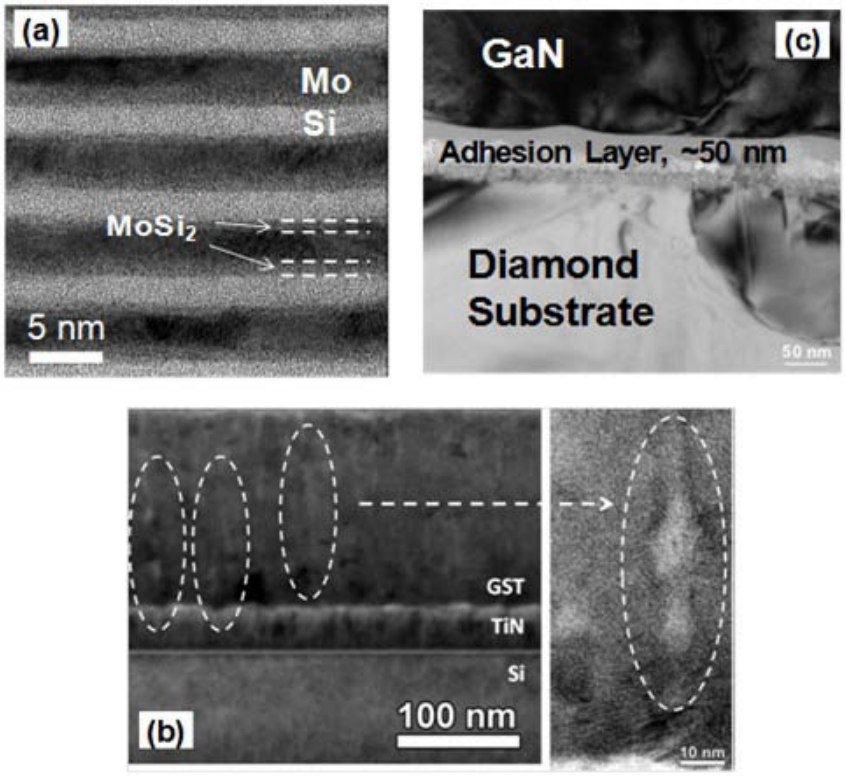


Figure 2. Transmission electron microscope (TEM) images of the three types of interfaces studied in this work. (a) Material boundaries: interfaces between alternating Mo and Si thin films which are used as extreme ultraviolet mirrors [21]. (b) Phase boundaries: interfaces between the crystalline and amorphous regions in a $Ge_2Sb_2Te_5$ thin film for phase change memory [25]. (c) Interfacial material layer: disordered adhesion layer between GaN and diamond substrate for high electron mobility transistors.

Several theories on the physics of TBR have been developed in the past several decades. The diffuse mismatch model (DMM) is commonly used to evaluate the thermal conductance due to phonon-phonon coupling across an interface [17, 29-31]. The DMM assumes diffusive phonon reflection at interfaces, which is typically valid at the room temperature where the phonon wavelength is shorter than the interface roughness. Assuming the temperature drop across the interface is small, the thermal interface conductance is [31]

$$h_{pp,1\text{-}2} = \left(\frac{\alpha_{1-2}}{12} v_{1,D}^3 \sum_j v_{1,j}^{-2} \right) C_{1,v}(T), \tag{5}$$

where $C_v(T)$ is volumetric heat capacity at T, and v is the speed of sound with its subscript j denoting the polarization (l for longitudinal and t for transverse). The phonon transmission coefficient [17, 31] from Material 1 to Material 2, $\alpha_{1\text{-}2}$, can be written as

$$\alpha_{1-2} = \frac{\sum_j v_{2,j}^{-2}}{\sum_j v_{1,j}^{-2} + \sum_j v_{2,j}^{-2}}, \tag{6}$$

and v_D is the speed of sound calculated using the Debye model:

$$v_D = \left(v_l^{-3} + 2v_t^{-3} \right)^{-1/3}. \tag{7}$$

The DMM estimate can lead to substantial deviations in the thermal interface conductance near room temperature because the Debye approximation does not properly account for the complexity of the phonon dispersion relationships at the edge of the Brillouin zone [30, 32]. Depending on the material combination and temperature, Reddy *et al.* [30] reported as large as 100 percent difference between the Debye model and a numerical computation considering the full dispersion relationship over the entire Brillouin zone. There is some evidence that the presence of at least one amorphous material can mitigate the error due to the strong scattering of short wavelength phonons – for which dispersion is most important – in the amorphous material [29, 33]. The determination of the error is further complicated by the polycrystalline structure of molybdenum on the opposite side, which may render the use of an average, isotropic dispersion relationship more appropriate. For these reasons, Chapter 5 of the present work models the phonon transport across a metal-amorphous semiconductor interfaces using the DMM with Debye approximation. Further research on the crystalline-amorphous interfaces considering the full dispersion relationship on one side and strong scattering on the other would be useful in refining the modeling developed in the present work.

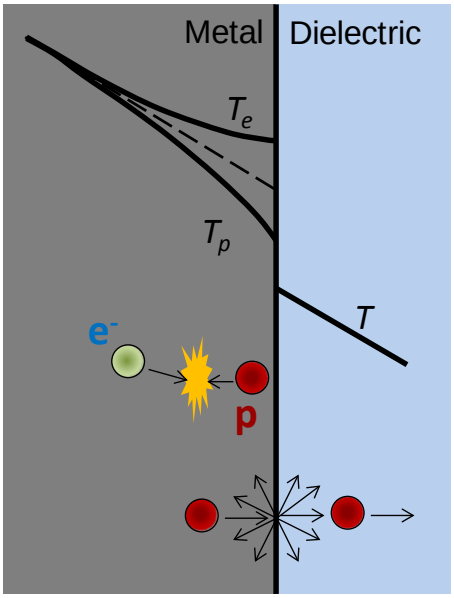


Figure 3. Illustration of the two-temperature model (TTM). Temperatures of the electron system (T_e) and the phonon system (T_p) in the metal side deviates from each other near the metal-dielectric interface. Thermal energy carried by the electrons must first be transferred to the phonons in the metal layer before being carried to the dielectric side by the phonons.

The DMM only models the phonon transport across a material interface. However, metal-dielectric or metal-semiconductor interfaces are common in a variety of nanodevices [21, 32, 34-36]. Since the electron concentration in dielectrics and most semiconductors is negligible, for thermal transport across the interface, electrons in the metal need to transfer their energy into the phonon system in the metal before the phonons can carry the heat across the metal-dielectric or metal-semiconductor interface (Figure 3). This electron-phonon nonequilibrium can be modeled by the two-temperature model (TTM) [22, 24, 37]. The TTM states that the electron temperature and phonon temperature deviate from each other near the metal-dielectric interface where the electrons and phonon are not in equilibrium. It extends the heat diffusion equation with an electron-phonon interaction term:

$$k_e \frac{\partial^2 T_e}{\partial z^2} - G\left(T_e - T_p\right) = 0; \quad k_p \frac{\partial^2 T_p}{\partial z^2} + G\left(T_e - T_p\right) = 0, \tag{8}$$

where the subscript e and p denotes electrons and phonons, respectively. The parameter G is an electron-phonon coupling factor which describes the rate of energy exchange between the electron system and the phonon system in the metal. Assuming the metal film is thick enough such that the T_e and T_p converge at locations far away from the interface (see Figure 3), the additional thermal resistance due to the electron-phonon nonequilibrium process, R_{ep}, can be derived as [22]

$$R_{ep} = \frac{1}{\sqrt{G k_{p,metal}}} \tag{9}$$

where $k_{p,\text{metal}}$ is the phonon contribution of the thermal conductivity of the metal. Chapter 5 provides detailed discussion of the TTM in the context of the heat conduction through Mo/Si multilayers.

For a metal-dielectric interface, the electrons may also exchange energy with the phonon system in the dielectric by scattering inelastically at the interface. Although ignored in some of the previous work on ultrathin metal/dielectric multilayers [32, 34, 35], the inelastic electron-interface scattering may be significant if the metal film thickness is close to or less than the electron mean free path [37-39]. Past research has used the inelastic phonon radiation limit theory [40], the maximum transmission model [41], the anharmonic inelastic model [42], and a quasi-analytical approach combined with experimental data [43, 44] to quantify the inelastic thermal conductance. The modeling work presented in Chapter 5 considers this inelastic scattering effect and discusses its relative strength and impact on the overall thermal resistance of a metal/dielectric multilayer.

1.3 Electrical Techniques for Thermal Measurement

Thermal characterization techniques are essential to better understanding of thermal phenomena at the nanoscale. Thin film materials play an important role in advanced nanodevices owing to their unique mechanical, thermal, and electrical

properties. Nanostructured materials usually exhibit reduced thermal conductivities as compared to bulk materials because of more frequent scattering of energy carriers at material interfaces, material impurities, grain boundaries, and lattice defects. The film geometry, grain structures, and phase impurities can also render the thermal conductivity of thin films anisotropic, meaning that the thermal conductivity in the in-plane direction is different from the out-of-plane value [25, 26]. The thermal boundary resistance (TBR) has been shown to be a significant, sometimes the dominant, contributor to the overall thermal resistance of nanostructures [20]. One experimental challenge is to accurately measure the anisotropic thermal properties of the nanometer-scale thin films and separating out the effect of TBR. This work develops a set of electrical thermometry techniques, useful for measuring the thermal conductivity anisotropy, and makes progress towards improving the thermal metrology for nanostructured materials and interfaces.

1.3.1 The 3ω Technique

One widely used electrical thermometry method for characterizing thermal conductivity is the 3ω technique, which was first introduced by Cahill and colleagues [45, 46]. This method uses the harmonic Joule heating of a microfabricated metal bridge to extract the thermal properties of the underlying materials. The schematic of a typical 3ω sample is shown in Figure 4(a). The metal bridge is usually fabricated with widths ranging from tens of micrometers to tens of nanometers, depending on specific applications and lithography resolution. The four-probe configuration facilitates accurate resistance measurement because it minimizes the impact of electrical contract resistance between the contact pads and the probe tip. The film of interest, typically with thickness from tens of nanometers to a few micrometers in this work, is deposited on top of a substrate. Depending on the electrical conductivity of the thin film, passivation layers may be required on the top and bottom of the thin film to avoid electrical leakage.

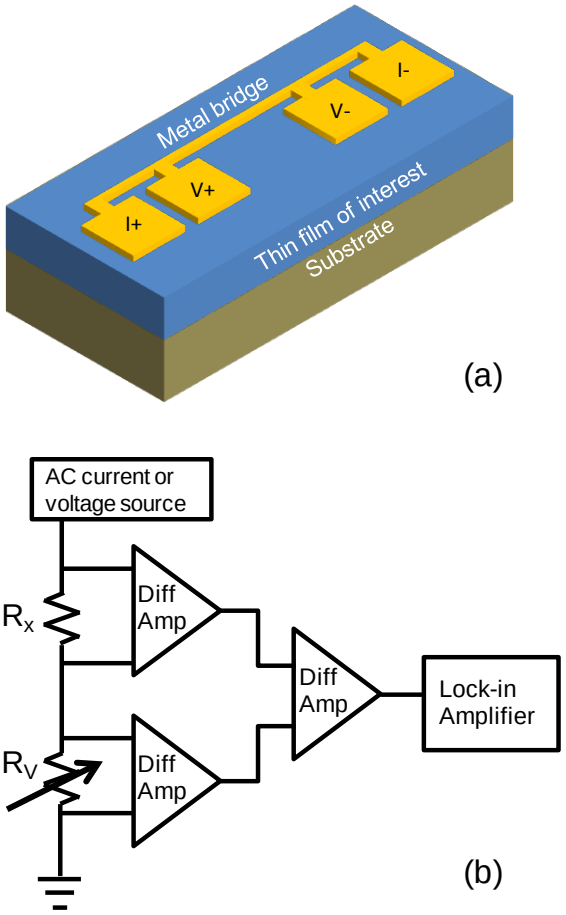


Figure 4. Schematic of a typical setup for 3ω measurements. (a) schematic of a sample structure. Metal bridges with a 4-probe configuration are fabricated on top of the thin film. Passivation layers (not shown) may be necessary between the metal pattern and the thin film, as well as between the thin film and the substrate. (b) a typical measurement circuit using differential amplifiers. The sample and a variable resistor are denoted as R_x and R_v, respectively.

Figure 4 (b) shows the schematic of a typical circuit for 3ω measurement. A current source generates an ac current at frequency ω that runs through the metal bridge on the sample and a variable resistor connected in series. Joule heating within the metal bridge induces the temperature of the metal heater bridge to oscillate at frequency 2ω. The variable resistor is selected to have a much lower temperature

coefficient of resistivity (TCR), so that most of the resistance change is contributed by the metal bridge. The change in resistance is captured by monitoring the voltage drop across the sample (R_x) and the variable resistor (R_v) by differential amplifiers. Due to the linear relationship between temperature and the electrical resistivity of the metal bridge, the measured voltage contains a smaller, third harmonic (3ω) component in addition to the larger, fundamental (ω) component. The variable resistor is fine tuned to the same resistance as the metal bridge, so that the voltage oscillation at ω can be cancelled out by a third differential amplifier. A lock-in amplifier captures the amplitude and phase information of the remaining 3ω signal, which are functions of the thermal properties of the underlying layer. Chapter 2 presents the detailed experimental procedure and data reduction method used in this work.

The 3ω technique has been further developed over the past decade to extend its capability in thermal characterization of complex thin film systems. D. Cahill and colleagues [45, 46] in their original 3ω experiment measured the thermal conductivities of bulk materials including SiO_2, Pyrex, nitrate glass, and PMMA. T. Yamane *et al.* [47] used a used a Wheatstone bridge-based 3ω circuit to measure the thermal conductivity of SiO_2 films deposited by different processes with thickness from a few tens of nanometers to 1 μm. B. Olson *et al.* [48] developed an data reduction method to extend the 3ω method for multilayer structures. In addition to the focus on the 3ω component, C. Dames *et al.* [41] showed the usefulness of the other two components (1ω and 2ω) in extracting the thermal properties and improved the flexibility of the 3ω technique. Many thin film materials have been characterized by the 3ω technique for a variety of applications: D. Borca-Tasciuc *et al.* [49] measured the specific heat and thermal conductivity of multi-wall carbon nanotube (CNT) strands, D.-W. Oh *et al.* [50] applied the 3ω technique to aluminum oxide nanofluids, and more recently W. Risk *et al.* and R. Fallica *et al.* [51-53] studied the thermal properties of the phase change chalcogenide $Ge_2Sb_2Te_5$ for memory applications.

The metrology techniques developed in this work further advance the 3ω measurement, by suspending the thin film [25, 26] and developing nanoscale heater bridges with varying width, in order to characterize two-dimensional thermal

characterization [21]. Chapter 2 and Chapter 5 provide detailed discussions on these measurements.

1.3.2 Steady-State Joule Heating Thermometry

Many modern nanodevices usually contain thin films of different materials stacked together to form a multilayer structure. The thermal properties of each constituent film, which are located at different depth below the top surface, are important in engineering the thermal performance of the nanodevice. Frequency-domain thermometry such as the 3ω technique can probe different depths into the underlying layers by varying the frequency of the driving current. On the other hand, heat confinement can also be achieved by steady-state Joule heating by varying the width of the heaters. This spatial heat confinement provides a convenient way to probe thermal properties at different depths within a film, as well as to characterize the thermal resistance of the entire multilayer structure for a range of length scales.

The schematic of the dc Joule heating measurement sample is shown in Figure 5. When dc electrical current runs through the metal heat bridge, the temperature rises due to the Joule heating. Because the electrical conductivity of the metal typically decreases linearly with temperature for the temperature range of this work, the electrical resistance of the heater bridge changes with temperature as

$$R(T) = R_0 \left(1 + \alpha \Delta T\right) \tag{10}$$

where $R(T)$ and R_0 are the electrical resistances of the heater bridge at temperature T and at a reference temperature. The temperature coefficient of resistivity (TCR) α is a material property and considered constant, and ΔT denotes the temperature rise from the reference temperature. By measuring the electrical resistance change of the metal heater bridge, one can derive the temperature rise of the heater bridge with Eq. (10). The thermal resistance R_{th} that this heater experiences is by definition:

$$R_{th} = \frac{\Delta T}{Q}, \tag{11}$$

where Q is the amount of Joule heating power that was dissipated through the multilayer stack. For small temperature rises, it is safe to ignore the convective and radiative heat loss at the top surface and assume that all the Joule heating power goes into the multilayer structure.

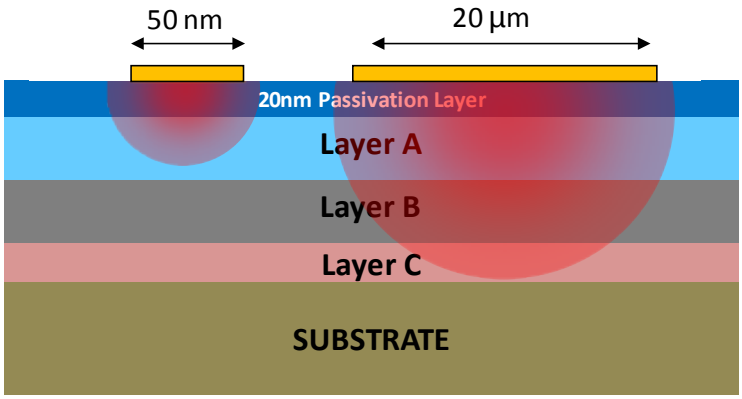


Figure 5. Schematic of a multilayer structure and heater bridges with varying widths. Narrow heaters confine the heat within a shallow region below the surface, and their temperature rise is not sensitive to the thermal properties of the layers further below. The heat generated from the wide heaters probes deeper into the multilayer stack. Schematic is not drawn to scale.

Heaters with varying widths probe into different regions of the underlying layers by means of spatial heat confinement. Heat generated from narrow heaters (compared to the layer thickness) sees the underlying structure as a semi-infinite medium, and most of the temperature drop is confined within a small region underneath the narrow heater. This spatial heat confinement provides a way to measure the thermal conductivity of the very thin layers near the top because the temperature rise of the heater is highly sensitive to the thermal properties of the material in this shallow region, and less sensitive to the materials further down (for example, the substrate). The narrow heaters are also useful in measuring the in-plane thermal conductivity because of the significant two-dimensional heat spreading from the heater line. Wider heaters, on the other hand, generate almost one-dimensional heat flow through the top

layers of the sample and, thus, are less sensitive to the in-plane thermal conductivity of this shallow region. The heat generated from the wider heaters can penetrate deep into the multilayer stack, and the temperature drop from the layers to the substrate can be significant. Therefore, the temperature rise of the wide heaters is more sensitive to the thermal properties of the layers near the bottom and the TBR at each interface.

The steady-state Joule heating thermometry has been widely used to for thermal characterization of thin-film materials and other nanostructured devices. W. Liu *et al.* measured the thermal properties of single-crystal silicon-on-insulator (SOI) layers down to approximately 20 nm [54]. P. Kim *et al.* observed a thermal conductivity of more than 3000 W/mK of individual multiwall carbon nanotubes by fitting the steady-state Joule heat data to a theoretical model [55]. E. Pop *et al.* applied dc DC Joule heating power to a single wall carbon nanotube with a diameter of 1.7 nm and measured a thermal conductivity of nearly 3500 W/mK [56, 57]. More recently, S. LeBlanc *et al.* measured the thermal conductivity of zinc oxide nanowires for energy conversion applications [58], and A. Marconnet *et al.* studied periodically porous silicon nanobridge for photonic applications using a similar steady-state Joule heating approach [59].

Furthermore, the steady-state Joule heating thermometry provides a convenient way to study the thermal resistance of nanostructured electronic devices at different length scales. Modern nanodevices often feature a hierarchy of characteristic length scales. For example, a high electron mobility transistor (HEMT) usually consists of local hotspots in the individual channels with dimensions of approximately 1 μm, a multigate array with dimensions of 10-100 μm, and the device package level of above 1000 μm. Effective thermal management requires knowledge of the thermal resistances that are experienced by these different length scales, as well as the dominating factor that contributes to the overall thermal resistance. Heater bridges with varying widths can accurately measure the thermal resistances for different length scales and, in conjunction with thermal modeling, identify the specific layers or TBRs that are critical to the temperature rise of the nanodevice. Chapter 3 describes the

detailed steady-state Joule heating measurement and modeling approach in the context of HEMT applications.

1.3.3 Suspended Structures for In-Plane Measurements

The thermal conduction in the in-plane direction has been of increasing interest over the past decade. Measurement of the heat conduction in the in-plane direction is important for a variety of microdevices with lateral structures. For example, M. Lankhorst *et al.* fabricated a low-current phase change memory (PCM) device with a $Ge_2Sb_2Te_5$ bridge connecting the two electrodes laterally [60], and Y. Yin *et al.* developed a TiN/SbTeN double layer in the in-plane direction to achieve multibit programming in PCM [61, 62]. The few-layer graphene heat spreader, developed by Z. Yan *et al.* [63], effectively removes heat from localized hot spots in high-power GaN transistors and redistributes it laterally to the nearby heat sinks. Thermal properties of the relevant compounds and thin films can exhibit strong anisotropy, and accurate in-plane thermal characterization is important in the successful design of these nanodevices.

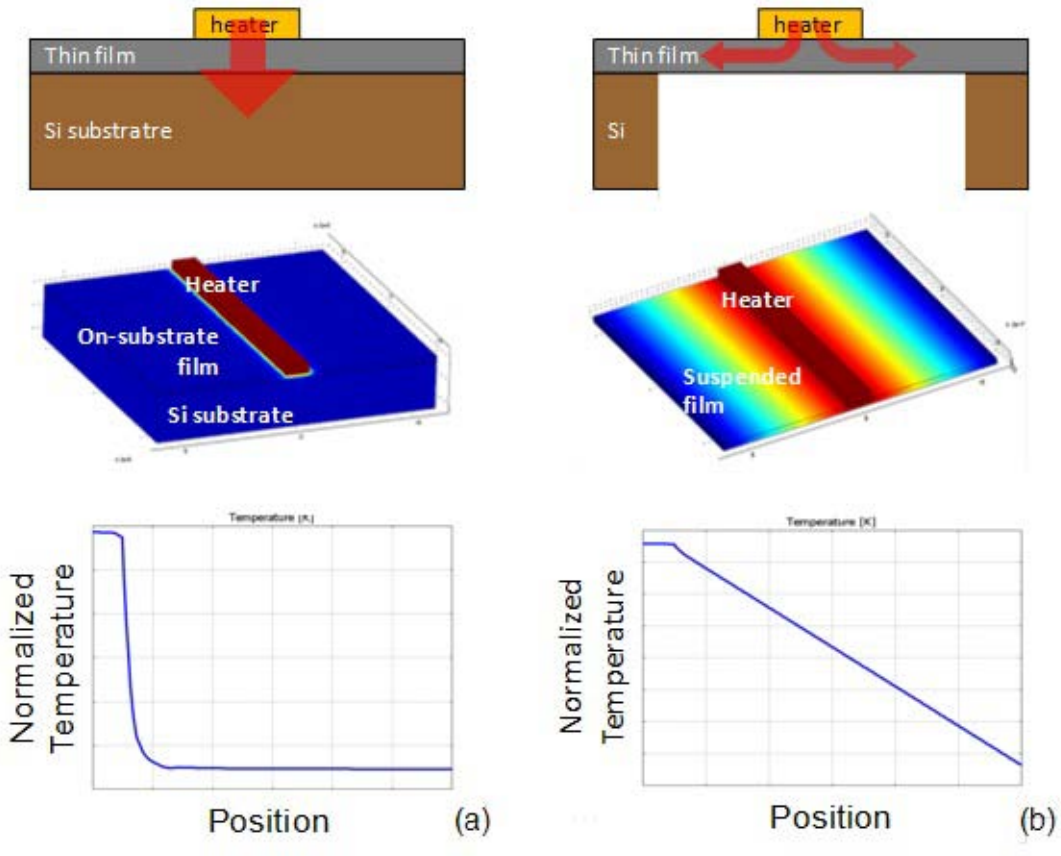


Figure 6. Temperature distribution of on-substrate and suspended structures. Top: schematics of the sample structures. Middle: numerical simulation of the temperature distributions. Bottom: temperature profile at the top surface in the lateral direction from the center of the heater to the edge of the sample (heat sink). (a) On-substrate structures usually show limited sensitivity to the in-plane conduction when the heater is much wider than the thickness of the thin film. (b) Suspended structures force all the heat to dissipate laterally and are therefore highly sensitive to the in-plane thermal conductivity of the thin film.

Conventional on-substrate structures for thermal characterization typically feature a metal heater to generate heating power, a thin film or multilayer of interest, and a silicon substrate. The high thermal conductivity of silicon makes it an effective heat sink drawing most of the heat vertically through the thin film as shown in Figure 6. This effect is most significant when the film thickness is much smaller than the heater

width, which is usually limited by the photolithography resolution (~1 μm). The suspended structure, on the other hand, can force the heat generated from the metal heater to dissipate laterally along the thin film before reaching the heat sinks at the edge. The temperature profile, which is nearly linear assuming convection and radiation heat loss can be neglected, is highly sensitive to the in-plane thermal conductivity and can be accurately measured by metal bridges deposited on the suspended thin film [64] or by Raman thermometry [65]. A frequency-domain measurement with the suspended structure can also resolve the thermal diffusivity and heat capacity of the thin film material [66].

Many variations of the suspended structures have been developed to characterize the thermal properties of a variety of nanomaterials and nanostructures. X. Zhang *et al.* measured the thermal conductivity and thermal diffusivity of silicon nitride film of 0.6 μm and 1.4 μm using the electrical thermometry with the suspended structure. W. Cai *et al.* [65] and A. Balandin *et al.* [67] fabricated single suspended layers of graphene and measured their in-plane thermal conductivity to be around 2000–5000 W/mK. The concept of suspended structures is also applicable to the thermal characterization of other non-planar nanostructures. Recent research has fabricated and measured the thermal conductivities of the free-standing structures including carbon nanotubes [56, 57, 68], zinc oxide, nickel, and silicon nanowires [58, 69-71], and DNA strands [72]. The design and fabrication of suspended structures to measure the in-plane thermal conductivity and heat capacity of $Ge_2Sb_2Te_5$ thin films are discussed in Chapter 2.

1.4 Thesis Overview

This work addresses thermal transport phenomena in nanostructured materials and devices. In particular, this work develops a set of electrothermal characterization techniques and theoretical modeling approaches and applies them to three nanodevices and nanostructures: phase change memory (PCM), gallium nitride high electron

mobility transistors (HEMT), and molybdenum/silicon multilayers for extreme ultraviolet (EUV) mirrors.

Chapter 2 starts with the measurements of in- and out-of-plane thermal conductivities of $Ge_2Sb_2Te_5$ thin films for PCM. The work presents the detailed experimental design and methodology of the 3ω technique and suspended measurement structures. Grain structure characterization of the $Ge_2Sb_2Te_5$ film facilitates the understanding and modeling of the thermal conductivity anisotropy in the thin film. Coupled electrothermal simulations predict the impact of the anisotropic thermal conduction on the performance of PCM devices.

The discussion of PCM continues in Chapter 3 which focuses on multibit programming capability. A set of coupled electrical, thermal, and phase transitional models describes the crystallization process in the nanodevice under transient electrothermal conditions. The simulations evaluate two standard PCM structures, the mushroom cell and the confined pillar cell, with feature sizes smaller than 40 nm. This work also explores a more compact architecture, the stacked vertical cell, with precise control of the Joule heating and potentially more stable intermediate resistance levels.

Chapter 4 is devoted to the discussion of thermal phenomena in HEMT devices. This work starts by reviewing the recent thermal data of the relevant materials and interfaces for GaN-based HEMT devices. Steady-state Joule heating thermometry, with nanoheaters with widths down to 50 nm, measures the thermal conductivity of the constituent materials of a HEMT structure with a diamond substrate for improved thermal management. A numerical code calculates the temperature rise of the multilayer structure and reveals the individual contribution of different layers to the overall thermal resistance at three distinct characteristic length scales: the single gate hot spot, the multigate array, and the device package.

Chapter 5 applies the 3ω technique with the nanoheaters with varying widths to measure the anisotropic thermal conductivity of Mo/Si multilayers for EUV lithography applications. This chapter also develops a theoretical model for the phonon-electron energy conversion at and near the metal/semiconductor interfaces.

This work introduces a criterion for the transition from electron to phonon dominated heat conduction in metal films bounded by dielectrics.

Chapter 6 concludes the dissertation by summarizing the major contributions of this work and suggesting future work which extends the understanding of heat transfer in nanomaterials and nanodevices.

Chapter 2: Anisotropic Thermal Conduction in Phase Change Memory

2.1 Introduction

Phase change memory (PCM) is becoming promising for next-generation nonvolatile memory applications due to its high read/write speeds, improved reliability and superior scalability [1, 3]. PCM stores information by exploiting the difference in electrical resistivity between crystalline and amorphous phases of the phase change material. The reversible phase transformations are induced through intense local Joule heating caused by electrical current pulses.

Phase change chalcogenide $Ge_2Sb_2Te_5$ (GST) and related compounds are among the most widely used materials for PCM. The thermal properties of GST govern the performance of PCM devices in terms of programming current, write speed and reliability [3, 73]. While several recent studies on the thermal conductivity normal to GST films have been reported [51, 52, 73-76], little attention has been given to the in-plane thermal conductivity of GST thin films or conductivity anisotropy. In-plane thermal conduction of GST not only governs the performance of lateral PCM cells [60, 62, 77], but also determines the thermal cross-talk effect of the conventional vertical PCM designs [78, 79]. The thermal conductivity anisotropy of GST films has been measured previously using multiple metal heater bridges of varying width [80], but this technique does not involve the direct measurement of the in-plane thermal conductivity. Asheghi *et al.* developed a suspended structure to measure the in-plane thermal conductivity of 3 μm thick polysilicon film [81]. However, lateral thermal measurements for thin films with sub-micrometer thickness and materials with low thermal conductivity such as GST (~1 W/mK) are still not available. We extends the characterization technique described in [81] to the measurements of materials with low thermal conductivity by using a differential method. This work focuses specifically on the in-plane thermal conductivity measurement and investigates the anisotropy in thermal conductivity of GST thin films using micromachined suspended structures.

2.2 Thermal Conductivity Measurement of $Ge_2Sb_2Te_5$ Films

2.2.1 Experimental Structure Design and Fabrication

Figure 7(a) shows the cross-sectional schematic of the experimental structure. A SiO_2 layer provides mechanical support to the suspended GST thin film, and a thin Si_3N_4 capping layer passivates and protects the top surface of GST. The suspended SiO_2-GST-Si_3N_4 stack is highly sensitivity to in-plane heat conduction due to the absence of a silicon substrate which serves as a heat sink in conventional on-substrate structures [81]. Figure 7(b) illustrates the top view of the experimental structure. A platinum heater located in the center of the suspended film provides heating power, and two platinum resistive thermometers measure the temperature rise at different locations (x_A and x_B) to determine the in-plane thermal conductivity. The platinum heater and thermometers extend over the entire suspended film; yet the generated heating power and local temperatures (T_A and T_B) are only captured within the central region (L) of the membrane using a four-point electrical measurement. The elongated shape of the suspended film creates one-dimensional lateral heat conduction along the x direction within the measurement region ($L \times L_2$) as verified by finite element simulation in Figure 7(c). The thermal resistance of conduction along the suspended film in the x direction is much smaller than that of all the other heat transfer paths; therefore, it is valid to assume that all the heat generated by the heater is dissipated laterally along the x-direction.

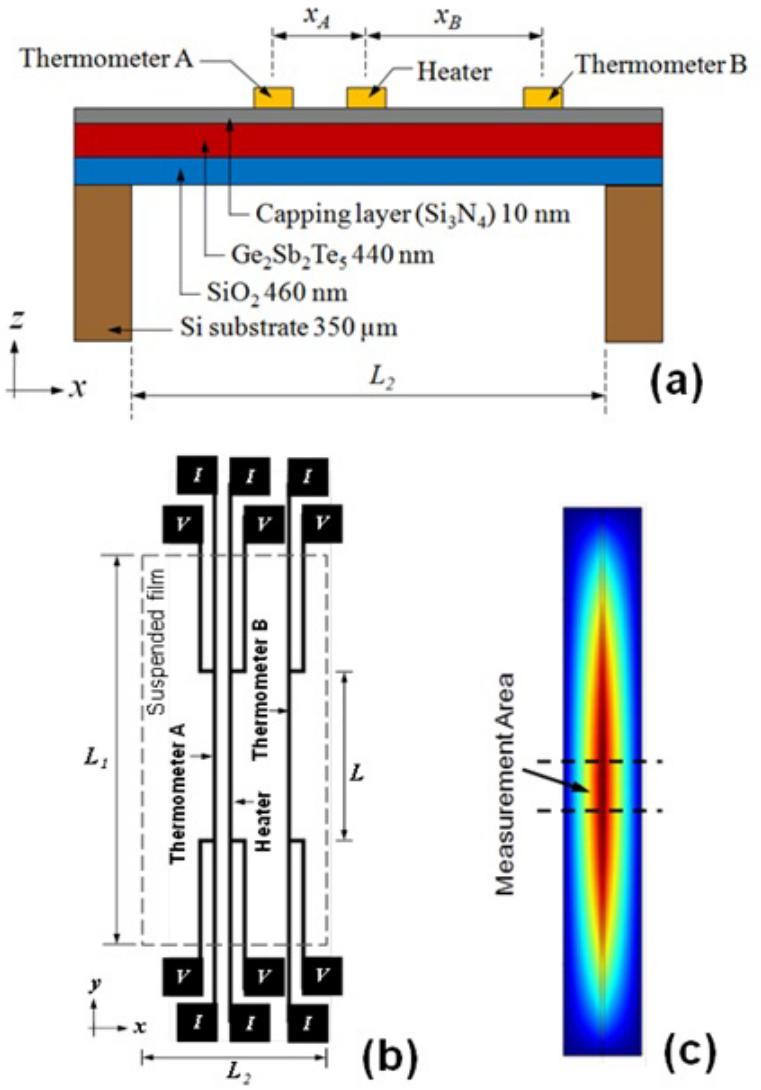


Figure 7. Schematic of the experimental structure with suspended GST thin film. (a) Cross-sectional view of the structure. The width of the heater and thermometers are 2 µm, and the distances x_A and x_B vary from 20 µm to 160 µm; (b) Top-view of the front side patterns. The example dimensions of the suspended film are L_1 = 3200 µm and L_2 = 400 µm. Measurement area is located in the center of the membrane with a length of L = 200 µm. (c) Finite-Element simulation of the temperature distribution of the suspended thin film. The 8:1 length-to-width ratio provides a one-dimensional temperature gradient in the x-direction. Figures are not drawn to scale.

The samples with suspended GST thin films are fabricated on double-side-polished silicon wafers. First, a 460 nm thick silicon oxide layer is thermally grown to offer passivation and mechanical support for the suspended structures. The GST layer of 440 nm is deposited on top of the thermal oxide by radio frequency magnetron sputtering at the amorphous phase (a-GST). A thin layer of silicon nitride is deposited on the top surface of GST to prevent it from being oxidized and to provide electrical isolation. A platinum layer of 50 nm is subsequently deposited and patterned using lift-off technique to form the 2 µm wide electrical heaters and resistive thermometers on the front side of the samples. The wafer is then coated with 7 µm SPR-220 photoresist and baked for 5 hours at 90 °C. This step provides protection to the structures on the front side and enhances the structural integrity during the subsequent deep reactive ion etching (DRIE). Backside photolithography creates access windows on the backside of the wafer, and an STS DRIE system etches the full thickness of the silicon wafer through these access windows, releasing the thin film stack on the front side. Finally, acetone removes the protective photoresist on the front side and completes the overall fabrication process.

The fabricated suspended structure is shown in Figure 8 (a). X-ray diffraction (XRD) confirms the phase transition from a-GST to face-centered cubic GST (f-GST) at around 110 °C and further to hexagonal close packed GST (h-GST) at about 200 °C for the identical material and deposition conditions [80]. Figure 8 (b) and (c) show a 7.0 % decrease in GST thickness from 440 nm to 409 nm as the GST transforms from a-GST to f-GST. This is due to the density difference between a-GST and h-GST. Reifenberg *et al.* [73], Pedersen *et al.* [82] and Weidenhof *et al.* [83] also reported similar thickness reduction upon crystallization. No further decrease in film thickness from f-GST to h-GST is observed given the resolution of the Scanning Electron Microscopy (SEM) which is approximately 3 nm.

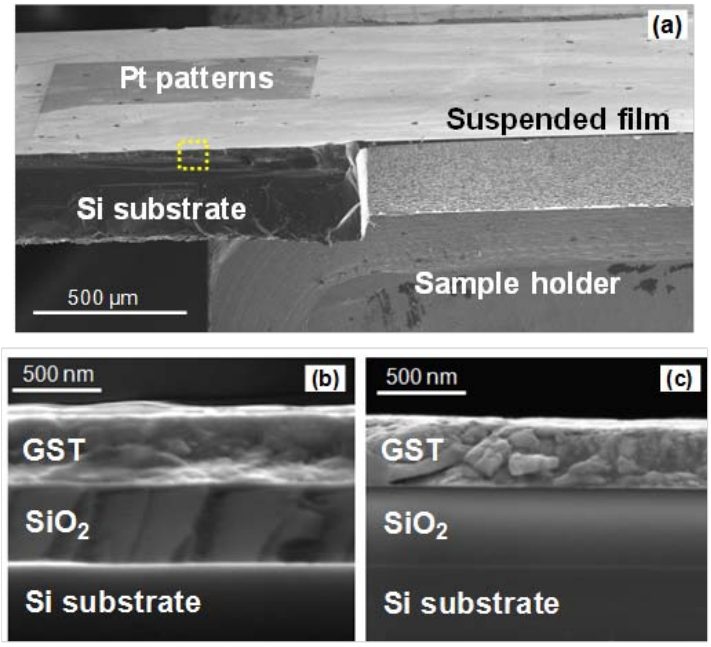


Figure 8. Scanning Electron Microscopy (SEM) images of the experimental structure with suspended thin film. (a) Part of the sample near one end of the suspended thin film; (b) Magnified image of the dotted region in (a) with as-deposited a-GST thickness of 440 nm; (c) Crystalline f-GST is obtained by annealing the sample at 150°C. The thickness of f-GST film is reduced to 409 nm due to the increase in density upon crystallization.

2.2.2 Measurement Techniques and Procedure

The in-plane thermal conductivity is measured using DC heating and resistive thermometry. A Keithley 6221 current source provides DC current to the platinum resistive heater which induces a linear temperature profile in the x direction along the suspended thin film. Platinum resistive thermometers measure the temperature rises at different locations over the extent of the measurement region L. Temperature-controlled calibration shows the temperature coefficient of resistance (TCR) for a 50 nm thick platinum thin film is 2.2×10^{-3} K^{-1} which is consistent with the previously

reported value [84]. A differential measurement is used to subtract the contributions of SiO_2 and Si_3N_4 layers by comparing the experimental samples to another set of reference samples which have identical structures but without a GST layer.

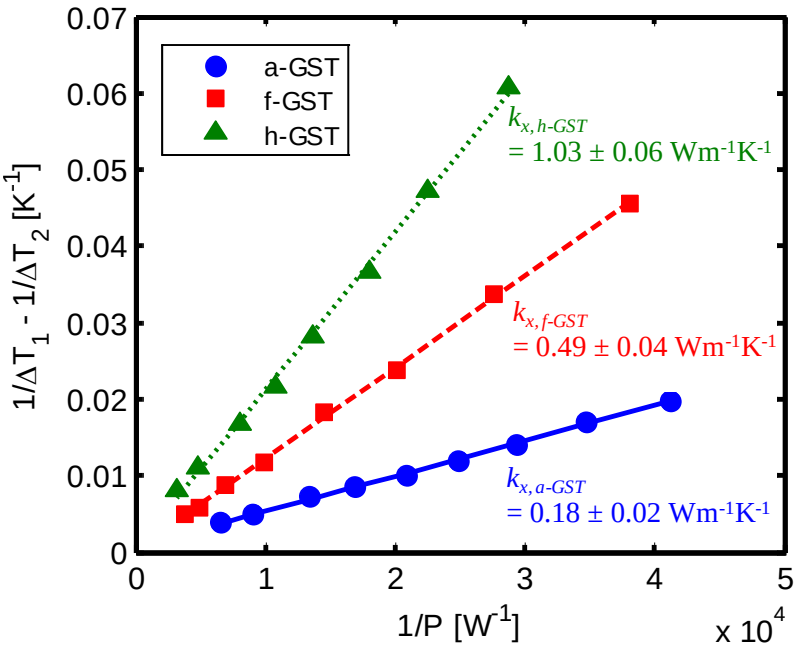


Figure 9. Data of the in-plane thermal conductivity measurement. The solid, long-dashed and short-dashed lines are the linear fit of a-GST, f-GST and h-GST, respectively. The slopes of these fitted straight lines give the values of in-plane thermal conductivities of the GST thin film at different phases. Uncertainty of each data point is less than 0.002 K^{-1}.

The in-plane thermal conductivity of the GST layer, $k_{x,GST}$, is extracted using

$$\frac{1}{\Delta T_1} - \frac{1}{\Delta T_2} = \left(\frac{2 d_{GST} k_{x,GST} L}{\Delta x} \right) \frac{1}{P} \tag{12}$$

where $\Delta T_1 = T_{A,1} - T_{B,1}$ is the difference in temperature rise measured by thermometers A and B on the samples with GST layers, whereas $\Delta T_2 = T_{A,2} - T_{B,2}$ is obtained from the

reference samples without GST. The quantity $\Delta x = x_B - x_A$ is the difference in distances of the two thermometers from the central heater as shown in Figure 7(a). Equation (12) indicates a linear relationship which is plotted in Figure 9. The slope of the linearly fitted line determines the value of $k_{x,GST}$.

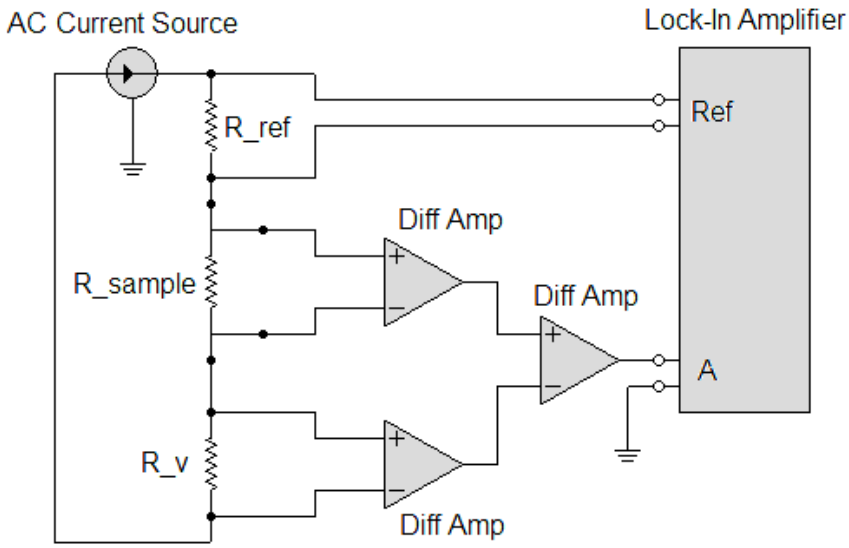


Figure 10. Electrical circuit for the 3ω measurement. R_sample is the resistance of the 3ω structure and R_v is a variable resistor with low thermal coefficient of resistivity (TCR). The amplitude and phase of the voltage signal at 3ω frequency is captured by a lock-in amplifier.

In order to capture the anisotropy in the thermal conductivity of the GST thin film, the out-of-plane thermal conductivity (k_z) is measured using the 3ω technique. The 3ω technique, which was first introduced by Cahill [45, 46], employs harmonic Joule heating of a heater/thermometer line to extract the thermal properties of the underlying materials. A driving AC current at frequency ω generates Joule heating and temperature oscillation at frequency 2ω. Due to the linear relationship between

temperature and the electrical resistivity of platinum over the temperature range where this experiment is carried out, the voltage measured across the platinum heater/thermometer contains a third harmonic (3ω) component which is a function of the thermal conductivity of the underlying layer. The experimental setup is shown schematically in Figure 10. The on-substrate 3ω samples for this measurement are fabricated on the same wafers as the suspended structures to maintain the identical multi-layer stack. The lateral heat spreading can be neglected because the heater width is much larger than the thickness of GST-SiO_2 stack. Therefore, this 3ω structure is only sensitive to the out-of-plane thermal conductivity.

2.2.3 Measurement Results of Anisotropic Thermal Conductivity

The measured in-plane thermal conductivities include 0.18 ± 0.02 $Wm^{-1}K^{-1}$ for as-deposited a-GST, 0.49 ± 0.04 $Wm^{-1}K^{-1}$ for f-GST annealed at 150 °C, and 1.03 ± 0.06 $Wm^{-1}K^{-1}$ for h-GST annealed at 260 °C. Temperature rise of the suspended film is kept below 13 °C during the experiment in an effort to minimize the heat loss due to radiation and convection. The relative uncertainties in film thickness d_{GST}, measurement area length L, and conducted heating power P are 2%, 2.5% and 1%, respectively. The most important source of uncertainty originates from the measured temperature rise which has approximately 5% uncertainty limited by the resistive thermometry.

Similar to the in-plane measurement, a differential method subtracts the heat conduction contributions from SiO_2, Si_3N_4 and the Si substrate, leaving only the effect of the GST film. The detailed theoretical derivation of the 3ω technique is discussed elsewhere [45, 46], and the effective out-of-plane thermal conductivity is deduced as

$$k_{z,GST} = \frac{Pd_{GST}}{WL\left[\Delta T_1(\omega) - \Delta T_2(\omega)\right]} \tag{13}$$

where $\Delta T_1(\omega)$ and $\Delta T_2(\omega)$ are the amplitudes of temperature oscillation for samples with and without GST layer, respectively. The resulting out-of-plane thermal

conductivities are 0.18 ± 0.04 $Wm^{-1}K^{-1}$ for a-GST, 0.61 ± 0.04 $Wm^{-1}K^{-1}$ for f-GST, and 1.25 ± 0.04 $Wm^{-1}K^{-1}$ for h-GST. The data agree with the reported value range for each material phase and film thickness [51, 52, 73, 81]. The major source of uncertainty stems from the temperature measurement using resistive thermometry which is approximately 5% of the nominal temperature. Thermal boundary resistance (TBR) also brings error in the measured out-of-plane thermal conductivity. The TBR of GST-SiO_2 and GST-Si_3N_4 interfaces are deduced as 2.2×10^{-8} $m^2K^{-1}W^{-1}$ and 4.3×10^{-8} $m^2K^{-1}W^{-1}$, respectively, from a previous study with samples of identical material and fabrication process [25]. Such TBR results in approximately 4% underestimation of the measured out-of-plane thermal conductivity.

Figure 11 summarizes the measurement results of the thermal conductivities of GST thin films in both in-plane and out-of-plane directions as a function of temperature. The abrupt increase in thermal conductivity between 110-120 °C corresponds to the phase transition from a-GST to f-GST as confirmed by XRD analysis. No significant difference in thermal conductivity between the two directions is observed for the amorphous phase, and the thermal conductivities remain constant at 0.18 $Wm^{-1}K^{-1}$ up to 80°C. This indicates isotropic heat conduction in a-GST films. In the fcc phase, the thermal conductivity grows gradually with temperature, and the out-of-plane thermal conductivity exceeds the in-plane value. This anisotropic heat conduction begins to appear after a- to f-GST phase transition and the ratio of the thermal conductivities in two directions is roughly constant. This anisotropy is discussed in more detail in the following section.

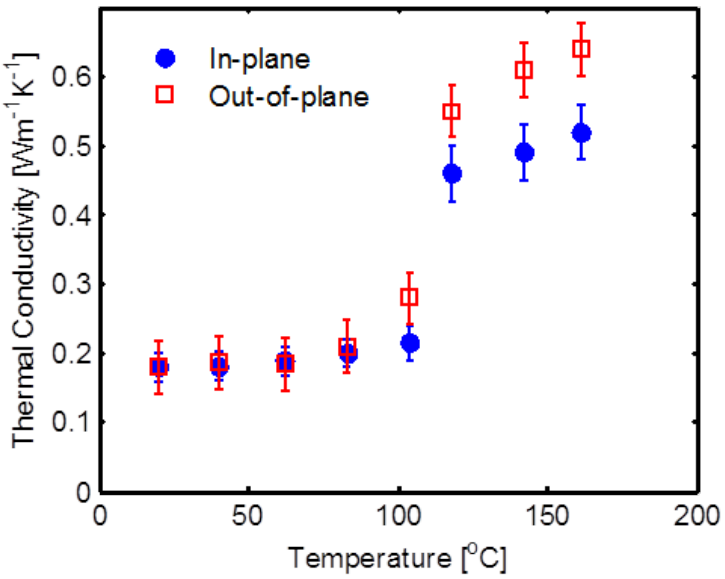


Figure 11. Temperature-dependent in-plane and out-of-plane thermal conductivities of the GST thin film. Thermal conductivity anisotropy begins to appear at the transition from a-GST to f-GST.

Varying the duration of annealing achieves different levels of crystallization. Our measured in- and out-of-plane thermal conductivities change with annealing duration as shown in Figure 12, indicating that the phase impurity affects the effective thermal conductivity of GST thin films. The overall volume fraction of the crystalline phase, p_c, depends on the annealing temperature and duration. For an isothermal phase transformation, p_c can be predicted using the Johnson-Mehl-Avrami-Kolmogrov (JMAK) equation [85],

$$p_c = 1 - \exp\left(-Kt^m\right) \tag{14}$$

where t is annealing time, m is the Avrami exponent, and K is a rate constant. The Avrami exponent, which depends on the type of nucleation and the crystal growth morphology, is set to 2 for the GST films assuming interface-controlled one-dimensional growth nucleation at a constant rate [86]. The rate constant is determined

from the best fit to the data. The amorphous GST film has an isotropic thermal conductivity. In-plane and out-of-plane thermal conductivities deviate from each other during the GST crystallization process. Because an annealing duration of more than 60 minutes at 110 °C completely crystallizes the GST film, the thermal conductivity anisotropy disappears. The next section presents a way to describe the anisotropic grain formation, which, when combined with the JMAK equation, models the thermal conductivity anisotropy in the GST films.

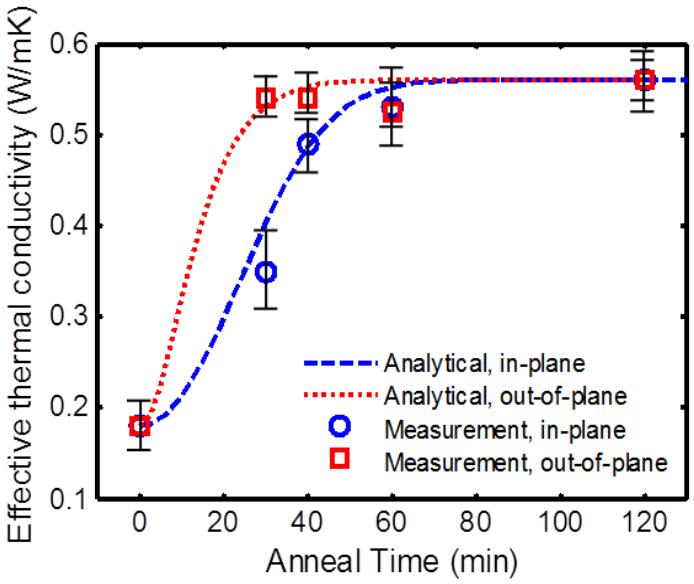


Figure 12. Data for the in-plane and out-of-plane thermal conductivities of GST films, summarized here based on a full-length article [6], and compared with the model developed in this work. The amorphous GST was annealed at 150 °C for each time duration.

2.2.4 Heat Capacity Measurement of the GST Thin Film

Another important thermal property of the GST thin film, the heat capacity, is also measured by the suspended structure. The measurement employs AC Joule heating of the central heater and one-dimensional heat conduction along the suspended GST film.

The AC current provides periodic heating whose frequency induces a semi-infinite heat conduction boundary condition in the in-plane direction, and the phase of the transient temperature response contains the information about heat capacity of the GST thin film. The measured heat capacity of GST thin film is 1.25×10^{6} - 1.29×10^{6} $JK^{-1}m^{-3}$ and does not show strong dependence of temperature from 20 °C to 160 °C as shown in Figure 13.

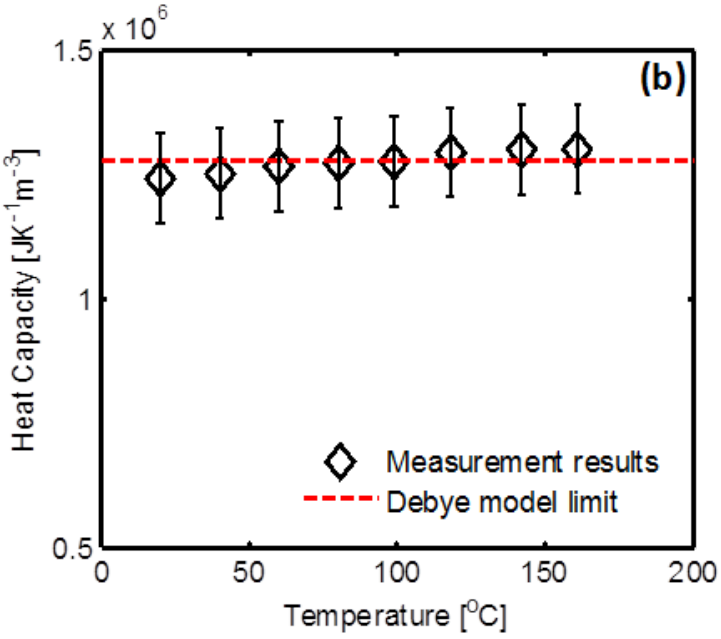


Figure 13. Heat capacity measured by the suspended structure and the theoretical limit calculated by Debye model for heat capacity.

The theoretical value of heat capacity of GST film is estimated based on the Debye model,

$$C = 9nk_B\left(\frac{T}{T_D}\right)^3\int_0^{T_D/T}\frac{x^4e^x}{\left(e^x-1\right)^2}dx \qquad (15)$$

where C is the volumetric heat capacity. The atomic number density n of GST is reported as 3.09×10^{22} cm^{-3} through Rutherford backscattering spectrometry [52], and

the Debye temperature of GST, T_D, is around 100K [87]. This study resides in the high temperature limit ($T >> T_D$) where the heat capacity can be simplified as

$$C \approx 3nk_B \tag{16}$$

Equation (16) estimates the theoretical heat capacity of GST as 1.28×10^6 $JK^{-1}m^{-3}$ which is in good agreement with the measurement results over the temperature range of this study. However, the Debye model does not include electrons' contribution to heat capacity for crystalline phases, and, thus, the calculated heat capacity at high temperature limit is underestimated.

2.3 Grain Structure and Anisotropy Analysis

2.3.1 Thermal Conductivity Anisotropy

The anisotropy ratio in thermal conductivity of GST thin film is defined as

$$\eta = \frac{k_x}{k_z} \tag{17}$$

where k_x and k_z are the in-plane thermal conductivity in the x direction and out-of-plane thermal conductivity in the z direction as depicted in Figure 7, respectively. We observe an anisotropy ratio of 0.6-0.8 for crystalline GST thin films whereas films in the amorphous phase show isotropic thermal conductivity. Possible sources of the thermal conductivity anisotropy include partial preferential orientation of grains in the polycrystalline GST thin films. The internal scattering of phonons overwhelms the film-boundary scattering. Grain boundaries, lattice imperfections and impurities can result in increased internal phonon scattering and reduced phonon mean free path in polycrystalline films. However, there is no available theory rigorously models the anisotropic effect and the impact on device performance has not been assessed. Electrical conduction modeling is expected to be similar to thermal conduction given the grain structure and phase composition of GST thin films [88]. Understanding the

impact of anisotropic thermal conduction is essential for improved PCM engineering and simulation. The following subsections present detailed material characterization of the GST thin film using X-ray diffraction and transmission electron microscopy, and employs the effective medium theory (EMT) to model the conductivity anisotropy.

2.3.2 Material Characterization[1]

X-ray diffraction (XRD) analysis of the GST film provides evidence of preferential grain growth in the crystalline phases. The peaks shown in Figure 14 are in agreement with published XRD patterns of GST films [89, 90]. The change in intensity and shift in peak locations confirm the phase transition from a-GST to f-GST and eventually to h-GST as annealing temperature increases. The a-GST film is exposed to temperature near 110 °C during the fabrication process; therefore, partial crystallization may occur in the amorphous sample. The XRD pattern of a-GST shows weaker cubic peaks. The f-GST and h-GST films are annealed at 150 °C and 260 °C, respectively, for 15 min to achieve phase transformation. The XRD pattern from h-GST sample indicates a dominant hexagonal closed packed (HCP) phase and a much diminished cubic phase. The HCP (0 1 3) peak replaces cubic (2 0 0) peak when GST becomes stable HCP phase.

[1] The TEM images are taken by Jaeho Lee, Sangchul Lee, and Robert Sinclair of Stanford University. The XRD data are taken by Jaeho Lee.

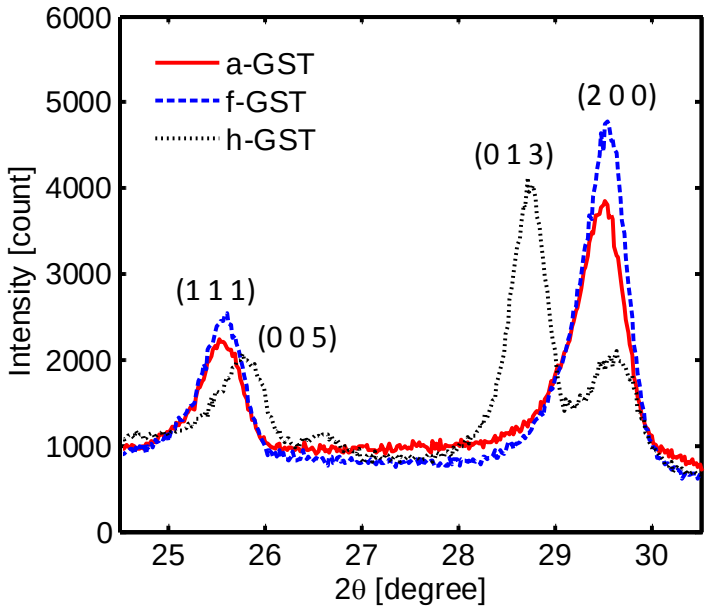


Figure 14. X-ray diffraction (XRD) patterns of a-GST, f-GST, and h-GST. The a-GST is annealed near the phase transition temperature to show a weaker cubic pattern. h-GST exhibits a strong hexagonal (0 1 3) peak and diminished cubic (2 0 0) peak. The intensities of the peaks are compared with data from GST powder sample.

Table 1. XRD peak intensities of different forms of GST

Sample	**Powder GST [91]**	**f-GST thin film**	**h-GST thin film**
Average grain size (nm)	N/A	25.7	24.2
Lattice constants (Å)	6.02	6.00	4.15/18.1
Relative intensity of (111) peak (%)	11.4	50.4	N/A
Relative Intensity of (005) peak (%)	3.6	N/A	45.25

The relative intensities of the corresponding XRD peaks in Table 1 indicate preferred orientation of the GST polycrystalline grains. Table 1 compares the (1 1 1) peak intensity of f-GST and the (0 0 5) peak of h-GST films to the data obtained from an isotropic powder GST sample [91]. The f-GST film used in this study exhibits higher relative intensity for (1 1 1) plane and the h-GST sample shows stronger intensity in (0 0 5) plane than the powder sample does. Since the XRD technique captures the polycrystalline grains aligned perpendicular to the sample surface, these higher intensities indicate the (1 1 1) and (0 0 5) crystal planes are preferentially orientated towards the out-of-plane direction for f-GST and h-GST, respectively. The preferential grain growth of GST thin film is also confirmed by other studies using various techniques. Park *et al.* [87] found anisotropic grain growth of h-GST along the (0 0 0 1) plane at the major axis due to its lowest surface energy with no additional broken atomic bonds. Ryu *et al.* [92] used TEM to reveal a similar preferential growth of GST polycrystalline grains, and Matsui *et al.* [93] reported a columnar grain structure that is aligned in the cross-plane direction.

The preferential crystal growth of polycrystalline GST film leads to a vertically aligned grain structured as observed in the TEM image in Figure 15. The columnar polycrystalline grain structure induces more severe phonon scattering near grain boundaries in the in-plane direction than in the out-of-plane direction. More importantly, we found amorphous region in the shape of thin walls that reside between the crystalline grains. The average grain size of the GST is ~20 nm, while the thickness of the amorphous region is ~5 nm. For a columnar polycrystalline film, the average grain size in the in-plane direction is smaller than in the out-of-plane direction. In addition, the amorphous phase tends to be discrete and dispersed in a sea of crystalline phase. This fact allows us to model the mixed-phase GST film as the bottom diagram in Figure 15. The next section uses the abstracted grain distribution to model the thermal conductivity anisotropy.

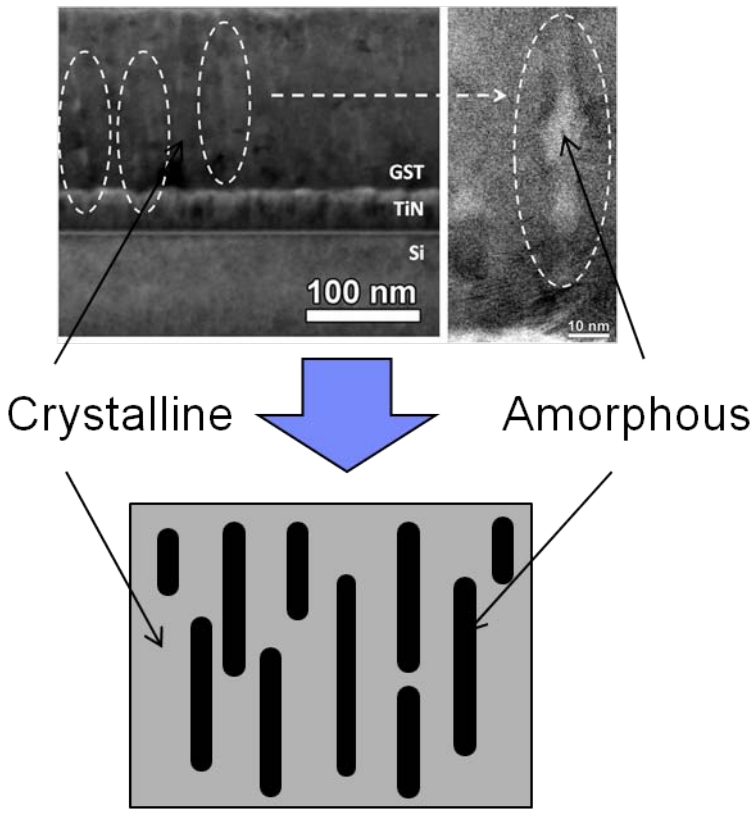


Figure 15. Grain structures of the polycrystalline GST film. Top: transmission electron microscope (TEM) image of the polycrystalline GST film. Amorphous regions are found between the grain boundaries and are aligned in the out-of-plane direction. The TEM image is from our work described in [25]. Bottom: an abstraction of the mixed-phase grain structures where discrete, vertically-aligned amorphous regions are dispersed among a continuous crystalline phase.

2.3.2 Modeling the Thermal Conductivity Anisotropy

GST with a crystalline-amorphous mixture can be treated as a heterogeneous material with two phases. This work models the thermal conductivity of GST films using the Maxwell-Eucken (M-E) theory [94-96], which is a derivative of the effective medium theory (EMT) [97]. Assuming one of the two phases is continuous while the other is dispersed, M-E theory describes the thermal and electrical conductivities of

binary mixtures. The previous section has demonstrated the columnar growth of crystalline grains normal to the surface for GST films annealed at 150 ºC for 30 min using transmission electron microscopy (TEM). We also identified amorphous regions of characteristic dimension ~6 nm located within the continuous crystalline phase at grain boundaries as shown in Figure 15. Grains tend to grow from the film boundaries and elongate vertically with amorphous residues located at grain boundaries [25]. These amorphous regions may originate from incomplete crystal nucleation and growth. Because the grain size of the crystalline GST film is significantly larger than the phonon mean free path of 1nm in GST [6] [15], the effect of phonon scattering at grain boundaries is neglected.

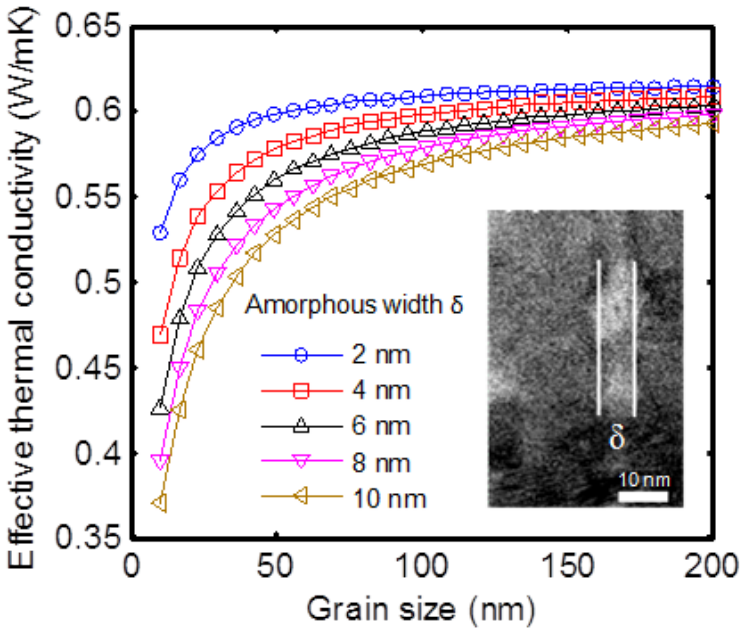


Figure 16. Calculated effective thermal conductivities of f-GST as a function of grain size. The extent of the amorphous region (δ) between crystalline grains is estimated from TEM image [25].

For the crystalline-amorphous GST film modeled here, the thermal conductivity is predicted using M-E theory as

$$K_v = \frac{k_c p_{c,v} + 3k_c k_a \left(1 - p_{c,v}\right) / \left(2k_c + k_a\right)}{p_{c,v} + 3k_c \left(1 - p_{c,v}\right) / \left(2k_c + k_a\right)} \tag{18}$$

where K_v is the effective thermal conductivity in direction v (in-plane or out-of-plane). k_c and k_a are the thermal conductivities of pure crystalline and amorphous GST films, respectively. The volume fraction of the crystalline phase can be estimated as $p_{c,v} = d_{g,v}/(d_{g,v}+\delta)$ where δ is the width of amorphous region and $d_{g,v}$ denotes the average grain size in direction v. Figure 16 shows the effective thermal conductivity calculated as a function of grain size and amorphous region size using Eq. (18). The thermal conductivity generally decreases with reducing grain size and increasing volume fraction of amorphous phase.

The vertically aligned, elongated grain structure explains the anisotropic heat conduction in GST films. Because the average grain size is much larger in the out-of-plane direction, the volume fraction of the amorphous phase is significantly lower in this direction than in the in-plane direction. Since the thermal conductivity of the amorphous phase is only ~30% of that of the crystalline phase, the alignment of amorphous inclusions along the vertically-oriented grain boundaries results in a higher thermal conductivity in the out-of-plane direction according to M-E theory. This effect is calculated using Eq. (14) and (18), and is illustrated as analytical curves in Figure 16.

The film thickness may affect the thermal conductivity anisotropy due to geometrically limited grain growth in the out-of-plane direction, especially when the thickness becomes comparable to the GST grain size. Laterally confined geometry, such as that in confined PCM cells [20], is expected to change the thermal conductivity anisotropy due to the additional interfaces between GST and its surrounding materials. Grain structure will also be strongly influenced by deposition conditions, which may eventually be adjusted to tailor the anisotropic thermal properties of GST in the crystalline phase.

2.4 Impacts of Anisotropic Thermal Conduction on Device Performance

2.4.1 Thermal Disturbance and Minimum Cell Spacing

Thermal conductivity strongly influences the thermal resistance in a phase change memory cell, which affects the programming current during a reset operation. Higher thermal resistance elevates the temperature of the active region in the GST layer and reduces the required programming current. We simulated a set-to-reset transition for various combinations of the experimentally observed thermal conductivity anisotropy and GST layer thickness. The simulation assumes that the GST volume begins in the crystalline phase and that the entire molten region quenches into the amorphous phase. The simulation also neglects the possible cyclic effect on the material properties. Since thermal boundary resistance (TBR) influences the temperature distribution, we include a typical TBR of 20 m^2K/GW between GST layer and electrode [98].

The high temperature during a reset operation of a PCM cell presents a reliability issue by disturbing the state of its neighboring cells [78]. This thermal disturbance limits the minimum cell spacing in PCM arrays. For a given GST thickness, a lower in-plane thermal conductivity confines the heat within the region above the bottom contact more effectively. Figure 17 compares the temperature distribution between isotropic and anisotropic heat conduction. For a 100 nm GST layer under this configuration, the minimum cell space is approximately 135 nm for isotropic GST layer to withstand thermal disturbance, while an anisotropy ratio of 0.6 reduces the minimum cell spacing down to around 80 nm. Therefore, anisotropic GST layers offer one route to higher data storage density, and decreased risk of thermal disturbance.

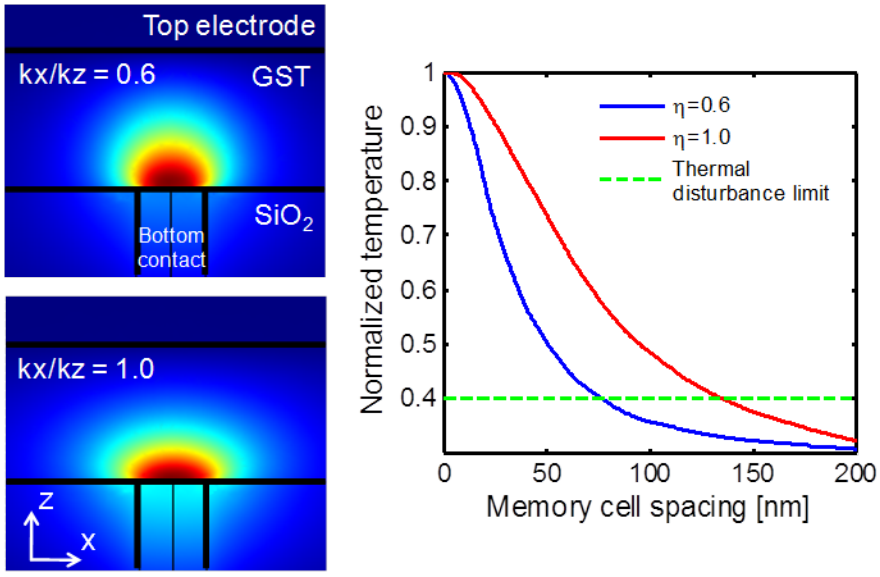


Figure 17. Electro-thermal simulation results. (a) Temperature distribution during reset operation of a PCM cell with anisotropic and isotropic GST layers of 100 nm. (b) Normalized temperature profile along the GST layer in the *x* direction. Thermal disturbance limit is set close to the phase transition temperature neglecting cyclic effects.

2.4.2 Programming Current of PCM Devices

Thermal conductivity anisotropy also influences the thermal resistance in a PCM cell, which determines the programming current. We investigate two types of PCM cells: vertical "mushroom" cells as described in [3] and lateral cells such as those presented in [60]. Figure 18(a) shows the programming current for a vertical cell decreases with increasing GST layer thickness due to higher thermal resistance. In addition, for each GST thickness, the programming current is further reduced with smaller thermal conductivity anisotropy ratio ($\eta = k_x/k_z$). The performance of vertical PCM devices also depends on the geometry in specific cell structures. The confined cell in [20], for example, can affect the anisotropy ratio when the lateral dimensions approach the GST grain size (~20 nm), causing the programming current deviate from the values predicted here.

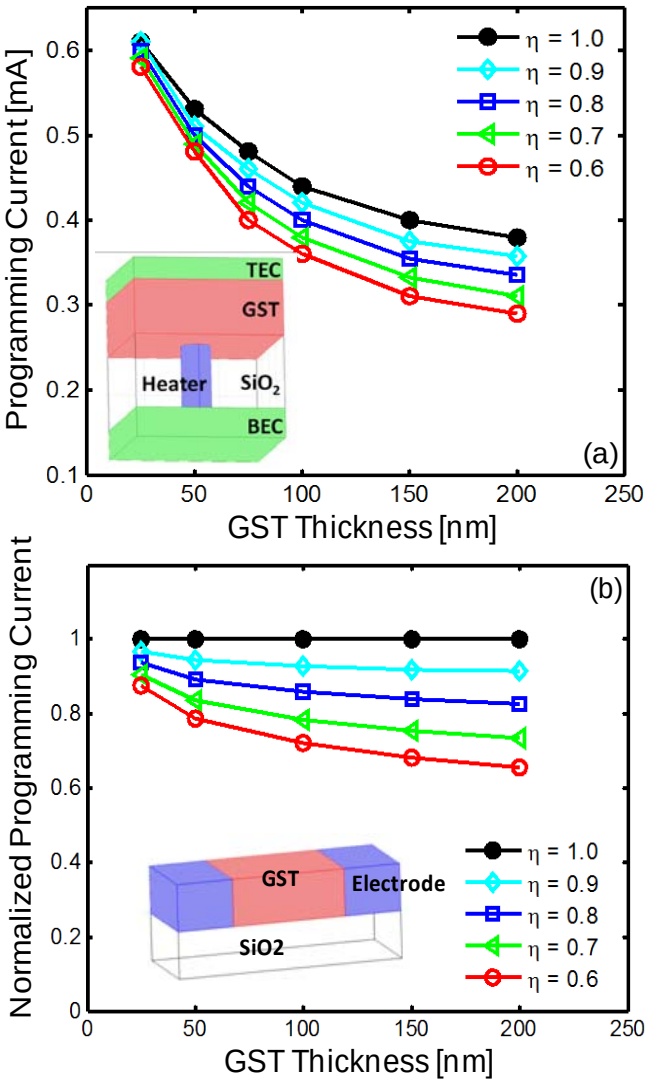


Figure 18. Programming current during a reset operation as a function of GST film thickness and thermal conductivity anisotropy. (a) Programming current of a vertical phase change memory cell. Inset: schematic of the vertical cell including bottom electrode contact (BEC) and top electrode contact (TEC) used for simulation. (b) Programming current of a lateral line-shaped cell. Inset: lateral cell used in the simulation.

The lateral cell model used in this study is depicted in Figure 18(b). Electrical current flows laterally from one electrode to another, causing Joule heating in the GST

bridge that switches the memory cell. Because the cross-sectional area for current flow changes with GST film thickness, we normalize the programming currents to their values under the isotropic heat conduction condition to highlight their relative variation. Figure 18(b) shows that when anisotropy is introduced in the GST layer, the programming current decreases significantly due to the enhanced lateral thermal confinement. An anisotropy ratio η = 0.6 reduces the programming current by about 30% for a lateral cell with 100nm GST layer.

2.5 Summary and conclusions

This chapter measures the in-plane and out-of-plane thermal conductivity of GST thin film in the amorphous, face-centered cubic and hexagonal close packed phases. The microfabricated experimental structures with free-standing thin films are highly sensitive to in-plane heat conduction. A 3ω differential technique with on-substrate samples measures the out-of-plane thermal conductivity of GST thin films. The anisotropy ratio between in-plane and out-of-plane thermal conductivities is measured as 0.8 for f-GST and h-GST, whereas no anisotropy is observed for a-GST.

Grain structure characterizations of the GST thin film using XRD and TEM reveal the mixed-phase composition of polycrystalline GST. The preferential orientation of the grains leads to a columnar structure, and amorphous regions are found at the crystal grain boundaries. This work develops a model based on Maxwell-Eucken theory to accurately model the thermal conductivity anisotropy in crystalline GST thin films for phase change memory. This model relates the directional effective thermal conductivity of GST films to its grain structure and phase purity and is validated by measurement results. Significant reduction of cell spacing and programming current of PCM devices can be achieved considering the anisotropy in the GST layer.

Chapter 3: Multibit Phase Change Memory Analysis and Design Strategy

3.1 Introduction

Phase change memory (PCM) is a competitive next-generation nonvolatile memory technology due to its high performance, endurance, and scalability [1]. PCM stores information by thermally changing the structural phase of a chalcogenide compound such as $Ge_2Sb_2Te_5$ (GST). The crystalline phase with low electrical resistivity and the amorphous phase with high resistivity yield the SET and RESET states of a memory cell, respectively. Electrical pulses induce intense local Joule heating which realizes the phase transitions.

Multibit operation, in which a single cell stores more than one bit of data (e.g. 2 bits/cell requires 4 resistance levels), can substantially increase PCM data densities. The wide resistivity range between the crystalline and amorphous states, which typically exceeds 2-3 orders of magnitude, allows sufficient margins for the intermediate resistance levels. Up to 16 resistance levels have been achieved to store 4 bits per cell by an iterative write-and-verify algorithm [99]. However, the resistance of the amorphous phase drifts continuously after the material has been thermally melted and quenched [100-102]. In addition, the resistance variation during the programming cycle blurs the separation of the intermediate levels and degrades the reliability of multibit PCM. Although the use of programming algorithm such as write-and-verify can mitigate this problem [99, 103, 104], it significantly compromises the programming speed. Novel phase change materials [105-107] and cell architectures [62, 108] can generate more stable intermediate resistances without the write-and-verify sequence. The complex thermal, electrical, and crystallization physics involved in multibit PCM require a fully-coupled multiphysics model for effective design and accurate performance predictions.

Past simulation progress on the multibit problem includes establishing an equivalent PCM circuit with voltage-controlled current source [109], simplifying the

PCM as a one-dimensional heat conduction model [110], using a lumped thermal resistor to describe the RESET operation [111], and inferring the size of the amorphous GST (a-GST) from measured I-√V curves [112]. The crystallization process was usually simplified using the Johnson–Mehl–Avrami (JMA) theory to calculate the crystalline fraction of the GST [113]. However, the resistance of a PCM cell is not only determined by the crystalline fraction, but more importantly by the shape and distribution of a-GST, which are not captured by these approximate models. Kim *et al.* proposed an improved simulation method which computed the local crystal fraction and used the effective medium approximation to determine the local electrical and thermal conductivities of the mixed crystalline and amorphous phases [114]. The various existing models and simulation approaches, some of which are still under debate, require careful comparisons and calibrations to the experimental data that are critical for the sustained improvement in multibit PCM design.

This work develops a fully coupled electrothermal simulation to predict the temporal evolution of GST phases at very short length and time scales. Section II presents a set of transient thermal, electrical, and phase transition models, and compares the computed phase distributions with transmission electron microscope (TEM) images. While achieving good agreement for the RESET operation, the simulated phase distribution deviates from SET process because it neglects the filament growth which is likely the dominant crystallization pattern. Section III evaluates the multibit performances of two widely used PCM structures and programming schemes, and compares the simulations with existing experimental data. Section IV implements the simulation code to explore a new architecture which yields four distinct resistance levels with improved multibit reliability. The results and methodology developed here enable more efficient design of multibit PCM devices.

3.2 Electrothermal Modeling and Simulation[2]

3.2.1 Electrical, Thermal, and Phase Transition Models and Algorithms

Phase change memory involves a rich set of coupled electrical, thermal, and phase change phenomena. One of the most interesting electrical aspects of GST behavior is associated with the amorphous phase [115-117]. For a volume of amorphous GST subject to a voltage less than the threshold voltage V_{th}, the current grows exponentially and can be described by the Poole-Frenkel model [115] as

$$I = I_{PF} e^{\beta_{PF} V_A^{1/2}} \tag{19}$$

where V_A is the applied voltage, and I_{PF} and β_{PF} are material constants [118]. The simulation code numerically evaluates the local electrical field and current density by applying Eq. (19) to each mesh grid in the a-GST volume. The algorithm shown in Figure 19(a) compares the local electric field E to the critical value E_{crit} and adjusts the electrical conductivity accordingly. Threshold switching happens when the local electric field exceeds the critical value. This first occurs around the corners of the amorphous GST where the electric field is the strongest [119], or along the paths where the trap activation energies are the lowest [117]. The local temperature and phase are subsequently determined after the switching. The electric field-dependence of electrical conductivity σ was sometimes ignored in the past based on the fact that the conductivity of the amorphous phase exhibits ohmic behavior for an applied voltage higher than the device threshold voltage [114]. Since the electric field distributes non-uniformly in a PCM cell depending on its geometry and amorphous level, the present work iteratively finds the field-dependent electrical conductivity of each node using $\sigma = \sigma_0 \exp(V\beta_{PF})$, where V is the local voltage.

The thermal model for a PCM cell involves three-dimensional, anisotropic heat conduction as described using:

[2] The modeling work is performed in collaboration with Rakesh Jeyasingh of Stanford University.

$$\frac{1}{D_i}\frac{\partial T_i}{\partial t} = \eta_i\left(\frac{\partial^2 T_i}{\partial x^2} + \frac{\partial^2 T_i}{\partial y^2}\right) + \frac{\partial^2 T_i}{\partial z^2} \tag{20}$$

where D_i is the thermal diffusivity of layer i, and $\eta_i = k_{xy}/k_z$ captures the anisotropy ratio between the in-plane and cross-plane thermal conductivities [26]. Note that Eq. (20) neglects any material nonhomogeneity or defect in the GST film. The nonhomogeneity in material can lead to filament growth of conduction paths which may alter the temperature distribution. Equation (20) also assumes continuous heat dissipation which is valid when the mean free paths of both electrons and phonons (~1 nm) are much smaller than the average grain size (~20 nm) and the cell dimensions [25]. Although often neglected in past work [111, 114, 120], the thermal boundary resistance (TBR) at the material interfaces dominates the nanometer scale thermal conduction problem and can strongly influence the temperature response of the cell [20]. For this reason, we add the TBR to the inter-layer boundary condition using:

$$\vec{q}_i'' = \frac{T_j - T_i}{R_b} \tag{21}$$

where $\vec{q}_i''$ is the heat flux normal to the interface, R_b is the TBR, and T_i and T_j are the temperatures of the adjacent layers. The TBR also shifts the location of the amorphous region towards the heater interface due to the enhanced thermal resistance, an effect to be discussed in the following section.

We use a probabilistic crystallization and nucleation model to evaluate the phase change transition in the PCM cells [75]:

$$P_n = \alpha \Delta t \exp\left\{-\beta\left[E_a + \frac{A}{(\Delta G)^2}\right]\right\} \tag{22}$$

where P_n is the probability of an amorphous small volume to become a crystalline nucleus during time interval Δt. E_a is the activation energy associated with the nucleation, ΔG is the excess Gibbs free energy of the amorphous phase (either solid or molten) compared to the crystalline solid, and A is the determined by the interfacial surface free energy at the phase interface. The frequency factor α relates to the atomic vibration, and the parameter β is defined as $1/k_B T$ where k_B is the Boltzmann constant. Alternatively, a small volume may become crystalline due to the growth of an adjacent nucleus. The crystalline growth velocity V_g can be written as [75]

$$V_g = f a_0 \alpha \left[1 - \exp\left(-\beta \Delta G\right)\right] \exp\left(-\beta E_{a2}\right) \tag{23}$$

where f is a parameter relates to the temperature and crystalline growth mode [75, 121], and a_0 is the atomic jump distance, and E_{a2} is the activation energy associated with atomic diffusion. The model applies these two mechanisms in parallel, as shown in Figure 19(b), to determine the phase distribution.

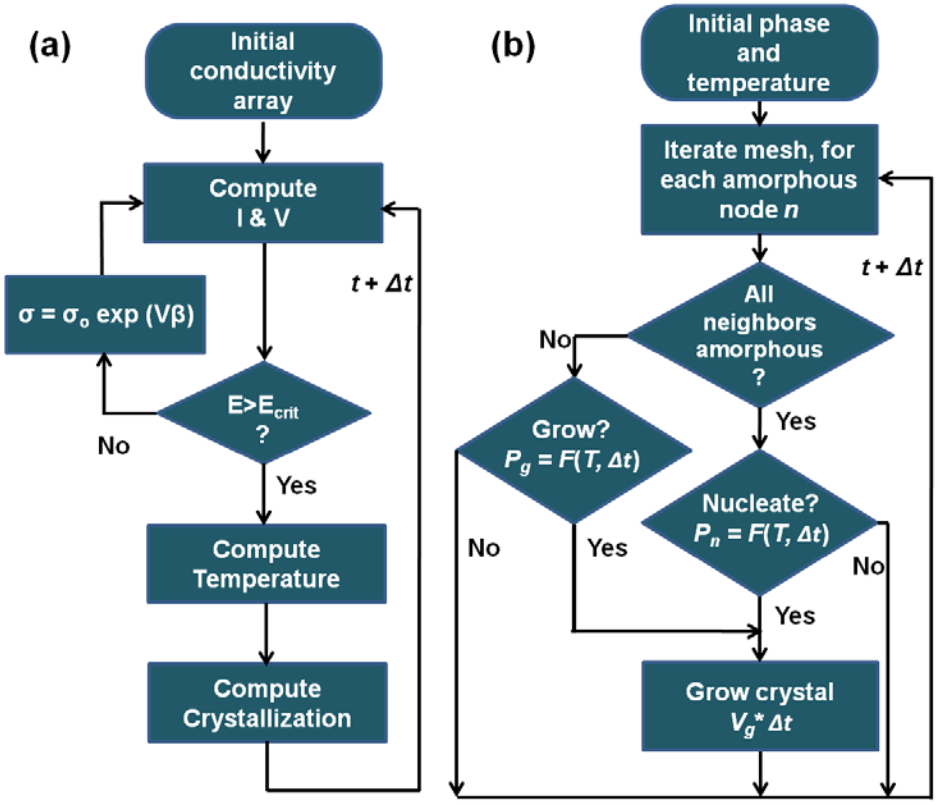


Figure 19. Key computational flows implemented in the coupled simulation. (a) Electrical model compares the local electrical field with the critical field before solving for the temperature and phase; (b) GST crystallization algorithm considers two parallel mechanisms: probabilistic nucleus formation and crystalline growth, both as functions of cell temperature T and time duration Δt.

3.2.2 Simulation results of SET and RESET Operations

This work uses a "mushroom" vertical cell geometry similar to those developed in reference [99] to implement the coupled electro-thermal-phase transition models. The symmetry of the device geometry reduces computation time by using only a quarter cell as illustrated in the inset of Figure 20(a). In this demonstrative simulation, the top electrode contact (TEC) and bottom electrode contact (BEC) are made of tungsten. A TiN heater delivers heating power while reducing atomic interdiffusion with the phase

change chalcogenide. The phase transition occurs in a region very close to the interface between GST and the heater. The TBR at this interface helps enhance the thermal insulation from the cold metal components and reduces the required programming power [20]. The simulation uses a thermal conductivity of 0.56 W/mK for crystalline GST (c-GST) and 0.18 W/mK for a-GST at room temperature [26]. The temperature dependence of thermal conductivity up to 350 ºC has been measured in previous studies [73, 74], and this simulation assumes constant conductivity beyond 350 ºC because the short time scale inhibits further transition to the hexagonal close packed (hcp) phase. The heat capacity of GST is $C = 1.3\times10^6$ J/m^{3}K and assumed constant for different temperatures and phases [25, 114]. The thermal boundary resistance between GST and surrounding material is estimated at 20 m^{2}K/GW based on previous measurements [98] and is assumed to be temperature-independent.

An electrical current pulse induces the SET process causing the cell to transition from a high-resistance state into a low-resistance state as shown from A to D in Figure 20(a). The phase transition involves electrical switching in addition to the thermal effects. Equation (19) suggests that the electrical conductivity of the amorphous region increases exponentially with the voltage before threshold switching. This increase in conductivity causes an even larger current to flow through the amorphous region until the critical electric field is reached for threshold switching which in this case is approximately 1 MV/cm [115]. Following threshold switching, the significantly larger current flowing through the device raises temperature in the amorphous volume, which is sufficient for crystallization. Figure 20(b) shows the different level of crystallization of the original a-GST region after SET pulses with varying amplitudes. For an ideally homogeneous GST layer free of defects as assumed in this simulation, the crystallization process starts from the location close to the heater electrode and grows outwards owing to the higher temperature in that region.

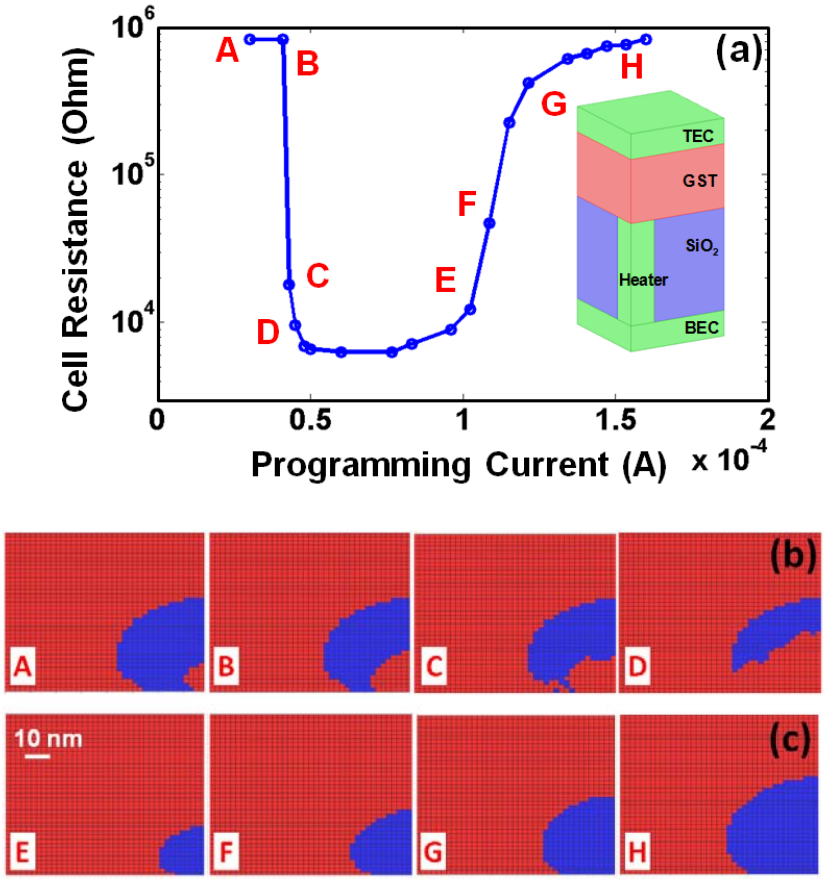


Figure 20. Simulation results of phase transitions in a mushroom-shaped PCM device. (a) Simulated R-I characteristics of a PCM cell for different programming currents. SET operation occurs in A through D, while E through H correspond the RESET process. Inset: schematic of the PCM cell; (b) Cross-sectional view of the GST phase distribution after a SET operation with different current amplitude; (c) GST phase distribution after a RESET process with varying current amplitude. Red and blue colors represent crystalline and amorphous phases, respectively.

A RESET current pulse with larger amplitude and shorter pulse width melts and subsequently quenches the GST active region into the amorphous state. We use an electric pulse of width 10 ns and rise/fall time of 3 ns/3 ns respectively. The initial cell is in the crystalline phase with a low electrical resistance before the pulse. The intense

local Joule heating from a RESET current pulse causes the region close to the heater electrode to melt and quench subsequently. This forms a dome shaped amorphous region near the heater, the volume of which increases with increasing current amplitude as shown in Figure 20(c). The high electrical resistance state can be achieved with sufficiently large amplitude as shown in the R-I characteristic curve as in Figure 20(a). The sharp slope between E and G leads to fast switching between the low and high resistance states. However, it also introduces difficulties in controlling the intermediate resistances which will be discussed in the next section.

3.2.3 Comparison between Simulation and TEM Images

In order to verify and calibrate the models developed here, we compare the simulated phase distribution after a partial RESET operation to the TEM images. Past work [122] identified the phase distribution of a vertical PCM cell at SET and partial RESET states. Electron scattering pattern confirms the polycrystalline phase in the initial SET state as shown in Figure 21(a), and a partial RESET operation forms an amorphous cap on top of the heater as in Figure 21(b). Abnormally large grains of c-GST are found around the amorphous cap with substantially different texture from the initial c-GST region. Several other studies also observed similar phenomenon after a RESET pulse and inferred the possible shrinkage of amorphous region after RESET pulse [112, 123]. Our transient simulation captures this effect reasonably well and reveals the detailed phase transition dynamics. First, the active region in the GST layer melted during a RESET pulse (Figure 21(c)). As the cell starts to cool, several nodes at the liquid-solid interface start to nucleate or solidify into amorphous GST (Figure 21(d)), the probabilities of which depend on the temperature and the cooling rate as discussed earlier in this section. Nucleation and crystal growth inside the amorphous region is also possible if the temperature remains between the crystallization temperature and the melting point during time interval Δt. The competition between the recrystallization and quench- amorphization processes determines the shape and volume of the final amorphous cap which is always smaller than the initially molten volume as shown in Figure 21(f). The recrystallized region

undergoes rapid phase change, resulting in different grain size around the final amorphous cap than the initially annealed c-GST as observed in the TEM images.

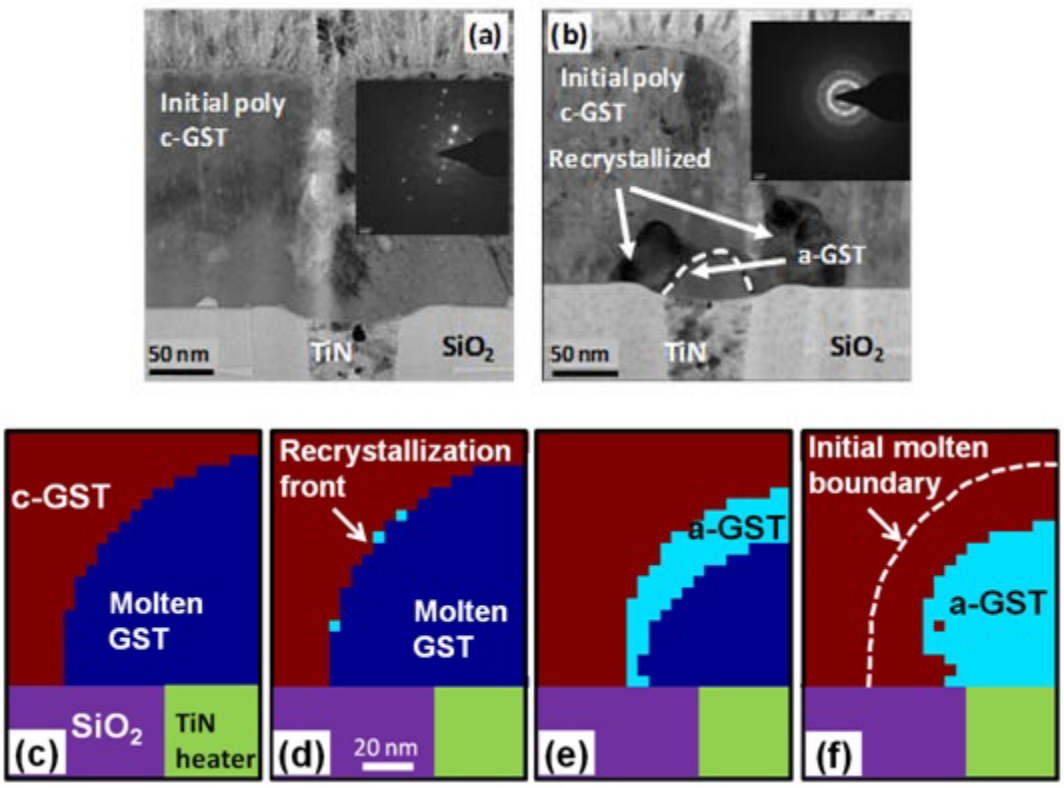


Figure 21. Comparison of transmission electron microscopy (TEM) images and the simulated phase distribution after RESET pulses. Cross-sectional TEM image were taken with a similar device in a previous study by Kuzum *et al.* [122]. (a) The GST film is polycrystalline (c-GST) in the initial SET state as confirmed by the electron diffraction pattern in the inset. (b) Amorphous GST (a-GST) cap is formed on top of the TiN heater after RESET operation. The inset shows the electron diffraction pattern corresponding to the a-GST cap region. (c)-(f) Simulated transient phase distribution during a partial RESET process. The area between the initial molten region and the final a-GST cap resulted from recrystallization process explains the different crystalline texture around the a-GST cap.

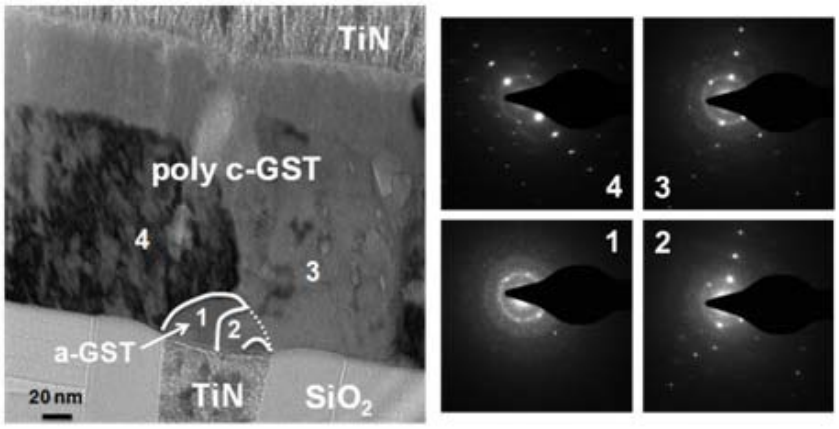


Figure 22. Filament-like crystallization of a PCM cell after partial SET pulses. The cross-sectional TEM images were taken in a previous study by Kuzum *et al.* [124]. The amorphous region 1 is marked by dashed lines. A thick filament region 2 of crystalline nature is seen between the amorphous regions. Regions 3 and 4 are polycrystalline as confirmed by the electron diffraction pattern. This filament growth pattern, possibly due to material inhomogeneity and defects, is not captured by the current simulation.

Another interesting aspect of the phase change process is to understand how the SET process happens. As described at the beginning of this section, the SET involves electrical transport before switching and a thermal-phase change process after switching. The theoretical model with ideal, homogeneous material quality predicts that the current flows through the entire amorphous volume. However, the current can also trickle through filament-shaped conduction paths that have the least resistance in the amorphous state [117]. Due to the nonequilibrium distribution of electrons in traps from the equilibrium states (e.g. Fermi level) developed at high fields [115], the switching happens and a large current flows through these filaments, causing a temperature rise in the surrounding regions. Subsequently, the crystallization process initiates around this filament region and eventually crystallizes the entire amorphous region. One way of studying the filament-like growth is to apply a SET pulse of voltage above the threshold but of shorter pulse width which prevents the entire

volume to crystallize. This partial SET programming yields intermediate resistance values that can be used for multibit PCM operations. Figure 22 shows the cross-sectional TEM image of an initially amorphous PCM cell after a partial SET programming [124]. A polycrystalline filament conduction path embedded between the amorphous regions is evident in the graph, indicating that the amorphous conduction is more likely filamentary in nature. However, the present simulation model assumes a more homogenous current flow during the SET process which generates an over-idealistic phase distribution as in Figure 20(b). The strong electric field near a crystalline filament facilitates the nucleation of additional conductive particles at the end of the filament, making it longer and resulting even larger local electric field [125]. As a result, the required voltage to set a cell based on filament-like crystallization mechanism may be lower than predicted by the simulation. The future versions of this simulation will incorporate the filament-based conduction model for the SET process.

3.2 Multibit PCM Performance Analysis

The vertical mushroom cells similar to the inset of Figure 20(a) have been explored for multibit programming [99, 126]. Varying the amplitude of the programming pulse can control the cell resistance by delivering different amounts of heating power which forms the amorphous cap on top of the heater. However, the sharp transition between the low and high resistance states as shown in Figure 20(a) makes it difficult to precisely control the intermediate resistances. Here we investigate another strategy proposed in reference [99], in which the tail duration of a current pulse determines the resistance level by adjusting the cooling rate of the cell. Atoms in the molten phase can be frozen into a disordered amorphous structure if the cooling rate is faster than the crystallization rate. The crystalline growth of GST requires a proper temperature range and a sufficient period of time during which the temperature stays in this range. The thermal time constant scales with the cell resistance and heat capacity. The former is determined by the heater contact area and the resistivity the

GST layer, while the latter mostly scales with the volume of the PCM cell. The transient simulation of the vertical cell shows a thermal time constant of ~5 ns which is of the same order of magnitude as the nucleation time. Therefore, a RESET pulse tail duration much longer than the thermal time constant can facilitate the recrystallization process which leads to a lower cell resistance.

3.2.1 Tail Duration-Controlled Mushroom Cell

Figure 23 demonstrates the control of intermediate resistances by changing the tail duration (t_{fall}) of a RESET pulse. In this simulation, a rise time t_r of 5 ns induces fast heating, and the active region of GST is melted during the pulse width t_w of 25 ns. As the current amplitude decreases and the temperature drops, the molten GST can either nucleate and grow to the crystalline phase or quench to the amorphous phase, depending on the temperature and cooling rate (see Figure 21(c)-(f)). The final shape and volume of the amorphous region determines the cell resistance. Tail durations from 20 ns to 200 ns successfully control the intermediate resistances between SET and RESET levels. In order to test the accuracy, we compare the simulation results from this work with experimental data from reference [109]. Since detailed material properties are not available in [109], we use the GST properties in Section II and the electrode material properties shown in Table 2. The high and low resistance bounds of the simulation results are then calibrated to the experimental data. The model from this work predicts the resistance change as a function of the tail duration which achieves good agreement with experimental data. Figure 23 also compares the model from this work with those reported previously. The general trend of the resistance change can be captured by all three models. However, the ones in [109] and [111] result in relatively large deviations in the intermediate resistances which are important to the multibit PCM applications. The difference most likely results from the fact that these models are based on the GST crystalline fractions without considering the shape of the amorphous cap. By computing the detailed phase distribution, this work improves the accuracy in predicting the resistance transition behavior of a PCM cell.

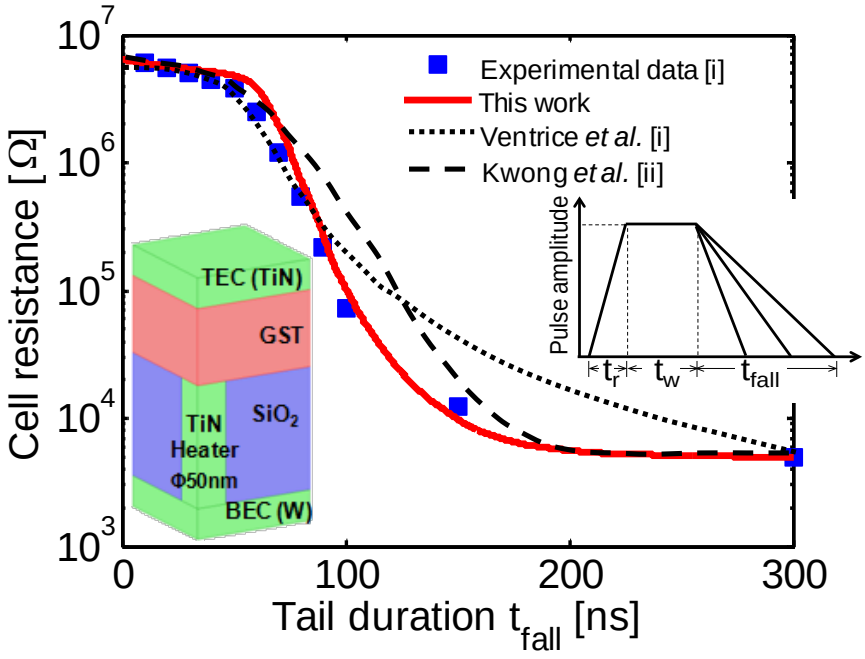


Figure 23. Mushroom cell resistance as a function of the tail duration of a RESET current pulse. Experimental data are taken from i-[109]. This work achieves improved prediction of the transitional behavior of the cell resistance compared with two other models proposed in i-[109] and ii-[111]. Inset: mushroom cell schematic used in this simulation, and the shape of a RESET pulse.

3.2.2 Amplitude-Controlled Confined Pillar Cell

Another widely used PCM structure features a confined GST element between the heater and the electrode [127] as illustrated in the inset of Figure 24. In this simulation, the diameter and height of the confined GST element are 75 nm and 50 nm, respectively, which represents the current fabrication technology [127]. The confined pillar structure improves the heating efficiency because it generates Joule heating in the center of the GST element and away from the GST-electrode interface. The thermal boundary resistances around the GST element further impedes the heat loss through the surrounding electrodes and dielectrics. The RESET pulses with varying amplitude induce different levels of amorphization in the GST pillar, leading

to a resistance profile as shown in Figure 24. The RESET programming pulse in this simulation features rapid rise time and tail duration of 5 ns each, and a pulse width of 65 ns. The near logarithmic relationship between cell resistance and pulse amplitude from 0.6 mA to 0.9 mA is consistent with experimental data [127]. As a comparison, we overlay in Figure 24 the results from an amplitude-controlled mushroom cell [120] which has a similar transition current of 0.55 mA. We normalize the resistance data from the mushroom cell to the upper and lower bounds of the pillar cell while preserving the values of pulse amplitude in order to compare their transitional behaviors. The pillar cell structure yields a more gradual R-I curve than the mushroom cells for the same transition current amplitude, indicating more effective control of the intermediate resistance states. As shown earlier, the resistance of a mushroom cell is predominantly determined by the phases near the GST-heater interface. Instead of forming an amorphous cap which abruptly blocks the heater contact area as in the mushroom cell (Figure 21), the amorphization occurs gradually from the center of the confined GST element in the pillar cell which offers a more gradual resistance change as a function of current pulse amplitude.

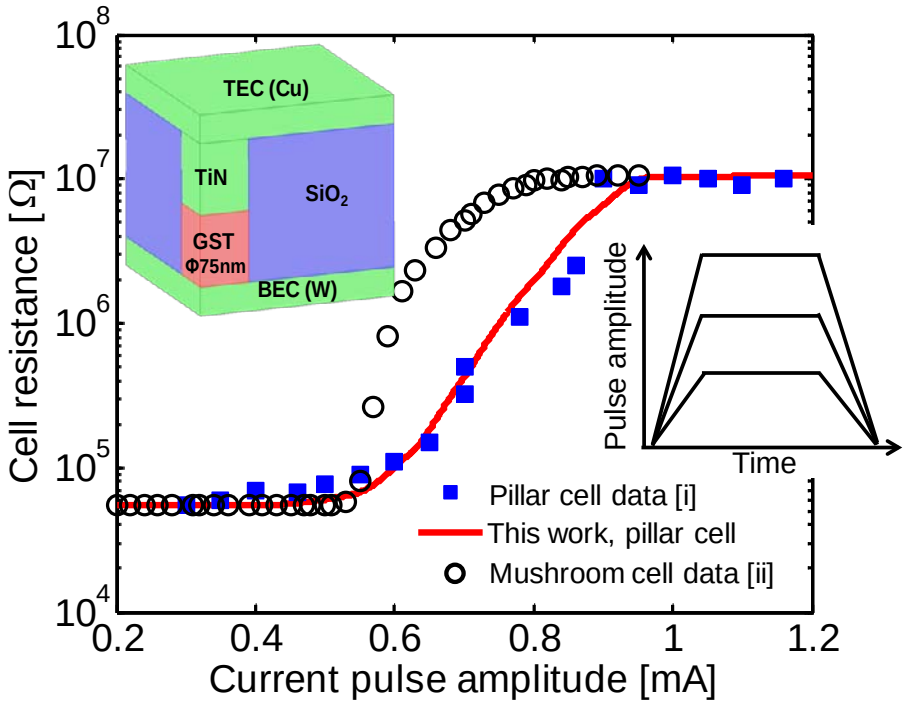


Figure 24. Amplitude-controlled cell resistance after a RESET current pulse. Experimental data of the confined pillar cell are taken from i-[127]. The simulated intermediate resistances match reasonably well with measured resistance evolution. The pillar cell yields more gradual resistance change comparing to a mushroom cell controlled by the same amplitude-based scheme ii-[120]. Inset: confined pillar cell schematic, and the shape of RESET pulses with varying amplitudes.

Table 2. Electrical conductivity σ, thermal conductivity k, and heat capacity C of the electrode and insulator materials used in the simulation.

	σ [S/m]	k [W/mK]	C [J/m^{3}K]
TiN	1×10^6 [a]	15 [b]	3.2×10^6 [a]
W	7.1×10^6 [c]	175 [a]	2.58×10^6 [a]
Cu	5.4×10^7 [d]	356 [d]	3.4×10^6 [e]
SiO2	1×10^{-14} [a]	1.2 [f]	3.1×10^6 [a]

[a] Ref. [114], [b] Ref. [128], [c] Ref. [129], [d] Ref. [130], [e] Ref. [131], [f] Ref. [47]

3.3 Novel Cell Structure and Multibit Design Strategy

One of the biggest challenges for multibit PCM is the poorly separated resistance levels owing to the continuous transitions of R-I characteristics, a problem which is augmented by the drift of resistance in the amorphous condition [1, 103, 132]. The write-and-verify technique can mitigate this problem, but it introduces substantial overhead in programming latency [99, 103]. The uncertainty in cell resistance can be significantly reduced if the R-I characteristics exhibit distinct, stair-case resistance levels over a certain range of programming currents. Past research has explored several implementations including stacking chalcogenide layers with different stoichiometries and resistivities [105-107], and novel PCM architectures that rely on the asymmetric temperature distribution in the cell [62, 108]. These implementations generally occupy large areas owing to their lateral or parallel structures.

Here we explore the potential of a stacked vertical multibit cell, which achieves four distinct resistance levels in a much reduced device footprint. The model developed in this work provides a valuable tool to accurately predict the phase distribution and analyze the performance of the novel cell structure. Figure 25(a) shows the cell structure. Two heating elements are connected in parallel on each of the two floors. The confined GST elements with thickness less than 10 nm can be fabricated by the sidewall deposition technique that has been developed extensively [108, 133]. The BEC, TEC and the middle electrode contact (MEC) are made of tungsten, which is a good thermal and electrical conductor, in this demonstrative design. Potential optimizations include using TiN as electrode material to minimize diffusion between GST and electrode. The MEC is floating electrically and thermally, decoupling the heating power of the GST elements on the two floors. The heating power for R_1, for instance, can be written as

$$P_1 = \frac{I^2 R_1}{\left(1 + R_1 / R_0\right)^2} \tag{24}$$

where I is the applied programming current, R_1 and R_2 are the electrical resistances of the two elements on the lower floor. Equation (24) and the electrical model in Figure 25(b) suggest that the heating power of one floor is solely determined by the resistances on that floor, and is completely decoupled from the other resistors (R_2 and R_3). A representative temperature map of the cross-section of the device is shown in Figure 25(a) where the temperature of each GST element is clearly separated, leading to effective control of the phase change in each GST element. Four resistance levels can be achieved by controlling the states of the three GST elements as shown in the insets of Figure 25(c). The width of each GST elements determines its current density, temperature and the resulting phase distribution. In this design, the widths of the four heating elements R_0 through R_3 are 10 nm, 10 nm, 30 nm, and 10 nm, respectively, and the depth of the device is 20 nm. The three GST elements amorphize sequentially after RESET pulses with amplitudes from 60 μA to 90 μA and pulse width of 65 ns, yielding a 2-order-of-magnitude resistance margin. The small contact area of the GST elements enables an order-of-magnitude reduction in programming current compared to other designs [99, 108, 127]. A SET current pulse with amplitude of 35 μA and duration of 200 ns crystallizes all the GST elements and sets the cell to low resistance level. The simulated temperature profile in Figure 25(a) also shows that the peak temperature occurs away from the GST-electrode interface which minimizes the interdiffusion between GST and the electrode materials.

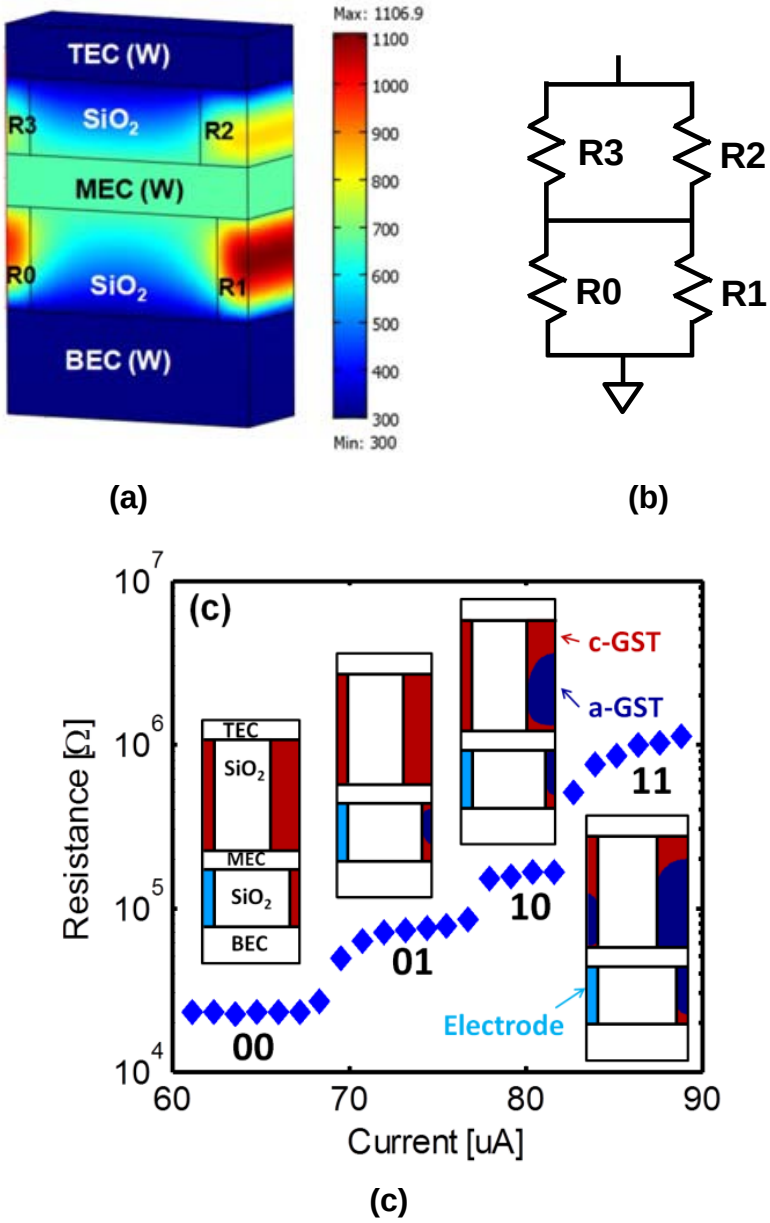


Figure 25. Stacked vertical multibit cell. (a) A schematic and representative temperature distribution of the cell. (b) Electrical model in which the heating power is decoupled between the two floors. (c) Simulation results of the multibit programming with four distinct resistance levels. Insets: device cross-section view and phase distributions at each of the four resistance levels. Red and dark blue corresponds to c-GST and a-GST, respectively. The heating element (light blue) is a tungsten electrode.

3.4 Summary and Conclusions

Multibit operation is an important enabling feature that can allow PCM to compete with other non-volatile memory technologies. The electrothermal simulations developed here reveal that the thermally-induced, transient phase transitions are critical to multibit programming. Recrystallization from the melted phase during a RESET operation reduces the volume of a-GST as a function of the thermal time constant of the PCM cell. The coupled electrothermal modeling improves the accuracy in predicting the intermediate phase distributions and cell resistances, both of which are important in multibit PCM operations. The inefficient intermediate resistance control limits the multibit capability of the standard cell structures such as the mushroom cell and the confined pillar cell. In this work we explore the operation of a stacked vertical cell structure which allows the programming current to be reduced by an order of magnitude comparing to conventional PCM cells.

Chapter 4: High Electron Mobility Transistor

4.1 Introduction

High electron mobility transistors (HEMTs) based on AlGaN/GaN are promising for next generation radar applications due to their wide bandgap, high electron velocity, and high breakdown field. Studies over the past decade have increased the maximum power density from around 10 W/mm [134] to more than 30 W/mm [135]. HEMT self heating can compromise the reliability by degrading electron mobility, promoting the formation of crystalline defects, decreasing the breakdown voltage, and accelerating the interdiffusion of gate-channel materials [136]. The geometry and thermal properties of the complex multilayer structure in a HEMT device govern its thermal resistance and temperature rise. The thermal boundary resistance (TBR) at each interface also contributes significantly to the total thermal resistance and strongly influences the temperature rise in the device channels [137]. Since the cooling system represents a significant fraction of the overall cost of a HEMT transmitter, past studies have developed different approaches for effective heat dissipation such as flip-chip bonding [138] and more thermally conducting substrates [139].

Silicon carbide (SiC) substrates are common for the epitaxial growth of high-performance GaN/AlGaN HEMT structures because they offer much higher thermal conductivity (~400 W/mK) than conventional sapphire substrate (~35 W/mK). Substrates containing CVD diamond are promising owing to their potentially high thermal conductivity, which could be as much as 3 to 5 times higher than that of SiC. However, the benefit of a diamond substrate is often partly offset by the additional low-thermal-conductivity transition layer necessary for high-quality GaN heteroepitaxy [28]. Successful design of the GaN/AlGaN HEMT with a diamond substrate requires a comprehensive understanding of the impact of diamond substrate with various nucleation layers and TBRs. In addition, modern HEMTs often employ a compact multifinger configuration for high-power operations. The single gate hot spot (~1μm), multifinger pattern (1-100μm), and the device package (>100μm) represent

three distinct characteristic length scales whose thermal resistances are dominated by different components in the HEMT multilayer structure. Previous studies have experimentally measured the temperature rises in the channel region using photocurrent measurement [140], and in the multifinger and package level using Raman spectroscopy [141]. However, there is no complete thermal model available that investigates the scaling effect which facilitates device designs for more effective heat removal.

This work examines the best available data for composite substrates containing SiC and diamond and predicts the potential improvement available through the use of diamond on the temperature rise in HEMT geometries. This allows the reader both to understand the performance available in contemporary composite substrates based on SiC and to assess the improvements in thermal properties, in particular the thermal interface resistances, that will be required for future advances. Section II develops a semi-analytical simulation approach for the temperature rises at different length scales, with the goal of providing a more rapid and flexible process than is available through conventional finite element software. Section III compares the thermal performance of diamond- and SiC-based substrates with different configurations and discusses the potential benefits of removing or reducing the thermal resistance of the transition layer for the GaN.

4.2 Material Properties and Thermal Modeling

4.2.1 Thermal Properties of HEMT Constituent Materials

The thermal properties of the materials in GaN/AlGaN-based HEMT devices have been the subject of much research over the past decade. Our previous and ongoing work measured the thermal conductivities of GaN, AlGaN, AlN, SiC, and diamond films from multiple fabrication sources. These measurements use picosecond thermal reflectance and the electrical Joule heating techniques to extract the multiple interface resistances and anisotropic thermal conductivities in these complex multilayer systems. Figure 26 summarizes the experimental data from our past work [142] and

other studies [143-149], and the reader can refer to the original paper for details on the experimental procedures.

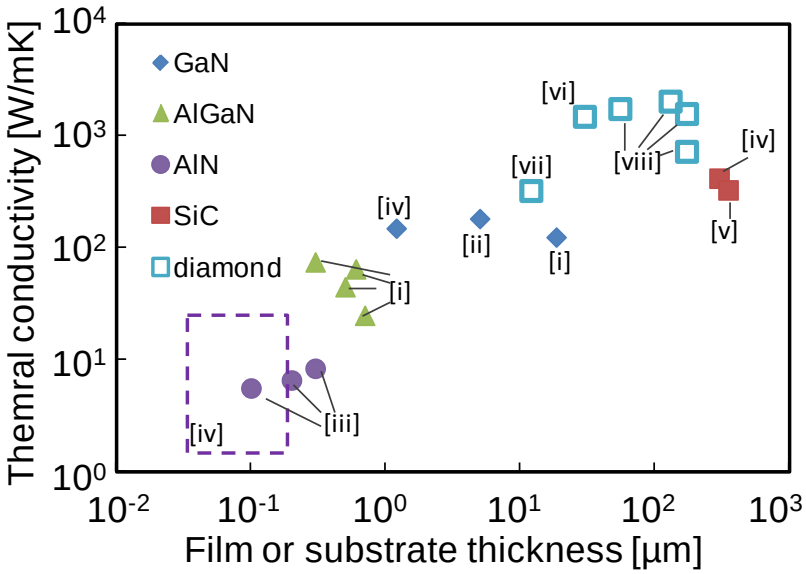


Figure 26. Representative cross-plane thermal conductivity data for the materials in AlGaN/GaN HEMT devices. Data are selected from the following references: i-[150], ii-[151], iii-[152], iv-[145], v-[146], vi-[147], vii-[148], viii-[149], iv-[143].

Large variation in the measured thermal conductivity exists among the polycrystalline diamond substrates from different sources because the material quality strongly depends on the grain structure, film thickness, and growth conditions. The thermal conductivity of GaN is also known to depend strongly on the material quality including dislocation density, impurity concentration, etc. [153] Although the GaN buffer layer has a moderately high thermal conductivity of ~120 W/mK, the low thermal conductivity (less than 10 W/mK) of the AlN nucleation layer introduces additional thermal resistance. The AlN nucleation layer mitigates the excessive stress due to lattice mismatch between GaN and the substrate which improves the quality of GaN heteroepitaxy. Thermal boundary resistance at the layer interfaces due to phonon scattering also increases the overall thermal resistance of a HEMT device.

4.2.2 Numerical Modeling

The single-finger hot spot, the multi-finger array, and the device package of a HEMT represent a range of characteristic length scales which experience different levels of thermal resistance. In order to study the complex heat conduction in all these length scales, we developed a set of numerical code which models the multilayer HEMT structure as shown in Figure 27. This quasi-closed form methodology is better suited for this study than the general-purpose commercial FEA software due to its ability to quickly modify the complex HEMT geometries with anisotropic and temperature-dependent material properties. It conveniently performs the thermal simulations with both steady-state and transient conditions for much less computing time.

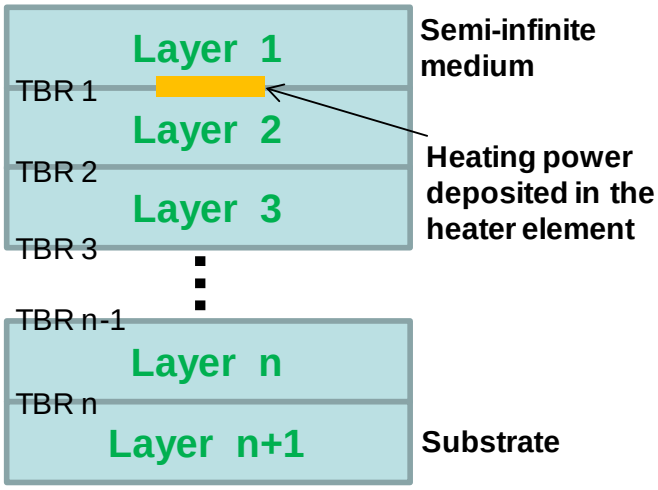


Figure 27. Multilayer HEMT model for thermal simulation. The heating power is deposited to the heater element with varying dimensions.

Layer 1 corresponds to the semi-infinite medium (usually air), and layers 2 to *n* represent the different compositions of the HEMT structure such as GaN/GaAlN device layer, GaN buffer, GaAlN transition layer, and AlN nucleation layer. The HEMT channel region lies between Layer 1 and Layer 2, where an AC heating power

is deposited in the heated area $W \times L$. The bottom Layer n+1 stands for the semi-infinite substrate. This bottom boundary condition recognizes the fact that the thickness of the substrate is usually much larger than that of the other films as well as the channel length. The measured or best known material properties are used for each layer, as well as the TBRs in between.

The code finds the temperature rise averaged over the heated area by solving the time-domain, two-dimensional heat diffusion equations:

$$\frac{1}{D_i}\frac{\partial T_i}{\partial t} = \eta_i \frac{\partial^2 T_i}{\partial x^2} + \frac{\partial^2 T_i}{\partial z_i^2}, \tag{25}$$

$$k_{1,z}\left.\frac{\partial T_1}{\partial z_1}\right|_{z_1=d_1} - k_{2,z}\left.\frac{\partial T_2}{\partial z_2}\right|_{z_2=0} = \frac{P}{2bL}e^{-j2\omega t}, \tag{26}$$

$$-k_{i,z}\left.\frac{\partial T_i}{\partial z_i}\right|_{z_i=d_i} = -k_{i+1,z}\left.\frac{\partial T_{i+1}}{\partial z_{i+1}}\right|_{z_{i+1}=0} = \frac{T_i\big|_{z_i=d_i} - T_{i+1}\big|_{z_{i+1}=0}}{R_{b,i}}, \tag{27}$$

$$\left.\frac{\partial T_n}{\partial z_n}\right|_{z_n=d_n} = 0 \tag{28}$$

In Eq. (25) to (28), the subscript i denotes the i^{th} layer from the top, and n is the total number of layers. Geometric parameters b and L are the half width and length of the heater, respectively. $k_{i,z}$ is the cross-plane thermal conductivity of the i^{th} layer, and $R_{b,i}$ is the thermal boundary resistance for the interface between layer i and i+1. The thermal conductivity anisotropy is defined as $\eta = k_x/k_z$. The heating power P is injected at the boundary between layer 1 and layer 2. A recursive algorithm solves these equations and finds the average temperature riseΔT in the heater using an extended version of the matrix formulation method developed by Feldman [154]. A very low frequency (e.g. 0.1 Hz) essentially simulates the steady-state temperature rise under DC heating power.

4.2.3 Model Calibration and Comparison with Measurement Data

We provide additional discussion about the above mentioned model because: (1) The code assumes a semi-infinite substrate; however, a more realistic setup would be a finite-thickness substrate with a fixed temperature at its bottom boundary. We need to check the conditions upon which this assumption is valid. (2) The implementation of the numerical model involves extensive mathematical operations, including recursive matrix transformations. We need to calibrate the code to debug and check its correctness in the DC limit of a frequency-domain solution.

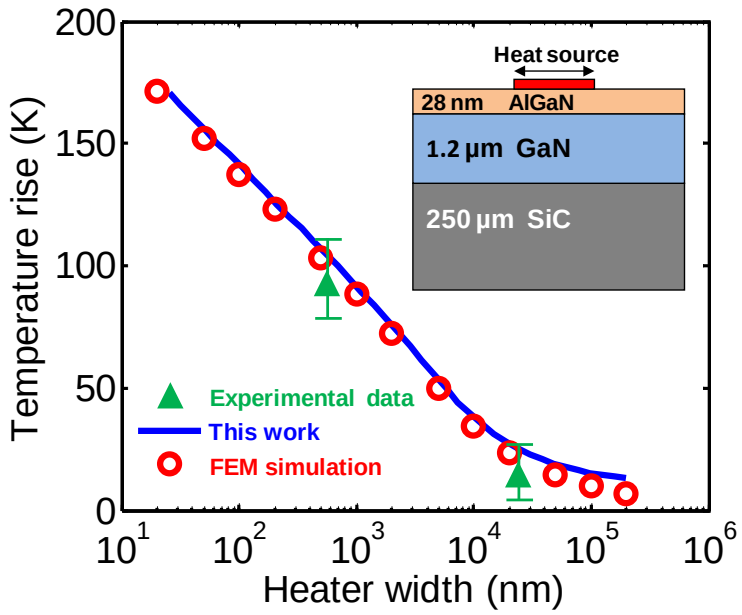


Figure 28. Comparison of the semianalytical HEMT thermal model with finite element method (FEM) simulation COMSOL and the experimental data from [141]. Our simplified model achieves good agreement for length scales smaller than 100 µm.

To determine the accuracy of our model, we compare the result from our quasi-analytic model, a commercial FEM package (COMSOL), and experimental data from Raman thermometry of a similar structure [141]. They agree reasonably well for

length scales smaller than 100 μm which are the most critical HEMT thermal analysis as shown in Figure 28. The semi-infinite assumption of the substrate thickness becomes invalid when the heater length scale is greater than 100μm, resulting in a ~20% difference from our simplified model to a full numerical solution using COMSOL. Figure 29 further confirms the modeling approach using our DC Joule heating and electrical resistance thermometry measurements on a complex HEMT substrate discussed (in the following section). The GaN buffer dominates the temperature rise in this sample, and reasonable agreement is obtained using thermal conductivity data for the GaN obtained using independent time-domain picosecond photothermal microscopy.

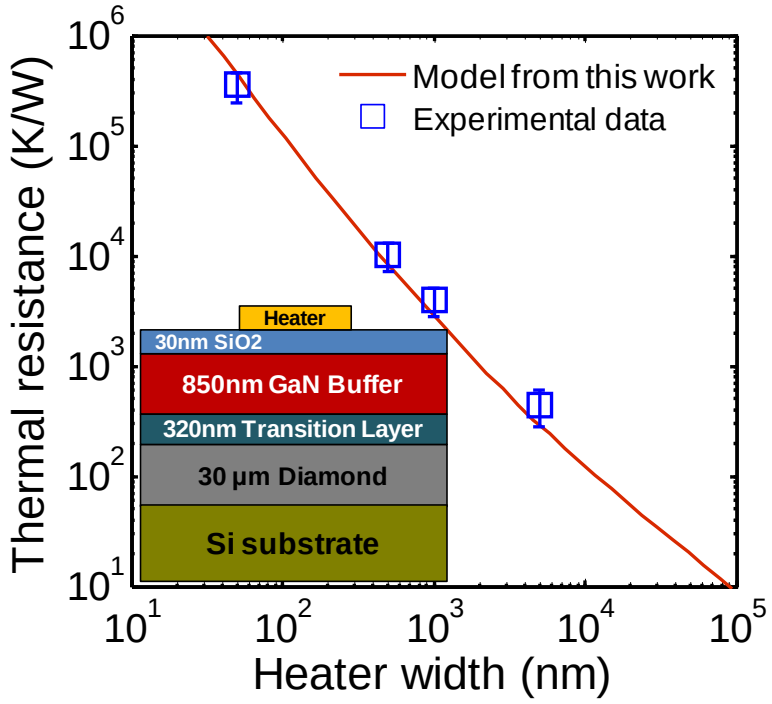
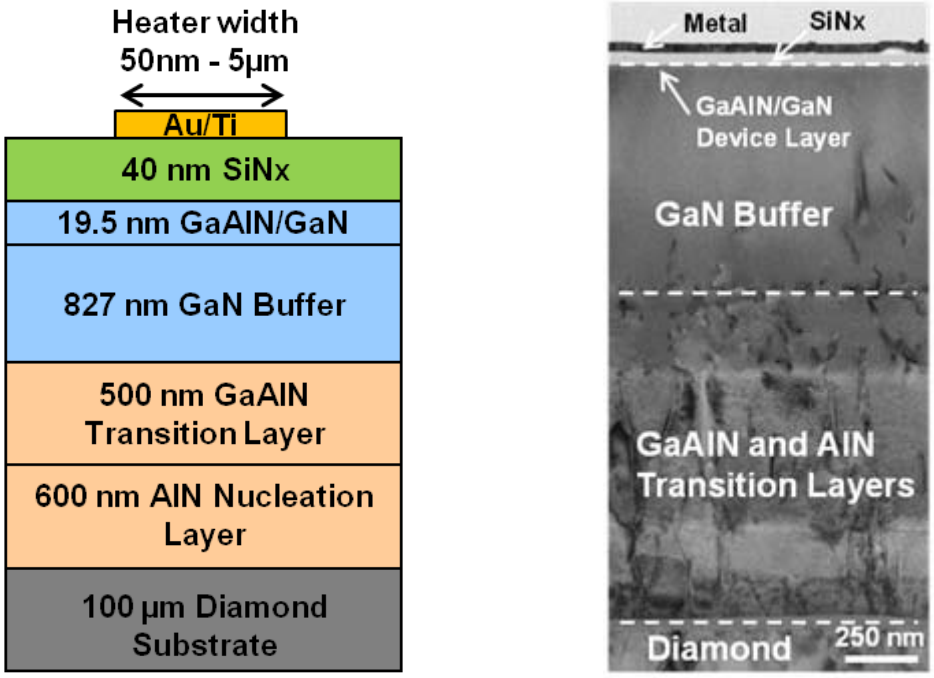


Figure 29. Simulated and measured thermal resistances seen by different heating source on a multilayer HEMT test structure. The experimental data are taken with the nanoheater measurement in this work.

4.3 Thermal Characterization Using Nanoheaters

4.3.1 Sample Preparation and DC Joule Heating Thermometry

We obtained the GaN/AlGaN HEMT samples from multiple suppliers with different layer structures engineered to extract specific thermal properties of the constituent layers and interfaces. One representative sample with diamond substrate for enhanced heat removal is shown in Figure 30.



(a) (b)

Figure 30. Layer structure and thicknesses of a representative HEMT sample. (a) Cross sectional schematic of the sample structure with nanoheater bridges deposited on the top; (b) TEM image of the sample stack.

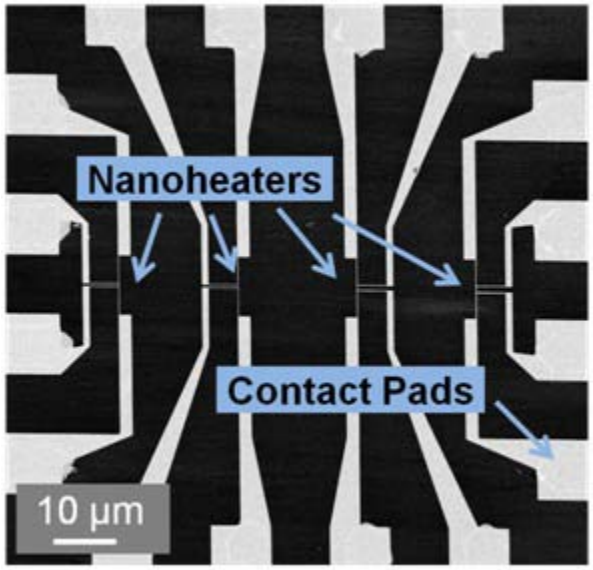


Figure 31. SEM image of a top view of the fabricated nanoheaters by e-beam lithography. Heater width of the sample varies from 50 nm to 5 µm. [3]

The AlN nucleation and GaAlN transition layers are necessary for mitigating the lattice mismatch between GaN and Si substrate. After the GaN is grown to the desired thickness using metal-organic chemical vapor deposition (MOCVD), the Si substrate is removed and the remaining GaN/GaAlN layers are attached to a diamond substrate using a proprietary adhesion layer. The 19.5 nm GaAlN/GaN layer is the active region for HEMT devices. The sample also comes with 40 nm SiNx on top which provides electrical insulation for the subsequent metal heater patterning. We fabricated Au nanoheaters on top of the sample stack with 4-probe configuration. The fabrication process is comprised of two major steps: 1) optical photolithography patterns the larger components in the peripheral including contact pads and contacting paths, and 2) electron beam (e-beam) lithography to pattern the fine nanoheaters in the center as shown in Figure 31. The high resolution of e-beam lithography achieves narrow heater widths in the sub-micrometer domain, and we have successfully

[3] Sample design and fabrication are performed in collaboration with Dr. Takashi Kodama, Stanford University.

fabricated electrically stable metal heaters with width of 50 nm[4]. All the metal patterns contain 5 nm thick Ti as adhesion layer and 55 nm Au as heater bridges.

The electrical thermometry captures the temperature by measuring the electrical resistance change in the nanoheaters. The temperature coefficient of resistivity (TCR) of Au is dependent on film thickness partly due to the electron scattering at film boundaries. Since the heater width affects the actual film thickness in the e-beam lithography process, it is necessary to calibrate the TCR of each heater width as shown in Figure 32. The temperature of the sample is gradually raised by a heating stage and monitored by thermal couples. Measured TCR of Au distributes around 0.0022 K^{-1}.

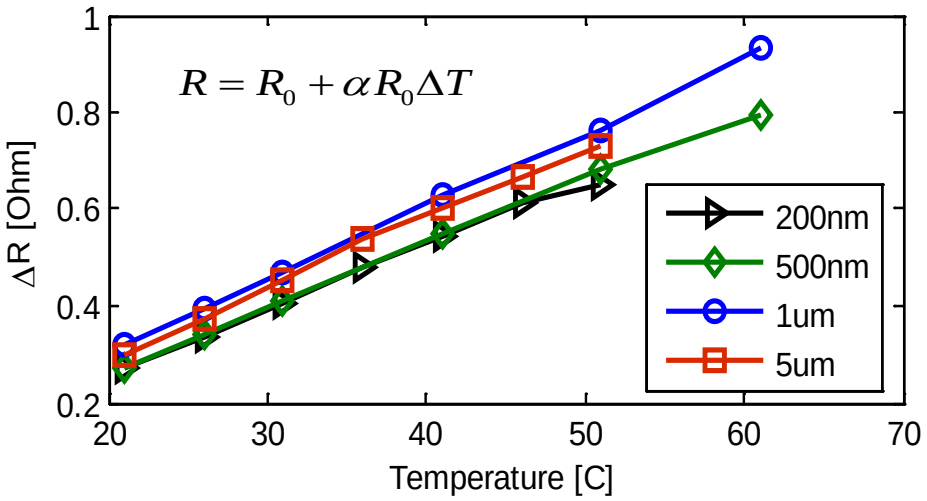


Figure 32. Calibration of TCR for four different heater widths. Due to the fabrication variations of the nanoheaters, the calibration process is performed before each measurement.

The sub-micrometer narrow heater makes it possible to confine the heat within a very shallow region with dc Joule heating. For a heater width of 50 nm, most of the heat is confined within a shallow layer of approximately 50-100 nm within which the heat is dissipated both vertically and laterally. This two-dimensional heat conduction

[4] Samples are fabricated by Dr. Takashi Kodama, Stanford University

is sensitive to the lateral thermal conductivity of this thin layer of material. On the other hand, wide heaters such as 5 µm induces nearly one-dimensional heat conduction across the thin layer on the top and is therefore only sensitive to the out-of-plane thermal conductivity of this layer as illustrated in Figure 33. The temperature rise of the heater bridge is captured by measuring the voltage drop across, and the temperature data is fitted using the multilayer heat diffusion code described in the previous section to determine the thermal properties of the underlying material.

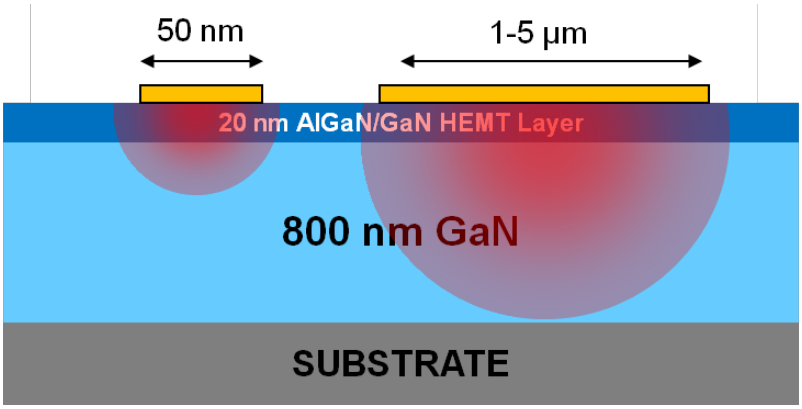


Figure 33. Spatial confinement by varying heater widths. Narrower heaters (50nm) confines the heat in a shallow layer on the top and is more sensitive to the lateral heat spreading, while wider heaters are less sensitive to the in-plane thermal conductivity of the 20 nm HEMT layer.

4.3.2 Thermal Conductivity Measurement of GaN Buffer Layer

We measured the thermal conductivity of GaN buffer layer using the sample in Figure 30. The thermal conductivity of SiNx is taken from an independent thermal reflectance measurement as one of the input parameter, and is verified in a subsequent measurement. TEM images indicate a GaN buffer layer that maintains isotropic heat conduction. Measurement result from 500nm heaters shows the thermal conductivity of GaN as 80 ± 10 W/mK which is consistent with heater widths from 200 nm to 1 µm

(Figure 34). Sources of uncertainty include fitting error and the variation in TCR due to uncertainty of the heater width. The thermal conductivity of GaN is constant from 30 to 80 ºC.

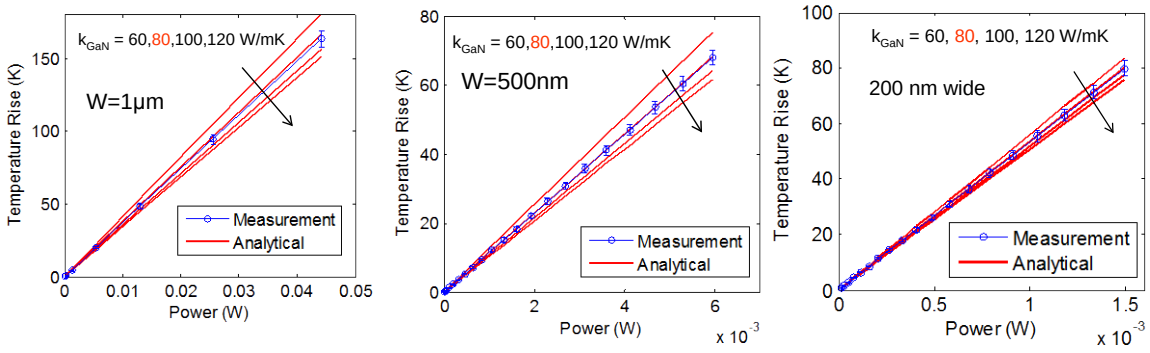
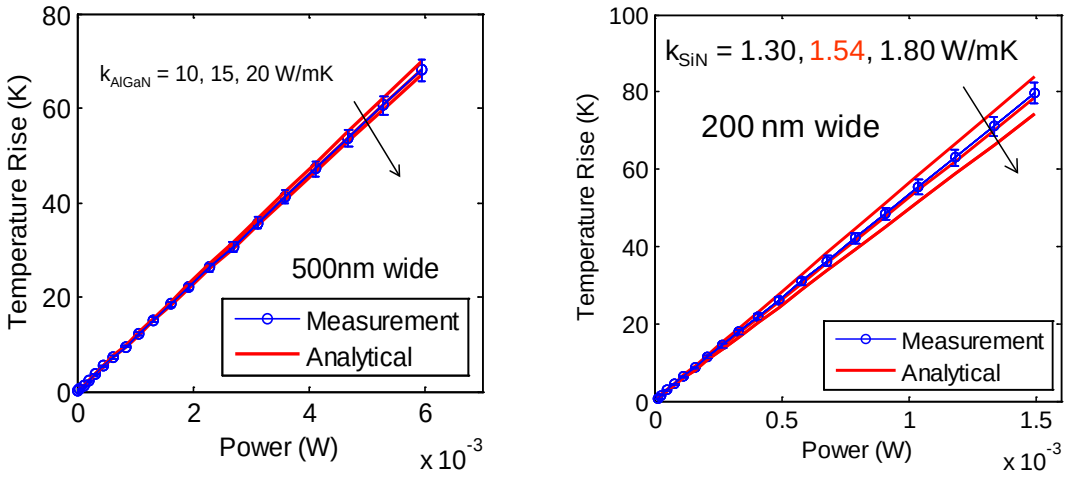


Figure 34. Parametric fitting of an analytical heat conduction model to the self-heating data for the heater bridge with width of 200, 500 and 1000 nm yield consistant results (~ 80 W/mK) for thermal conductivity of GaN buffer layer.

In this measurement, we have assumed that the 500 nm heaters are not sensitive to the bottom transition layers. This assumption is verified by contrasting the measurement results with simulation outcome while varying the thermal conductivity of the transition layer. Although the sensitivity increases with wider heaters due to deeper heat penetration, it is relatively low in our measurement with heater width of 500 nm as shown in Figure 35(a). Keeping other parameters constant, we change the thermal conductivity of AlGaN by ± 50% from 10 W/mK to 20 W/mK. The theoretical solution of the temperature rise does not change beyond the uncertainty bar of the measurement data. Therefore, the assumption of nanoheaters' low sensitivity to the bottom transition layer is valid in our measurement. We also verified the thermal conductivity of SiN using electrical technique. A narrow heater (200 nm) is used to confine the heat within the near-juntion reagion. We take the measured thermal conductivity of GaN (80 W/mK) as one of the input parameters and plot the simulated temperature rise again measurement data. The results from thermal reflectance, 1.54 W/mK, provides reasonably good fit as shown in Figure 35(b), and a more careful

fitting process finds the effective k_{SiN} as 1.42 ± 2.5 W/mK. Note that this is an effective value because we have lumped into the k_{SiN} all the TBRs which are small compared with the thermal resistance of the SiN layer itself.



(a) (b)

Figure 35. Verification of the assumptions made in the measurement. (a) Low sensitivity of the nanoheaters to the bottom transition layer. The theoretical temperature rises do not change beyond the uncertainty bar of the measurement data when varying k_{AlGaN} by ± 50%. (b) Cross check of the thermal conductivity of SiN using data from the DC Joule heating measurement. The value of 1.54 W/mK from thermal reflectance measurement achieves fairly good fit to the analytical solution.

4.3.3 GaN-Diamond Thermal Interface Resistance Measurement

More advanced GaN/AlGaN HEMT technology employs diamond substrate for more effective heat removal. The AlN nucleation and AlGaN transition layers add substantial thermal resistance between the GaN buffer and the diamond substrate. A 2nd generation HEMT sample eliminates the AlN nucleation layer and significantly reduces the AlGaN transition layer by 75% as shown in Figure 36. The thermal

resistance of the amorphous adhesion layer between AlGaN and the diamond substrate determines the effectiveness of HEMT heat removal and needs careful characterization. Using the nanoheaters with varying widths, we measured the thermal resistance of the overall multilayer stack and fitted the data with theoretical solution to deduce the thermal resistance of the adhesion layer. The results of two GaN-on-Diamond samples with slightly different layer thicknesses are complied in Table 3.

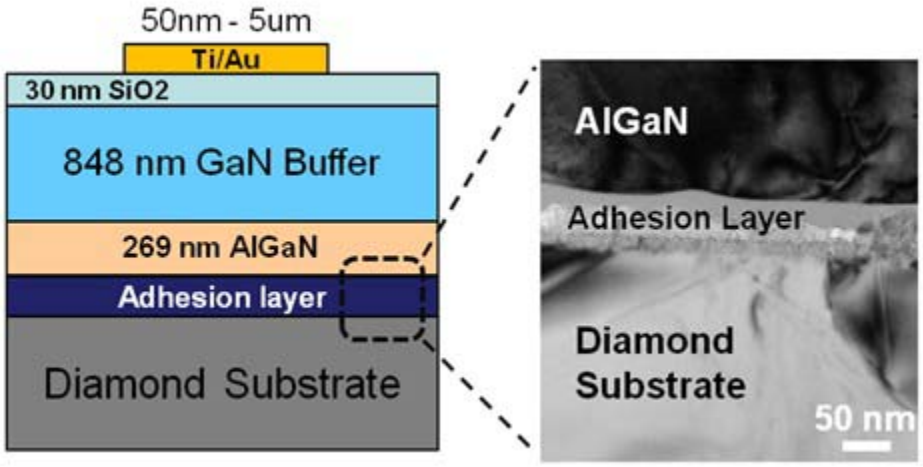


Figure 36. 2nd generation HEMT structure with removed AlN nucleation layer and much reduced transition layer thickness.

Table 3. Structures of 2nd Generation GaN-on-Diamond Samples and Thermal Resistance Data for the Adhesion Layer.

Sample Number	GaN thickness [nm]	AlGaN thickness [nm]	Adhesion layer thickness [nm]	Thermal resistance of adhesion layer [m^2K/GW]
A	828	142	3–42	25 ± 11
B	848	269	38–55	29 ± 12

4.4 Impact of Diamond Substrate on Near Junction Thermal Transport

4.4.1 HEMT Thermal Resistance Decomposition

The spatial temperature distribution of HEMT devices depends on the characteristic length scale of the heating source. Although the specific dimensions of current multi-finger HEMT devices vary, one can generally divide the characteristic length scales into three levels: the single gate or single-finger hot spot (below 1μm), the multi-finger pattern (1-100 μm), and the device package (above 100 μm). Due to the difference in characteristic length scales compared to the thickness of the underlying layers, the overall thermal resistance seen by each of these three levels differs significantly. This research investigates the thermal resistance decomposition of the HEMT multilayer stack, and quantifies their contributions to the overall temperature rise in the single-gate, multi-gate and package levels.

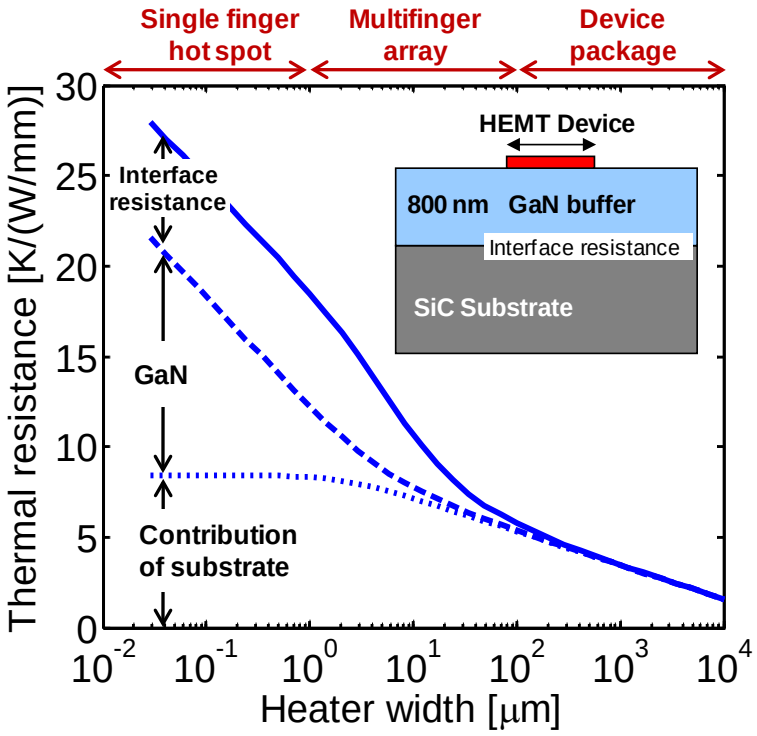


Figure 37. Thermal resistance decomposition. The GaN layer and thermal interface resistance are the major contributors to the total thermal resistance in the single-finger and multifinger length scales, while the substrate dominates in the package level.

For small devices with single gate length shorter than 1μm, two-dimensional heat spreading within the GaN buffer dominates the temperature rise of the hot spot in the channel region, as shown in Figure 37. The detailed description of our simulation approach is documented in our previous report, and we provide additional validation in the appendix. The volumetric thermal resistance of the GaN buffer accounts for 50-90% of the overall thermal resistance seen by a single gate. The thermal resistance of the substrate starts to be comparable to that of the GaN buffer in the multi-finger level and becomes dominant in the package level. The thermal interface resistance between the GaN buffer and the substrate also affects the average temperature rise in the multi-finger and single-finger scale, but becomes almost irrelevant in the package level. Therefore, a higher thermal conductivity GaN buffer helps reduce the peak

temperature in the hot spots below the gates, while a more thermally-conducting substrate lowers the average temperature of the overall HEMT package. Since the GaN buffer layer is fairly standard in all AlGaN/GaN-based HEMT devices, the following sections explore the more interesting impacts of the substrate.

4.4.2 Comparison between HEMT with SiC and Diamond Substrates

Conventional HEMT device consists of a GaN buffer layer on a SiC substrate with thermal conductivities ranging from 250 W/mK to 400 W/mK at room temperature. However, the high power density of HEMT devices demands even better heat conductor for the substrate in order to dissipate the excessive amount of heat. Therefore, diamond substrates draw great interest due to their extremely high thermal conductivity of approximately 1800 W/mK. Figure 38 compares the simulated temperature rise of a HEMT device on SiC and diamond substrates. Currently available technology requires an additional 1μm of AlGaN transition layer and AlN nucleation layer to mitigate the stress mismatch of the diamond substrate, while the thin nucleation layer (~10nm) between GaN and SiC can be either eliminated or modeled as an effective thermal boundary resistance (TBR). The diamond substrate results in a temperature rise that is about 4 times smaller than the SiC configuration in the package level (> 100 μm) even with the additional 1100nm transition and nucleation layers. However, at the single-gate (< 2 μm) and multi-gate (2-10 μm) dimensions, the diamond configuration generates higher temperature rises than SiC substrate. This is because the heat is mostly confined within GaN buffer and transition/nucleation layers, reducing the effectiveness of the substrate. The TBR between the substrate and the nucleation layer or the GaN buffer layer also influences the total temperature rise at the single-gate and multi-gate levels, as shown in Figure 38.

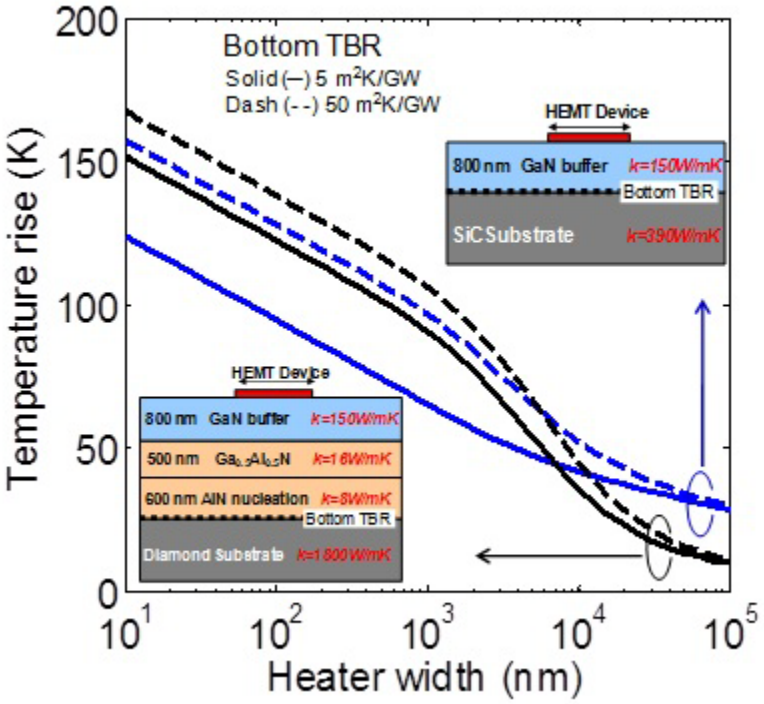


Figure 38. Comparison between SiC substrate and diamond substrate. Relevant TBRs are included in the simulation.

4.4.3 GaN-on-Diamond with and without Transition Layers

The relatively low thermal conductivities of AlGaN (~20 W/mK) and AlN (~7 W/mK) make them undesirable in a HEMT structure despite their roles in alleviating lattice mismatch stress. Figure 39 quantifies the benefits of removing the nucleation and transition layers on a diamond substrate. The removal of these layers further reduces the temperature for the singe-gate hot spot (< 1 μm) and multi-gate configuration (2-10 μm) by ~30 K for a heating power of 6 W/mm. The large characteristic length scale at the package level (> 50 μm) induces almost one-dimensional heat conduction through the layers into the substrate, therefore the performance remains unaffected by the absence of nucleation and transition layers.

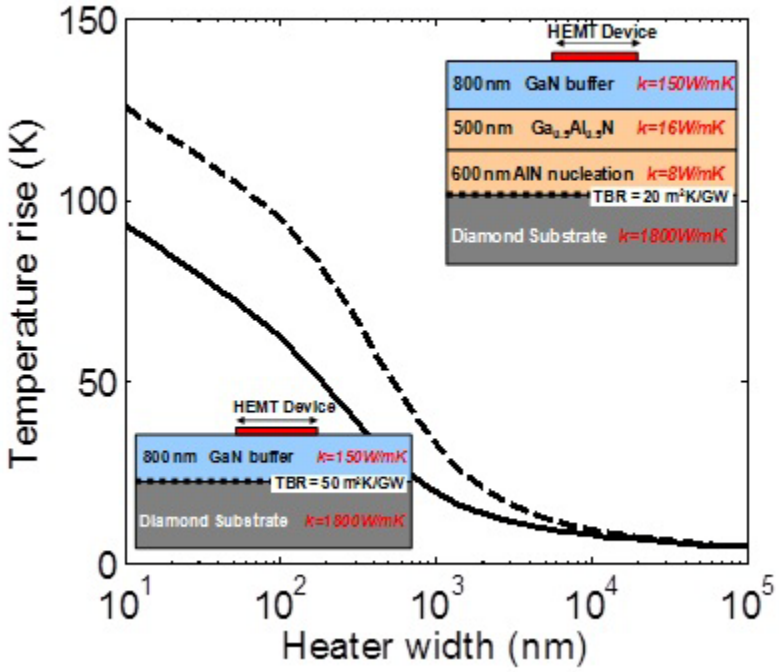


Figure 39. Performance improvement of the GaN-on-diamond configuration obtained by removing the GaAlN and AlN transition layers.

4.4.4 Target Value of GaN-Diamond Thermal Interface Resistance

The increasing power density of HEMT demands novel substrates, such as CVD diamond, that are more effective than SiC for heat extraction. Figure 40 compares the simulated temperature rises of a HEMT on SiC and diamond substrates and examines the impacts of a 1 μm transition layer. Diffuse mismatch model (DMM) yields the theoretical lower bounds of $TBR_{GaN\text{-}SiC}$ and $TBR_{GaN\text{-}diamond}$ as 1.3 m^2K/GW and 2.9 m^2K/GW, respectively. The simulation includes a thermal interface resistance of 50 m^2K/GW based on our measurements which accounts for both the TBR and the thermal resistance from any adhesion material. The diamond substrate results in a 70% lower temperature rise than that of the SiC in the package level even with the additional transitional layer. At the single finger and multifinger dimensions, however, the diamond substrate with a transition layer yields higher temperature rises

than the SiC does. This is because the heat is confined in the top layers and the relatively low thermal conductivity of the transition layer increases the GaN-diamond resistance significantly. Removing the transition layer further reduces the temperature rise of the diamond configuration by up to 52% as shown by the blue and red curves in Figure 40. A GaN-diamond thermal resistance below approximately 30 m^2K/GW allows the diamond configuration to outperform the SiC substrate in all the characteristic length scales.

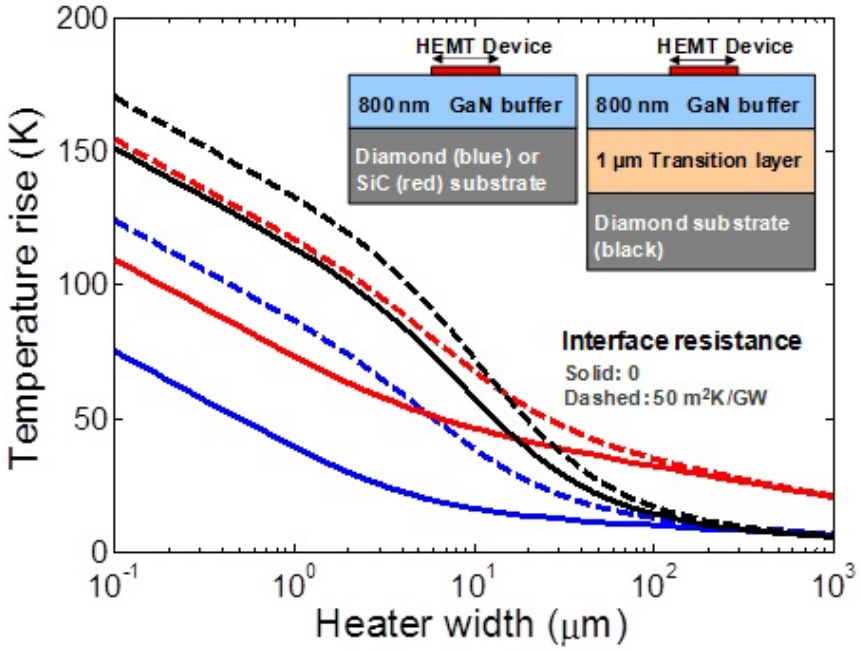


Figure 40. Simulated temperature rises of HEMT on SiC substrates (red), diamond with transition layer (black), and diamond without transition layer (blue) for a power dissipation of 6 W/mm. Inset: schematics of the HEMT structures. Figures are not drawn to scale.

4.5 Summary and Conclusions

This work measures the thermal conductivity of the GaN layer and the GaN-diamond interface resistance using metal bridges down to 50 nm wide. A numerical code calculates the temperature rise of the multilayer structure and reveals the individual contribution of each layer to the overall thermal resistance at the single-finger hop spot, multigate array, and device package length scales.

The thermal conductivity of the GaN buffer and the interface resistances govern the temperature rises of the AlGaN/GaN HEMTs in the single finger hot spots, while the substrate largely determines the averaged temperature rise on the multifinger and package level. Further advances in HEMT technology require novel substrates for more effective heat extraction. We predict that a diamond substrate outperforms one based on SiC due to its very high thermal conductivity, though the presence of a typical GaN-diamond interface resistance significantly impedes the near junction thermal transport and should be either removed or reduced.

Chapter 5: Ultrathin Mo/Si Multilayers

5.1 Heat Transfer in Metal/Semiconductor Multilayers

Heat conduction across metal interfaces with dielectrics and semiconductors governs the behavior of many nanostructured materials and devices. Past research observed the importance of interface resistance in metal/dielectric multilayers with periods of a few nanometers such as W/Al_2O_3 thermal barrier coating [32] and Ta/TaO_x tunnel junctions. [35] Conduction normal to these interfaces is complicated by thermal energy conversion between electrons and phonons near and at the interface. This conversion facilitates the lowest possible thermal resistance because phonons are the dominant heat carriers in dielectrics and most semiconductors, while electrons are the dominant heat carriers in metals. Extensive research has been performed on the metal-dielectric interface thermal resistances for the situation where the metal region is thick compared to the carrier free paths, which justifies the assumption that the energy conversion is complete and the dominant carrier types on each side are fully responsible for conduction. [16, 17, 22, 155, 156] However, there are a variety of applications in which the small thickness of the metal film inhibits the electron-phonon coupling and, we argue in this work, can render phonons the dominant heat conductor in the direction normal to the metal film. One example is Mo/Si multilayers with ~ 7 nm period, which serve as mirrors in extreme ultraviolet (EUV) and soft x-ray optics. [157] Heat conduction in these mirrors can strongly influence performance and reliability due to thermally induced stress and atomic diffusion between Mo and Si thin films. [158, 159]

This work makes progress on the modeling and experimental investigation of the complex electron and phonon transport and interaction processes in metal/dielectric multilayers with metal thickness below the electron and phonon mean free paths. We use frequency-domain thermometry to measure the in- and cross-plane thermal conductivities of a Mo/Si multilayer sample with 6.9 nm period. Thermal conduction

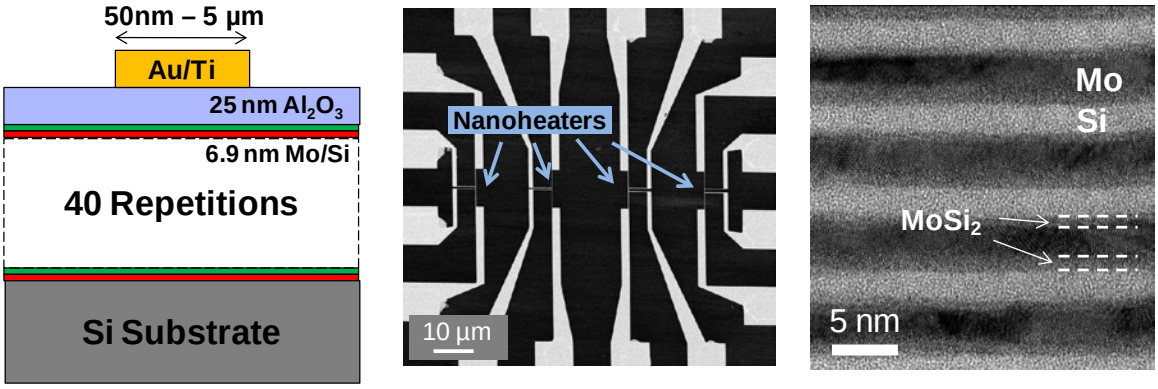
in such multilayers is influenced by phonon-phonon coupling across the interface [17], quasi-ballistic phonon transport across the metal layer, the electron-phonon nonequilibrium in the metal film [22, 160, 161], and the possibility of significant inelastic electron-interface scattering [16]. Electron-phonon nonequilibrium has been a common theme for decades in ultra-short pulsed laser heating experiments on metals [14, 16, 38, 162], but the potential for strong steady-state nonequilibrium has received relatively little attention. In this work we show that ultra-thin metal films spatially amplify the relevance of near-interfacial nonequilibrium in the steady state, which suppresses the electron contribution to conduction in the film-normal direction and renders phonons the dominant heat carriers.

5.2 Anisotropic Thermal Conductivity Measurement

5.2.1 Mo/Si Multilayer Sample Preparation

Multilayers consisting of 40 Mo/Si bilayers with a period thickness of 6.9 nm are deposited by DC magnetron sputtering. The ratios of the Mo layer thickness to the bilayer period studied here include Γ = 0.4 and 0.6. These values are selected based on the practical requirement of optimal reflectivity in the EUV mirror applications. [157, 158, 163] Preliminary sheet resistance measurements suggest a highly conductive surface of the Mo/Si stack, which motivates the use of a dielectric layer to achieve insulation from the metal heaters on top. An amorphous Al_2O_3 layer is sputtered to provide electrical insulation as shown in the schematic in Figure 41(a). The gold nanoheaters varying in width from 50 nm to 5 μm as shown in Figure 41(b) are patterned by electron-beam lithography on the same sample to minimize sample-to-sample variation. A titanium film of 5 nm enhances the adhesion between gold and the insulation layer. The transmission electron microscope (TEM) image in Figure 41 (c) shows the structural detail of the multilayers and thin films of $MoSi_2$ at the interfaces due to natural atomic diffusion during fabrication. The same fabrication process was utilized to prepare a reference sample with the Al_2O_3 but without Mo/Si multilayers in order to separate the substrate/insulator and Mo/Si contributions to the

measured thermal resistance. The Mo/Si multilayers maintain thermal stability at relatively low temperatures (25-100 ºC), [164] although interdiffusion between Mo and Si films can become a critical concern at higher temperatures and will be the subject of future thermal conduction studies [158].



(a) (b) (c)

Figure 41. Mo/Si multilayer sample and nanoheater patterns. (a) Schematic of the 40 repetitions of Mo/Si multilayer. (b) Scanning electron microscope (SEM) image of the e-beam patterned Au nanoheaters with width ranging from 50 nm to 5 µm (not all widths are shown in the graph). (c) Transmission electron microscope (TEM) image of the Mo/Si multilayer. A thin $MoSi_2$ layer of 0.5~1.2 nm is formed between Mo and Si due to atomic diffusion.

5.2.2 Measurement and Results

Metal heaters of widths varying from 50 nm to 5 µm extract the in-plane and cross-plane thermal conductivities of the Mo/Si multilayers by the 3ω technique. [25, 46] A driving AC current at frequency ω generates Joule heating and temperature oscillation in the heater at frequency 2ω. The linear relationship between temperature and the electrical resistivity of gold over the temperature range of this experiment

creates a third harmonic component in the voltage across the heater. This 3ω voltage component is governed in part by the thermal conductivity of the underlying Mo/Si layer. Heaters as wide as 5 μm induce nearly one-dimensional heat conduction through the Mo/Si multilayer and are therefore more sensitive to the cross-plane thermal conductivity, whereas heaters narrower than 200 nm are more suitable for capturing the in-plane heat spreading through the multilayers.

By modeling the 40 repetitions of the Mo/Si multilayers as a single layer with anisotropic thermal conductivity, the average temperature rise ΔT at the surface of a multilayer system can be derived as [165]

$$\Delta T = \frac{P}{2\pi L b^2} \int_0^\infty \frac{B^+(m) + B^-(m)}{B^-(m)A^+(m) - B^+(m)A^-(m)} \frac{\mathrm{sinc}^2(mb)}{k_{n,z}\gamma_n m^2} dm \tag{29}$$

$$\gamma_n = \sqrt{\eta_n m^2 + i\omega / D_n} \tag{30}$$

where P, L and b are the heating power, length and width of the heater, respectively. The dimensionless terms $A^+(m)$, $A^-(m)$, $B^+(m)$, and $B^-(m)$ are determined by a recursive matrix procedure developed by J. H. Kim *et al.* [165] The parameters $k_{n,z}$, η_n, and D_n are the cross-plane thermal conductivity, anisotropy ratio (k_x/k_z, where x and z denote in-plane and cross-plane directions, respectively), and thermal diffusivity of the n^{th} layer, respectively. Numerical solutions of (29) and (30) demonstrate that the temperature rise is most sensitive to the thermal conductivity anisotropy ratio when the heater width is small compared to the film thickness. However, the narrowest heater (50 nm) in this study yields suboptimum sensitivity to the thermal conductivity anisotropy because the heat is largely confined within the 25 nm Al_2O_3 insulation layer before penetrating into the Mo/Si multilayers. In the frequency domain, the 3ω measurement is carried out with an AC driving current between 1 kHz and 20 kHz, a frequency range where the characteristic thermal diffusion depth is larger than the Mo/Si film thickness while still preserves the substrate as semi-infinite medium.

The measured temperature rises from different heater widths capture the thermal conductivity anisotropy of the Mo/Si multilayer system. Because even the widest

heater cannot completely eliminate the lateral heat spreading, simultaneous fitting of all the temperature data obtained from available heater widths from 50 nm to 5 μm provide redundancy and improve the accuracy of the conductivity magnitudes. Figure 42 (a) plots the measured reduced temperature rise, which is the surface temperature rise divided by the heat flux, and the theoretical fit for varying heater widths. The thermal conductivity of the Al_2O_3 film is measured independently with a reference sample (25 nm Al_2O_3 on Si substrate) as k_{Al2O3} = 3.66 ± 0.16 W/mK, which is consistent with previous work [166, 167] and much lower than the bulk crystalline value owing to material disorder. The experimental uncertainty is governed by those of the temperature coefficient of resistivity (TCR) of the gold heaters as well as the parameter variations that are possible in the data fitting process. Solutions of (29) and (30) using the measured Mo/Si anisotropic thermal conductivity data simulate the surface temperature rises, which are normalized to the isotropic case, as shown by the solid curves in Figure 42 (b). The thermal conductivity anisotropy ratios $\eta = k_x / k_z \approx$ 13 are consistent among all the heater widths considering the uncertainty bars. Varying the Mo thickness ratio Γ between 0.4 and 0.6 is expected to have negligible effect on η because the cross-plane thermal conduction is dominated by the interface resistance. Table 4 compiles the measured thermal conductivity data for multilayers with Γ = 0.4 and Γ = 0.6, together with the theoretical calculations from the following sections.

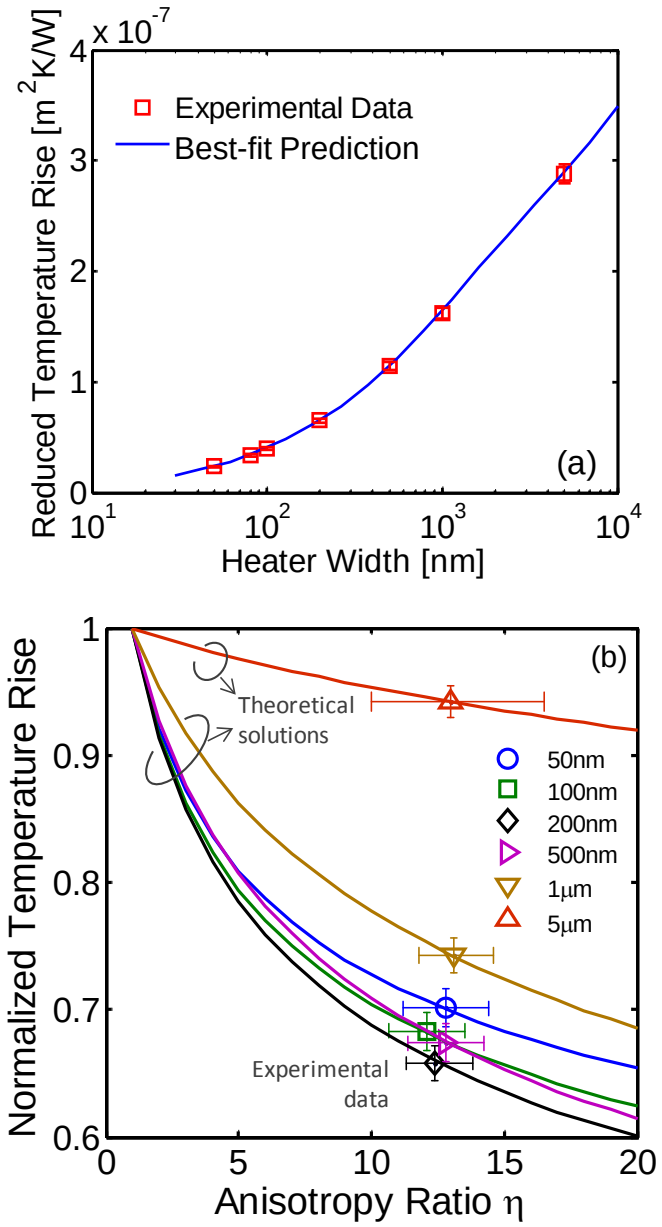


Figure 42. Electrical thermometry data and comparison with best-fit predictions for the Mo/Si multilayer with Mo thickness fraction of $\Gamma = 0.4$. (a) Reduced temperature rise for different heater widths. (b) Thermal conductivity anisotropy ratio $\eta = k_x/k_z$ is measured with multiple heater widths. The measured anisotropy ratio (~13) is consistent among all the heater length scales

Table 4. Effective cross-plane thermal conductivities of two multilayer samples with different Mo thickness fraction ($\Gamma = d_{Mo}/d_{total}$). Theoretical calculations agree with the measurement data.

Mo thickness fraction Γ	d_{total} [nm]	d_{Mo} [nm]	d_{Si} [nm]	$k_{z,model}$ [W/mK]	$k_{z,measurement}$ [W/mK]
0.4	6.9	2.8	4.1	1.30	1.2 ± 0.1
0.6	6.9	4.1	2.8	1.49	1.4 ± 0.1

5.3 Thermal Modeling of Metal/Dielectric Multilayers

The goal of the model developed here is to capture the effects of a variety of complex electron and phonon transport phenomena in thin metal films bounded by dielectrics, especially near and at the metal/dielectric interface. While there are major approximations involved, the purpose is to introduce the dominant physical mechanisms and provide an estimate of their relative importance. Phonon-phonon transmission and scattering at interfaces is estimated here using the diffuse mismatch model (DMM). [17, 31] Electron energy exchange with phonons within the metal is captured using a two-temperature model (TTM) and a conductance G between the two carrier types. [22, 24, 37] Electrons may scatter inelastically at the metal-dielectric interface and interact directly with the phonon system across the interface through an electron-interface conductance. [38] A consequence of the extra resistances imposed on electron transport normal to the metal films is that phonon heat conduction, usually negligible in metals, can become the dominant mechanism. The following sections investigate the contributions of these mechanisms to the overall cross-plane thermal resistance.

For a heat flux perpendicular to the multilayer surface, the overall thermal resistance consists of both the volumetric thermal resistance of each layer and the thermal boundary resistance at each interface. This approach neglects the thin $MoSi_2$

layers at the interfaces due to atomic diffusion. The cross-plane thermal resistance of one period of the Mo/Si multilayer, $R_{Mo/Si}$, is therefore approximated using

$$R_{Mo/Si} = \frac{d_{Mo} + d_{Si}}{k_{eff,z}} = R_{Mo} + R_{Si} + R_{b,Mo-Si} + R_{b,Si-Mo} = \frac{d_{Mo}}{k_{Mo,z}} + \frac{d_{Si}}{k_{Si,z}} + \frac{1}{h_{B,Mo-Si}} + \frac{1}{h_{B,Si-Mo}} \quad (31)$$

where d_{Mo} and d_{Si} are the individual thicknesses of the Mo and Si layers, respectively. The effective cross-plane conductivity $k_{eff,z}$ describes the Mo/Si multilayer, while $k_{Mo,z}$ and $k_{Si,z}$ are the cross-plane thermal conductivities of each layer considering the thin film size effects. [11] The thermal boundary conductance h_B between a metal and dielectric is related to electron-phonon nonequilibrium, and the electron-interface inelastic scattering.

5.3.1 Electron-Phonon Nonequilibrium

The two-temperature model (TTM) is traditionally used to describe the electron-phonon nonequilibrium in \the metal layer near the metal-semiconductor interface. [22, 160] Electron and phonon temperatures deviate from each other in the near-interface region, often referred to as the cooling length [18], causing electrons to lose energy to phonons which then carry the heat across the interface into the dielectric medium. For steady-state heat flow across the film, the energy balance in the metal can be expressed as

$$k_e \frac{\partial^2 T_e}{\partial z^2} - G\left(T_e - T_p\right) = 0; \quad k_p \frac{\partial^2 T_p}{\partial z^2} + G\left(T_e - T_p\right) = 0 \quad (32)$$

where T is temperature, and the subscripts e and p denote electron and phonon, respectively. The electron-phonon coupling coefficient G can be derived from the rate of electron-phonon energy exchange considering an electron density of states (DOS) applicable at room temperature: [14, 168]

$$G(T_e - T_p) = \left.\frac{\partial E_e}{\partial t}\right|_{ep} = \frac{4\pi}{\hbar}\sum \hbar\omega_Q \left| M_{kk'} \right|^2 \left[S(k,k') \right] \delta\left(\varepsilon_k - \varepsilon_{k'} + \hbar\omega_Q \right) \tag{33}$$

where E_e is electron energy and ω is the phonon frequency. The electron and phonon wave numbers are denoted as k and Q, respectively, and the electron-phonon scattering matrix $M_{kk'}$ describes the probability of electron scattering from state k to state k'. The thermal statistical factor $S(k,k') = (f_k - f_{k'})\, n_Q - f_{k'}\,(1 - f_k)$ relates the phonon absorption and emission processes to the electron distribution f_k and phonon distribution n_Q. Using the Fermi-Dirac and Bose-Einstein distributions for the electron and phonon systems, respectively, Eq. (5) can be simplified as

$$\left.\frac{\partial E_e}{\partial t}\right|_{ep} = 2\pi g(\varepsilon_F) \int_0^\infty \alpha^2 F(\varepsilon, \varepsilon', \Omega) (\hbar\Omega)^2 \left[n(\Omega, T_p) - n(\Omega, T_e) \right] d\Omega \tag{34}$$

where $g(\varepsilon_F)$ is the electron DOS at the Fermi level, and $\alpha^2 F(\varepsilon, \varepsilon', \Omega)$ is the electron-phonon spectral function.[168] Near room temperature, it is reasonable to assume the independence of $\alpha^2 F$ with respect to ε and ε', since only the states near the Fermi energy ε_F are involved in electron-phonon scattering. Thus, the electron-phonon couple parameter can be computed using[14, 169]

$$G = \frac{\pi\hbar k_B \lambda \langle \omega^2 \rangle}{g(\varepsilon_F)} \int_{-\infty}^{\infty} g^2(\varepsilon) \left(-\frac{\partial f}{\partial \varepsilon} \right) d\varepsilon \approx \pi\hbar k_B g(\varepsilon_F) \lambda \langle \omega^2 \rangle \tag{35}$$

where λ is the electron-phonon mass enhancement parameter[170] and $\langle \omega^2 \rangle$ is the McMillan Factor for the second moment of the phonon spectrum.[171] The last approximation is based on the fact that $-\partial f/\partial \varepsilon \approx \delta(\varepsilon - \varepsilon_F)$ at room temperature. Using the approximate relation $\langle \omega^2 \rangle \approx \theta_D^2 / 2$, [171, 172] the mass enhancement parameter $\lambda_{Mo} = 0.42$, [173, 174] and the electron DOS at Fermi level of 0.61 states/(eV·cell), [174] the above equation yields $G = 1.2\times10^{17}$ W/m^{3}K for Mo at room temperature.

The thermal conductance across the Mo/Si interface, $h_{B,Mo\text{-}Si}$, can be derived using the method proposed by Majumdar and Reddy[22] as

$$h_{B,Mo-Si}^{-1} \approx \frac{1+\sqrt{Gk_{p,Mo}}\,/\,h_{pp,Mo-Si}}{\sqrt{Gk_{p,Mo}}} = h_{ep}^{-1} + h_{pp,Mo-Si}^{-1} \tag{36}$$

where $k_{p,Mo}$ is the phonon thermal conductivity of Mo. This equations uses a serial connection of the thermal resistances from electron-phonon nonequilibrium (R_{ep} = $1/h_{ep}$) and interface phonon scattering (R_{pp} = $1/h_{pp,Mo\text{-}Si}$). The diffusive mismatch model (DMM) evaluates the phonon-phonon conductance h_{pp} and is discussed in more detail in the Supporting Information. Equation (8) assumes that the electron and phonons are in equilibrium far away from the interface. One problem with this assumption arises when the Mo film thickness becomes close to the electron cooling length, L_c = $[Gk_{Mo}/(k_{Mo,e}k_{Mo,p})]^{1/2}$ = 1.4 mn,[18] resulting in strong electron-phonon nonequilibrium and incomplete convergence of T_e and T_p. We have performed numerical simulations using the phonon Boltzmann transport equation yielding thermal resistance comparable with that predicted by the TTM for the 2.8 nm film thickness, with a difference less than 30%. Therefore, the TTM provides reasonable estimates of the electron-phonon nonequilibrium for the thicknesses our Mo/Si multilayers. More details on the comparison are provided in the Supporting Information.

5.3.2 Direct Phonon Transmission

Phonons in polycrystalline metal films can conduct heat by traveling directly across the film, either ballistically or impaired by scattering predominantly with each other and with defects, without transferring significant energy to the electron system. Although this conduction path is usually negligible in thick metal films due to the small phonon thermal conductivity [14], the extra burden of electron-phonon energy exchange imposed on the electron system can render direct phonon conduction the dominant mechanism. In our Mo/Si multilayer samples, the direct phonon transport path experiences a thermal resistance R_p = $d_{Mo}/k_{p,Mo}$ which is in parallel with the electron path R_e as shown in Figure 43 (a).

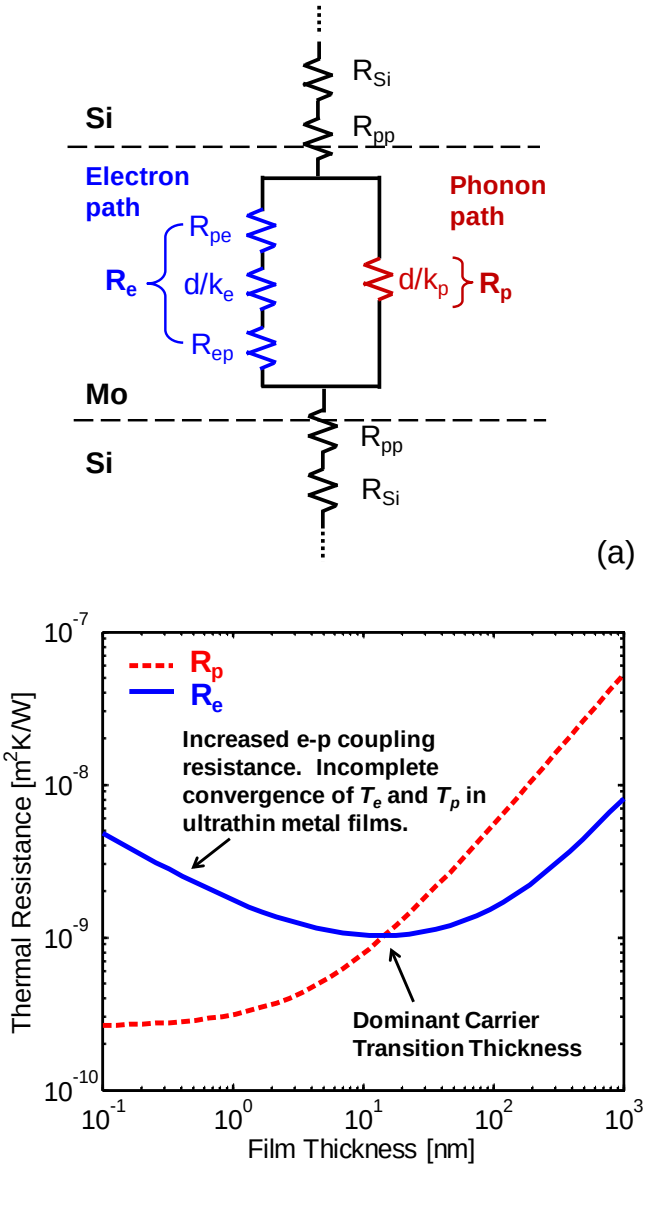


Figure 43. Thermal resistances in the Mo/Si multilayer system. (a) Approximate thermal resistance network model where the conduction in the Mo layer consists of a parallel of the electron path and the phonon direct transmission path. (b) Theoretical calculation result shows that the thermal resistance of the phonon path (R_p) becomes smaller than the electron path (R_e) for a metal film thickness of less than d_{trans} = 14 nm.

The phonon thermal conductivity of Mo can be estimated by:

$$k_{p,Mo} = \frac{1}{3}(C_v v \lambda)_p , \tag{37}$$

where C_V is the volumetric phonon heat capacity estimated using the Debye approximation [11], v is the speed of sound, and λ is the phonon mean free path in Mo which takes into account the thin film size effect. Although the spatial confinement from the thin film thickness can modify the phonon properties such as group velocity, polarization, density of states, etc, this expression provides an estimate of k_p when taking the size effect into the calculation of λ through Matthiessen's rule. [11] Figure 43 (b) shows that R_p monotonically decreases with decreasing Mo thickness and crosses R_e at a "Dominant Carrier Transition Thickness" which can be derived as $d_{trans} = 2k_e k_p / [\sqrt{G k_p}(k_e - k_p)]$. The phonon path starts to dominate the heat conduction in ultrathin films below d_{trans}. The overall thermal resistance of a single Mo/Si repetition now becomes:

$$\begin{aligned} R_{Mo/Si} &= \frac{d_{Mo} + d_{Si}}{k_{tot,z}} = R_{Mo} + R_{Si} + R_{b,Mo-Si} + R_{b,Si-Mo} \\ &= \frac{d_{Si}}{k_{Si,z}} + \left(R_e \parallel R_p\right) + \frac{1}{h_{pp,Mo-Si}} + \frac{1}{h_{pp,Si-Mo}} \end{aligned} \tag{38}$$

5.3.3 Inelastic Electron-Interface Scattering

The TTM discussed earlier assumes a diffusive process in which the electrons reflect elastically off the interface and eventually thermalize the phonons in the metal side. However, the electrons can also scatter inelastically at the interface and exchange energy with the phonon system in the dielectric. This creates an additional path for thermal transport which is more important when the metal film thickness is close to or less than the electron mean free path, although it was largely ignored in the

previous modeling of ultrathin metal/dielectric multilayers. [32, 34, 35] Past experiments have shown evidence of the inelastic heat loss from a metal film to a dielectric using the transient thermoreflectance (TTR) technique. [37-39] Several theoretical models also made effort to quantify the inelastic thermal conductance including the inelastic phonon radiation limit theory [40], the maximum transmission model [41], and the anharmonic inelastic model. [42] These methods either provide a strict upper limit for the interface conductance or require the detailed dispersion relationship. In this work we employ the model developed by Sergeev [43, 44] which uses a quasi-analytical approach combined with experimental data. The thermal boundary conductance due to inelastic electron-interface scattering can be written as:

$$h_{ei} = \frac{\pi^4}{10}\frac{g(\varepsilon_F)T^3}{p_F^2}\left(\frac{\beta_l}{v_l} + 2\frac{\beta_t}{v_t}\right)J\left(\frac{T}{\theta_D}\right) \tag{39}$$

where θ_D is the Debye temperature, p_F is the Fermi momentum, $g(\varepsilon_F)$ is the electron DOS at the Fermi level, and v_l and v_t are the longitudinal and transverse sound velocities, respectively. The integral term $J(y) = -(15/4\pi^4)\int_0^y x^4 \nabla N(x)dx$ expands the formula into the high temperature regime. The interaction constants of electrons with longitudinal and transverse phonons, β_l and β_t, are determined by fitting the experimental data of Nb films as in Table 5. [43] Since Nb and Mo have nearly the same electron orbital behavior and electronic band structures [175], we assume the electron scattering parameters of Mo are similar to those of Nb. Future measurements on the temperature-dependent electrical resistivity of Mo film will provide more accurate β_l and β_t. The inelastic electron scattering at interface adds another conduction path in parallel to the electron and phonon paths in a more complex fashion as in Figure 44. A portion of the electrons in the Mo layer transfer their energy through electron-phonon coupling resistance R_{ep} (by TTM) and subsequently the phonon boundary resistance R_{pp}, while the other electrons can scatter inelastically at the Mo-Si interface and lose energy to the Si lattice through R_{ei}. The effective cross-plane thermal conductivities of the Mo/Si multilayers computed from this model

agree reasonably well with the experimental data for various thickness ratios (d_{Mo}/d_{total}) as shown in Table 4.

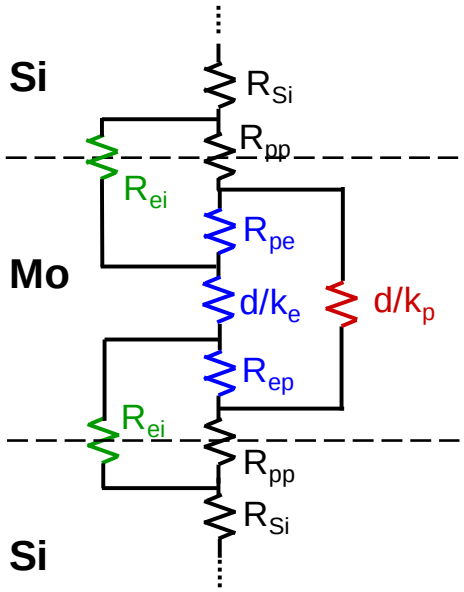


Figure 44. Complete thermal resistor network of the metal-semiconductor multilayers. Three physical mechanisms are included: electron-phonon nonequilibrium (R_{pe} and R_{ep}), direct phonon transport (d/k_p), and inelastic electron-interface scattering (R_{ei}).

Table 5. Material properties of molybdenum used in the calculation

v_l [10^3 m/s]	v_t [10^3 m/s]	v_F [10^6 m/s]	β_t	β_t	τ_e [10^{-15} s]
6.25	3.35	1.7	10	35	3.80

The interaction constants β_l and β_t are obtained by fitting the data of Nb films.[43] The Fermi velocity v_F and electron relaxation time τ_e of Mo are taken from reference [176].

5.4 Summary and Conclusions

In conclusion, for heat conduction normal to dielectric/metal interfaces, nonequilibrium between electrons and phonons prevails in the metal near the interface within a distance comparable to the phonon mean free path. In metal/dielectric multilayers in which the metal film thickness is only a few nanometers, the direct phonon conduction across the thin metal layer can present a dramatically more effective heat transfer path than the electron conduction path that dominates in thicker metals. By comparing the electron and phonon resistances developed in the network model in Figure 43(a), an approximate transition thickness $d_{trans} = 2k_p k_e / [\sqrt{G k_e k_p}(k_e - k_p)]$ can be extracted for the transition from electron to phonon dominated conduction. This criterion neglects the interface scattering and temperature dependence of the conductivities, but captures the main physical arguments developed here. As the metal film thickness shrinks below the electron mean free path, more electrons can travel ballistically and scatter inelastically at the metal-dielectric interface, adding another energy transfer path from the electron system in the metal to the phonon system in the dielectric. The thermal network model (Figure 44) considers all three conduction paths: the electron-phonon nonequilibruim (R_{ep} and R_{pe}), direct phonon transport (R_p), and inelastic electron-interface scattering (R_{ei}). The theoretical calculations agree with the measured thermal conductivities of two Mo/Si multilayers samples with period of 6.9 nm and Mo layer thickness fractions of 0.4 and 0.6. A more rigorous study based on the electron-phonon coupled, two-dimensional Boltzmann transport equation may provide a more detailed view of the multiple conduction mechanisms and their relative strengths.

Chapter 6: Concluding Remarks

6.1 Summary of Dissertation

This thesis studies the thermal transport phenomena in nanostructured semiconductor devices and materials by means of measurement, numerical simulation, and theoretical modeling. This work contributes to the fundamental understanding of electron-phonon couple heat conduction at the material interfaces which is becoming increasingly important in a variety of modern nanodevices. The measurement and simulation techniques developed here facilitate more accurate thermal characterization of nanostructured materials and analysis of a variety of nanodevices including the phase change memory (PCM), the high electron mobility transistors (HEMT), and the Mo/Si multilayers for extreme ultraviolet mirrors.

This work presents the in-plane thermal conductivity measurement of $Ge_2Sb_2Te_5$ (GST) films suspended in a microfabricated structure for the amorphous (a-GST), face-centered cubic (f-GST) and hexagonal close packed (h-GST) phases. The unique design of free-standing GST films eliminates the out-of-plane heat loss to the substrate and achieves high sensitivity to lateral heat conduction. The out-of-plane thermal conductivities are measured by using the 3ω technique. The in-plane thermal conductivity is found to be 60%~80% of the out-of-plane value for the crystalline phases while no anisotropy is observed for the amorphous phase. The anisotropic thermal conductivity of the crystalline phase of GST is attributed to the phase impurities at grain boundaries. This work models the anisotropy using effective medium arguments, lends further support to the hypothesis that phase impurities are responsible for the anisotropy. Thermal conduction strongly influences the programming energy and speed in PCM devices. Electrothermal simulations predict that the reduced in-plane conductivity will allow closer spacing of lateral-cell devices and reduce the reset programming current by 20-30%.

Electrothermal transport and crystallization dynamics govern the speed and bit stability of multibit PCM. This work develops a transient simulation methodology incorporating electrical, thermal, and phase transition models to investigate multibit PCM cell structures and programming strategies. The simulations evaluate two standard PCM structures, the mushroom cell and the confined pillar cell, with feature sizes smaller than 40 nm. The transient simulation captures the phase distribution and cell resistance profile, which are corroborated by transmission electron microscope imaging and the corresponding measured resistance values. This work also explores a more compact architecture, the stacked vertical cell, with precise control of the Joule heating and potentially more stable intermediate resistance levels. For an electrode area of 10 nm × 20 nm, a low programming current of 60 μA – 90 μA generates sufficient heating power to amorphize the phase change elements sequentially, resulting 4 distinct resistance levels distributed over a 2-order-of-magnitude resistance range with promise for multibit storage.

This research extends the thermal characterization and modeling techniques to the GaN HEMT devices with diamond composite substrate. The power density that can be handled by GaN HEMT devices is limited by substrate thermal resistances. Substrates containing high-thermal-conductivity diamond can help, but these composites require careful attention to thermal resistances between the GaN and diamond. The single gate hot spot (~1μm), multifinger pattern (1-100μm), and the device package (>100μm) represent three distinct characteristic length scales whose thermal resistances are dominated by different components in the HEMT multilayer structure. This work also measures the thermal conductivity of the GaN layer and the GaN-diamond interface resistance using metal bridges down to 50 nm wide. A numerical code calculates the temperature rise of the multilayer structure and reveals the individual contribution of each layer to the overall thermal resistance at the above-mentioned three characteristic length scales. The results show that diamond composite substrates can reduce the temperature rise by ~33% for single- and multifinger heating, and ~70% for package level heating, compared to a composite silicon carbide substrate. This work shows that a GaN-diamond thermal resistance

below ~30 m^2K/GW will be required for sustained power density improvements in HEMT technology.

This work also makes progress to the fundamental understanding of electron-phonon coupled thermal conduction at and near metal-dielectric or metal-semiconductor interfaces. Measurements use the 3ω method with six different bridge widths down to 50 nm to extract the in- and cross-plane effective conductivities of Mo/Si (2.8 nm/4.1 nm) multilayers, 15.4 and 1.2 W/mK, respectively. Thermal conduction in such periodic multilayer composites can be strongly influenced by nonequilibrium electron-phonon scattering for periods shorter than the relevant free paths. This work identifies two additional mechanisms – quasi-ballistic phonon transport normal to the metal film and inelastic electron-interface scattering – that can also impact conduction in metal-dielectric multilayers with period below 10 nm. Phonon conduction across the thin metal layer can become the more effective than the electron conduction path in ultrathin metal films with thickness of only a few nanometers. As the metal film thickness shrinks below the electron mean free path, more electrons can travel ballistically and scatter inelastically at the metal-dielectric interface, adding another energy transfer path from the electron system in the metal to the phonon system in the dielectric. Therefore, the overall heat conduction in the multilayers is expected to involve three conduction paths: the electron-phonon nonequilibrium, the direct phonon transport, and the inelastic electron-interface scattering. Theoretical calculations incorporating these mechanisms agree with the measured thermal conductivities of two Mo/Si multilayers samples with period of 6.9 nm.

6.2 Suggestions for Future Work

6.2.1 Compositional diffusion in chalcogenide materials for PCM

One major concern of PCM is its durability of resistance values for the “set” and “reset” states under repetitive programming cycles [1, 3, 177-180]. Many of the

failure modes in GST may originate from the compositional migration or diffusion of the atomic species, and past research has shown that all the species, Ge, Sb and Te, drift after a certain number of programming cycles [123, 179, 181, 182]. A thorough understanding of the GST compositional diffusion is critical for improving reliability. Since a PCM device is under both thermal and electrical stress during operation, it is reasonable to investigate the relationship between repetitive thermal and/or electrical stress and the compositional diffusion of GST.

Thermally-induced diffusion of GeSbTe species results from the incongruent melting of GeSbTe. Based on the pseudo-binary phase diagram, incongruent melting between Sb_2Te_3 and GeTe can result in the phase separation of GST into a Sb- and Te-rich liquid phase and a Ge-rich solid phase [182]. Incongruent melting drives the Sb, Te-rich liquid phase to diffuse into completely melted GST liquid, causing the active region to be Sb, Te-rich. The suspended structure can be used to test this theory by imposing a large, linear and repetitive temperature gradient on the suspended GST membrane while eliminating any electrical field. The quantitative relationship between thermal stress and compositional migration can be determined with TEM-electronic dispersion spectroscopy (TEM-EDS) analysis, and the suspended thin membrane on the suspended structure is readily compatible with TEM characterization. A detailed theory regarding the physics of compositional diffusion in GST can then be developed and verified by the experimental data.

Electrically induced diffusion has shown that GST species migrate toward the cathode, leaving a mass depletion area near the anode when the device is under high electrical stress ($>10^6$ A/cm^2) [183, 184]. The mass transport of phase change chalcogenide under electrical stress can be observed using an on-substrate structure with similar patterns to the suspended structure which generates large, linear, and periodic electrical field. TEM-EDS technique can be applied to quantify the relationship between electrical field and mass migration as well as possible compositional separation. This proposed work can provide experimental data on the compositional diffusion of the GST species under both high temperature gradient and

high electric field, which can lead to better understanding of the reliability and the failure mechanisms of phase change memory devices.

6.2.2 Fully-Coupled Multiphysics Modeling for PCM

Successful designs of PCM, especially the multibit PCM, rely on accurate prediction of the electrical, thermal, mechanical, and phase transitional behaviors of the phase change material in the nanometer scale. The simulation code in this work incorporates the coupled electrical, thermal, and phase transitional modules. The remaining mechanical model mainly concerns the stress evolution and distribution in the GST layer and its adjacent electrodes. The phase change material is known to have considerable change in volume of 6% to 9% upon crystallization which leads to a substantial amount of stress in the GST film [82, 185-188]. Furthermore, the high temperature in a PCM cell during programming cycles can introduce additional stress to the phase change material due to thermal expansion [9]. The stress can detriment the mechanical structure of the PCM cells in the forms of voids formation in the GST film [189] or delamination at the GST-electrode interface [190]. Electrical properties of the phase change material can also change under high stress level due to an altered band gap, and this effect is most significant in the drift behavior of the amorphous GST resistivity [191-193]. The temperature field and phase distribution determines the local stress field, which in turn affects the electrical properties and the crystallization rate of the GST. For these reasons, a more accurate simulation code should incorporate the stress module and couple it to the other electrical, thermal, and phase transition models. Developing and calibrating this fully-coupled multiphysics simulation code can significantly improve the understanding the complex behavior of the GST during programming operations and facilitate the PCM device design.

6.2.3 Measurement of Inelastic Electron-Interface Scattering in Mo/Si

The inelastic electron-interface scattering can be a significant path for heat transfer between a metal thin film and a dielectric thin film. This work made progress in the modeling of this effect and incorporate it into the overall energy transport process in

the metal/dielectric multilayers. The accuracy of the modeling results largely depend on the input material properties of the molybdenum film. However, some of the material property data are not readily available in the literature to the knowledge of the author. One example is the interaction constants of electrons with longitudinal and transverse phonons, β_l and β_t, in Equation (39). Future measurements on the temperature-dependent electrical resistivity of Mo film will provide more accurate β_l and β_t. Specifically, the change in electrical resistivity, $\delta\rho$, is a function of temperature T [43]:

$$\delta\rho = \frac{4\pi^2 \beta_{t,l}}{3\varepsilon_F p_F u_{t,l}} T^2 \rho_0 \tag{40}$$

where ρ_0 is a reference value which only accounts for the elastic scattering. The Fermi momentum and Fermi level are denoted as p_F and ε_F, respectively. By measuring the change in electrical resistivity of Mo as a function of temperature, one can fit the data using Equation (40) and extract the values for β_l and β_t. Recent studies have also measured the strength of the electron-interface scattering directly using transient thermal reflectance (TTR) technique for Au thin film on Si substrate [37-39]. Future experiment with a similar setup can measure the electron scattering in the Mo/Si interface. Possible sample structure includes a Mo film of ~ 40 nm on amorphous Si of a few hundred nanometers, and a Si substrate at the bottom. Such measurements can significantly improve the accuracy of the models presented in this work by providing reliable input parameters. The experimental study of electron-interface scattering of Mo/Si bilayers will also contribute to the fundamental knowledge of thermal transport across drastically different materials in the nanometer scale.

Bibliography

[1] H. S. P. Wong*, et al.*, "Phase Change Memory," *Proceedings of the Ieee,* vol. 98, pp. 2201-2227, Dec 2010.

[2] S. Raoux and D. Ielmini, "Phase Change Materials and Their Application to Nonvolatile Memories," *Chemical Reviews,* vol. 110, pp. 240-267, 2010.

[3] A. Lacaita, "Phase change memories: State-of-the-art, challenges and perspectives," *Solid-State Electronics,* vol. 50, pp. 24-31, 2006.

[4] D. M. Rowe, *Thermoelectrics handbook : macro to nano*. Boca Raton: CRC/Taylor & Francis, 2006.

[5] G. Bakan*, et al.*, "Self-heating of silicon microwires: Crystallization and thermoelectric effects," *Journal of Materials Research,* vol. 26, pp. 1061-1071, May 2011.

[6] A. I. Hochbaum and P. Yang, "Semiconductor Nanowires for Energy Conversion," *Chemical Reviews,* vol. 110, pp. 527-546, 2010/01/13 2009.

[7] K. E. Goodson and Y. S. Ju, "Heat conduction in novel electronic films," *Annual Review of Materials Science,* vol. 29, pp. 261-293, 1999.

[8] A. N. Smith and J. P. Calame, "Impact of thin film thermophysical properties on thermal management of wide bandgap solid-state transistors," *International Journal of Thermophysics,* vol. 25, pp. 409-422, Mar 2004.

[9] I. M. Park*, et al.*, "Thermomechanical properties and mechanical stresses of Ge2Sb2Te5 films in phase-change random access memory," *Thin Solid Films,* vol. 517, pp. 848-852, 2008.

[10] E. N. Zubarev, "Reactive diffusion in multilayer metal/silicon nanostructures," *Physics-Uspekhi,* vol. 54, pp. 473-498, 2011.

[11] C. Kittel, *Introduction to solid state physics*, 8th ed. Hoboken, NJ: Wiley, 2005.

[12] K. E. Goodson, "Heat Conduction Physics and Properties," *Course Reader for ME352B: Fundamentals of Heat Conduction, Stanford University,* 2008.

[13] G. Chen, "Thermal conductivity and ballistic-phonon transport in the cross-plane direction of superlattices," *Physical Review B,* vol. 57, pp. 14958-14973, Jun 15 1998.

[14] Z. Lin*, et al.*, "Electron-phonon coupling and electron heat capacity of metals under conditions of strong electron-phonon nonequilibrium," *Physical Review B,* vol. 77, Feb 2008.

[15] A. A. Joshi and A. Majumdar, "Transient Ballistic and Diffusive Phonon Heat-Transport in Thin-Films," *Journal of Applied Physics,* vol. 74, pp. 31-39, Jul 1 1993.

[16] P. E. Hopkins and P. M. Norris, "Contribution of Ballistic Electron Transport to Energy Transfer During Electron-Phonon Nonequilibrium in Thin Metal Films," *Journal of Heat Transfer-Transactions of the Asme,* vol. 131, Apr 2009.

[17] E. Swartz and R. Pohl, "Thermal boundary resistance," *Reviews of Modern Physics,* vol. 61, pp. 605-668, 1989.

[18] M. Bartkowiak and G. D. Mahan, "Heat and electricity transport through interfaces," *Recent Trends in Thermoelectric Materials Research Ii,* vol. 70, pp. 245-271, 2001.

[19] D. G. Cahill*, et al.*, "Nanoscale thermal transport," *Journal of Applied Physics,* vol. 93, p. 793, 2003.

[20] J. P. Reifenberg*, et al.*, "The impact of thermal boundary resistance in phase-change memory devices," *Ieee Electron Device Letters,* vol. 29, pp. 1112-1114, Oct 2008.

[21] Z. Li*, et al.*, "Phonon Dominated Heat Conduction Normal to Mo/Si Multilayers with Period below 10 nm," *Nano Letters,* vol. 12, pp. 3121-3126, 2012/06/13 2012.

[22] A. Majumdar and P. Reddy, "Role of electron–phonon coupling in thermal conductance of metal–nonmetal interfaces," *Applied Physics Letters,* vol. 84, p. 4768, 2004.

[23] J. Ordonez-Miranda, *et al.*, "The effect of the electron-phonon coupling on the effective thermal conductivity of metal-nonmetal multilayers," *Journal of Applied Physics,* vol. 109, May 1 2011.

[24] J. K. Chen, *et al.*, "The role of electron-phonon coupling in ultrafast laser heating," *Journal of Laser Applications,* vol. 17, pp. 63-68, Feb 2005.

[25] J. Lee, *et al.*, "Thermal conductivity anisotropy and grain structure in Ge2Sb2Te5 films," *Journal of Applied Physics,* vol. 109, p. 084902, 2011.

[26] Z. Li, *et al.*, "Grain Boundaries, Phase Impurities, and Anisotropic Thermal Conduction in Phase-Change Memory," *Electron Device Letters, IEEE,* vol. 32, pp. 961-963, 2011.

[27] J. Kuzmik, *et al.*, "Thermal characterization of MBE-grown GaN/AlGaN/GaN device on single crystalline diamond," *Journal of Applied Physics,* vol. 109, Apr 15 2011.

[28] J. G. Felbinger, *et al.*, "Comparison of GaN HEMTs on Diamond and SiC Substrates," *Electron Device Letters, IEEE,* vol. 28, pp. 948-950, 2007.

[29] T. Beechem and P. E. Hopkins, "Predictions of thermal boundary conductance for systems of disordered solids and interfaces," *Journal of Applied Physics,* vol. 106, Dec 15 2009.

[30] P. Reddy, *et al.*, "Diffuse mismatch model of thermal boundary conductance using exact phonon dispersion," *Applied Physics Letters,* vol. 87, Nov 21 2005.

[31] L. De Bellis, *et al.*, "Variations of acoustic and diffuse mismatch models in predicting thermal-boundary resistance," *Journal of Thermophysics and Heat Transfer,* vol. 14, pp. 144-150, Apr-Jun 2000.

[32] R. M. Costescu, *et al.*, "Ultra-Low Thermal Conductivity in W/Al2O3 Nanolaminates," *Science,* vol. 303, pp. 989-990, 2004.

[33] R. J. Stevens, *et al.*, "Effects of temperature and disorder on thermal boundary conductance at solid-solid interfaces: Nonequilibrium molecular dynamics simulations," *International Journal of Heat and Mass Transfer,* vol. 50, pp. 3977-3989, Sep 2007.

[34] Y. S. Ju, *et al.*, "Nanoscale Heat Conduction Across Metal-Dielectric Interfaces," *Journal of Heat Transfer,* vol. 128, p. 919, 2006.

[35] Y. S. Ju, *et al.*, "Nanoscale heat conduction across tunnel junctions," *Applied Physics Letters,* vol. 86, May 16 2005.

[36] D. Josell, *et al.*, "Thermal diffusion through multilayer coatings: Theory and experiment," *International Journal of Thermophysics,* vol. 19, pp. 525-535, Mar 1998.

[37] P. E. Hopkins, *et al.*, "Effects of electron scattering at metal-nonmetal interfaces on electron-phonon equilibration in gold films," *Journal of Applied Physics,* vol. 105, p. 023710, 2009.

[38] P. E. Hopkins and P. M. Norris, "Substrate influence in electron-phonon coup ing measurements in thin Au films," *Applied Surface Science,* vol. 253, pp. 6289-6294, May 30 2007.

[39] L. Guo, *et al.*, "Heat Transfer Across Metal-Dielectric Interfaces During Ultrafast-Laser Heating," *Journal of Heat Transfer,* vol. 134, p. 042402, 2012.

[40] P. E. Hopkins and P. M. Norris, "Relative Contributions of Inelastic and Elastic Diffuse Phonon Scattering to Thermal Boundary Conductance Across Solid Interfaces," *Journal of Heat Transfer-Transactions of the Asme,* vol. 131, Feb 2009.

[41] C. Dames and G. Chen, "Theoretical phonon thermal conductivity of Si/Ge superlattice nanowires," *Journal of Applied Physics,* vol. 95, pp. 682-693, Jan 15 2004.

[42] P. E. Hopkins, *et al.*, "Anharmonic Phonon Interactions at Interfaces and Contributions to Thermal Boundary Conductance," *Journal of Heat Transfer-Transactions of the Asme,* vol. 133, Jun 2011.

[43] A. V. Sergeev, "Electronic Kapitza conductance due to inelastic electron-boundary scattering," *Physical Review B,* vol. 58, pp. 10199-10202, Oct 15 1998.

[44] A. Sergeev, "Inelastic electron-boundary scattering in thin films," *Physica B,* vol. 263, pp. 217-219, Mar 1999.

[45] D. G. Cahill and R. O. Pohl, "Thermal-Conductivity of Amorphous Solids above the Plateau," *Physical Review B,* vol. 35, pp. 4067-4073, Mar 15 1987.

[46] D. G. Cahill, "Thermal-Conductivity Measurement from 30-K to 750-K - the 3-Omega Method," *Review of Scientific Instruments,* vol. 61, pp. 802-808, Feb 1990.

[47] T. Yamane*, et al.*, "Measurement of thermal conductivity of silicon dioxide thin films using a 3 omega method," *Journal of Applied Physics,* vol. 91, pp. 9772-9776, Jun 15 2002.

[48] B. W. Olson*, et al.*, "A practical extension of the 3 omega method to multilayer structures," *Review of Scientific Instruments,* vol. 76, May 2005.

[49] D. A. Borca-Tasciuc*, et al.*, "Thermal transport measurements in multi-wall carbon nanotube strands using the 3ω method," in *Semiconductor Thermal Measurement and Management Symposium, 2005 IEEE Twenty First Annual IEEE*, 2005, pp. 247-252.

[50] D. W. Oh*, et al.*, "Thermal conductivity measurement and sedimentation detection of aluminum oxide nanofluids by using the 3 omega method," *International Journal of Heat and Fluid Flow,* vol. 29, pp. 1456-1461, Oct 2008.

[51] R. Fallica*, et al.*, "Thermal and Electrical Characterization of Materials for Phase-Change Memory Cells†," *Journal of Chemical & Engineering Data,* vol. 54, pp. 1698-1701, 2009/06/11 2009.

[52] W. P. Risk*, et al.*, "Thermal conductivities and phase transition temperatures of various phase-change materials measured by the 3 omega method," *Applied Physics Letters,* vol. 94, pp. 101906-3, 2009.

[53] W. P. Risk*, et al.*, "In situ 3 omega techniques for measuring thermal conductivity of phase-change materials," *Review of Scientific Instruments,* vol. 79, Feb 2008.

[54] W. J. Liu*, et al.*, "Modeling and data for thermal conductivity of ultrathin single-crystal SOI layers at high temperature," *Ieee Transactions on Electron Devices,* vol. 53, pp. 1868-1876, Aug 2006.

[55] P. Kim, *et al.*, "Thermal transport measurements of individual multiwalled nanotubes," *Physical Review Letters,* vol. 87, Nov 19 2001.

[56] E. Pop, *et al.*, "Thermal conductance of an individual single-wall carbon nanotube above room temperature," *Nano Letters,* vol. 6, pp. 96-100, Jan 2006.

[57] E. Pop, *et al.*, "Heat generation and transport in nanometer-scale transistors," *Proceedings of the Ieee,* vol. 94, pp. 1587-1601, Aug 2006.

[58] S. LeBlanc, *et al.*, "Electrothermal phenomena in zinc oxide nanowires and contacts," *Applied Physics Letters,* vol. 100, Apr 16 2012.

[59] A. Marconnet, *et al.*, "Phonon Conduction in Periodically Porous Silicon Nanobridges " *Nanoscale and Microscale Thermophysical Engineering,* vol. under review, 2012.

[60] M. H. R. Lankhorst, *et al.*, "Low-cost and nanoscale non-volatile memory concept for future silicon chips," *Nat Mater,* vol. 4, pp. 347-352, 2005.

[61] Y. Yin, *et al.*, "Ultramultiple-level storage in TiN/SbTeN double-layer cell for high-density nonvolatile memory," *Applied Physics Letters,* vol. 92, p. 163509, 2008.

[62] Y. Yin, *et al.*, "Multilevel storage in lateral top-heater phase-change memory," *Ieee Electron Device Letters,* vol. 29, pp. 876-878, Aug 2008.

[63] Z. Yan, *et al.*, "Graphene quilts for thermal management of high-power GaN transistors," *Nature Communications,* vol. 3, May 2012.

[64] K. Kurabayashi, *et al.*, "Measurement of the thermal conductivity anisotropy in polyimide films," *Journal of Microelectromechanical Systems,* vol. 8, pp. 180-191, Jun 1999.

[65] W. W. Cai, *et al.*, "Thermal Transport in Suspended and Supported Monolayer Graphene Grown by Chemical Vapor Deposition," *Nano Letters,* vol. 10, pp. 1645-1651, May 2010.

[66] X. Zhang and C. P. Grigoropoulos, "Thermal conductivity and diffusivity of free-standing silicon nitride thin films," *Review of Scientific Instruments,* vol. 66, pp. 1115-1120, 1995.

[67] A. A. Balandin, *et al.*, "Superior thermal conductivity of single-layer graphene," *Nano Letters,* vol. 8, pp. 902-907, Mar 2008.

[68] H. Y. Chiu, *et al.*, "Ballistic phonon thermal transport in multiwalled carbon nanotubes," *Physical Review Letters,* vol. 95, Nov 25 2005.

[69] D. Banerjee, *et al.*, "Large-quantity free-standing ZnO nanowires," *Applied Physics Letters,* vol. 83, pp. 2061-2063, 2003.

[70] M. N. Ou, *et al.*, "Electrical and thermal transport in single nickel nanowire," *Applied Physics Letters,* vol. 92, pp. 063101-063101-3, 2008.

[71] D. Y. Li, *et al.*, "Thermal conductivity of individual silicon nanowires," *Applied Physics Letters,* vol. 83, pp. 2934-2936, Oct 6 2003.

[72] T. Kodama, *et al.*, "Heat Conduction through a DNA-Gold Composite," *Nano Letters,* vol. 9, pp. 2005-2009, May 2009.

[73] J. P. Reifenberg, *et al.*, "Thickness and stoichiometry dependence of the thermal conductivity of GeSbTe films," *Applied Physics Letters,* vol. 91, p. 111904, 2007.

[74] H. K. Lyeo, *et al.*, "Thermal conductivity of phase-change material Ge2Sb2Te5," *Applied Physics Letters,* vol. 89, Oct 9 2006.

[75] C. Peng, "Experimental and theoretical investigations of laser-induced crystallization and amorphization in phase-change optical recording media," *Journal of Applied Physics,* vol. 82, p. 4183, 1997.

[76] Y. Yang, *et al.*, "Thermal Conductivity Measurements and Modeling of Phase-Change GST Materials," *ASME Conference Proceedings,* vol. 2007, pp. 925-932, 2007.

[77] F. Merget, *et al.*, "Lateral phase change random access memory cell design for low power operation," *Microsystem Technologies-Micro-and Nanosystems-Information Storage and Processing Systems,* vol. 13, pp. 169-172, Jan 2007.

[78] A. Pirovano, *et al.*, "Scaling analysis of phase-change memory technology," in *Electron Devices Meeting, 2003. IEDM '03 Technical Digest. IEEE International*, 2003, pp. 29.6.1-29.6.4.

[79] S. Lai, "Current status of the phase change memory and its future," in *Electron Devices Meeting, 2003. IEDM '03 Technical Digest. IEEE International*, 2003, pp. 10.1.1-10.1.4.

[80] J. Lee*, et al.*, "Measurement of anisotropy in the thermal conductivity of Ge<inf>2</inf>Sb<inf>2</inf>Te<inf>5</inf> films," in *Non-Volatile Memory Technology Symposium (NVMTS), 2009 10th Annual*, 2009, pp. 52-57.

[81] M. Asheghi*, et al.*, "Thermal conduction in doped single-crystal silicon films," *Journal of Applied Physics,* vol. 91, pp. 5079-5088, Apr 15 2002.

[82] T. P. L. Pedersen*, et al.*, "Mechanical stresses upon crystallization in phase change materials," *Applied Physics Letters,* vol. 79, pp. 3597-3599, 2001.

[83] V. Weidenhof*, et al.*, "Atomic force microscopy study of laser induced phase transitions in Ge[sub 2]Sb[sub 2]Te[sub 5]," *Journal of Applied Physics,* vol. 86, pp. 5879-5887, 1999.

[84] K. Etessam-Yazdani*, et al.*, "Experimental Investigation of Scaling Effect on Thermal Transport in Nanoscale Hot Spots," *Nanoscale and Microscale Thermophysical Engineering,* vol. 13, pp. 203-217, 2009.

[85] T. H. Jeong*, et al.*, "Crystallization behavior of sputter-deposited amorphous Ge2Sb2Te5 thin films," *Journal of Applied Physics,* vol. 86, pp. 774-778, Jul 15 1999.

[86] S. Lombardo*, et al.*, "Amorphous-fcc transition in Ge(2)Sb(2)Te(5)," *Microelectronic Engineering,* vol. 87, pp. 294-300, Mar 2010.

[87] Y. J. Park*, et al.*, "Surface energy and the equilibrium shape of hexagonal structured Ge2Sb2Te5 grain," *Applied Physics Letters,* vol. 88, May 15 2006.

[88] J. P. Troadec*, et al.*, "Transport-Properties of Conducting and Semiconducting Anisotropic Mixtures," *Journal of Physics C-Solid State Physics,* vol. 14, pp. 4807-4819, 1981.

[89] T. Matsunaga and N. Yamada, "A study of highly symmetrical crystal structures, commonly seen in high-speed phase-change materials, using

synchrotron radiation," *Japanese Journal of Applied Physics Part 1-Regular Papers Short Notes & Review Papers,* vol. 41, pp. 1674-1678, Mar 2002.

[90] T. Matsunaga*, et al.*, "Structures of stable and metastable Ge2Sb2Te5, an intermetallic compound in GeTeSb2Te3 pseudobinary systems," *Acta Crystallographica Section B-Structural Science,* vol. 60, pp. 685-691, Dec 2004.

[91] N. Yamada and T. Matsunaga, "Structure of laser-crystallized Ge2Sb2+xTe5 sputtered thin films for use in optical memory," *Journal of Applied Physics,* vol. 88, pp. 7020-7028, Dec 15 2000.

[92] S. W. Ryu*, et al.*, "Phase transformation behaviors of SiO(2) doped Ge(2)Sb(2)Te(5) films for application in phase change random access memory," *Applied Physics Letters,* vol. 92, Apr 7 2008.

[93] Y. Matsui*, et al.*, "Semiconductor and semiconductor manufacturing arrangements having a chalcogenide layer formed of columnar crystal grains perpendicular to a main substrate surface," ed: United States Patent, No. US 7638786 B2, 2009.

[94] A. D. Brailsford and K. G. Major, "Thermal Conductivity of Aggregates of Several Phases Including Porous Materials," *British Journal of Applied Physics,* vol. 15, pp. 313-&, 1964.

[95] J. C. Maxwell, *A treatise on electricity and magnetism*, Unabridged 3d ed. New York: Dover Publcations, 1954.

[96] J. F. Wang*, et al.*, "A new approach to modelling the effective thermal conductivity of heterogeneous materials," *International Journal of Heat and Mass Transfer,* vol. 49, pp. 3075-3083, Aug 2006.

[97] Bernasco.J, "Conduction in Anisotropic Disordered Systems - Effective-Medium Theory," *Physical Review B,* vol. 9, pp. 4575-4579, 1974.

[98] J. P. Reifenberg*, et al.*, "Thermal Boundary Resistance Measurements for Phase-Change Memory Devices," *Ieee Electron Device Letters,* vol. 31, pp. 56-58, Jan 2010.

[99] T. Nirschl, *et al.*, "Write Strategies for 2 and 4-bit Multi-Level Phase-Change Memory," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, 2007, pp. 461-464.

[100] S. Kim, *et al.*, "Resistance and Threshold Switching Voltage Drift Behavior in Phase-Change Memory and Their Temperature Dependence at Microsecond Time Scales Studied Using a Micro-Thermal Stage," *Ieee Transactions on Electron Devices,* vol. 58, pp. 584-592, Mar 2011.

[101] A. Pirovano, *et al.*, "Low-field amorphous state resistance and threshold voltage drift in chalcogenide materials," *Electron Devices, IEEE Transactions on,* vol. 51, pp. 714-719, 2004.

[102] I. V. Karpov, *et al.*, "Fundamental drift of parameters in chalcogenide phase change memory," *Journal of Applied Physics,* vol. 102, pp. 124503-124503-6, 2007.

[103] S. Braga, *et al.*, "Voltage-Driven Partial-RESET Multilevel Programming in Phase-Change Memories," *Electron Devices, IEEE Transactions on,* vol. 57, pp. 2556-2563, 2010.

[104] N. Papandreou, *et al.*, "Drift-Tolerant Multilevel Phase-Change Memory," in *Memory Workshop (IMW), 2011 3rd IEEE International*, 2011, pp. 1-4.

[105] J. Feng, *et al.*, "Design of multi-states storage medium for phase change memory," *Japanese Journal of Applied Physics Part 1-Regular Papers Brief Communications & Review Papers,* vol. 46, pp. 5724-5728, Sep 2007.

[106] F. Rao, *et al.*, "Multilevel data storage characteristics of phase change memory cell with douhlelayer chalcogenide films (Ge(2)Sh(2)Te(5) and Sb2Te3)," *Japanese Journal of Applied Physics Part 2-Letters & Express Letters,* vol. 46, pp. L25-L27, Jan 2007.

[107] Y. F. Gu, *et al.*, "Novel phase-change material GeSbSe for application of three-level phase-change random access memory," *Solid-State Electronics,* vol. 54, pp. 443-446, Apr 2010.

[108] G. H. Oh, *et al.*, "Parallel multi-confined (PMC) cell technology for high density MLC PRAM," in *VLSI Technology, 2009 Symposium on*, 2009, pp. 220-221.

[109] D. Ventrice, *et al.*, "A phase change memory compact model for multilevel applications," *Ieee Electron Device Letters,* vol. 28, pp. 973-975, Nov 2007.

[110] D. H. Kang, *et al.*, "One-dimensional heat conduction model for an electrical phase change random access memory device with an 8F(2) memory cell (F=0.15 mu m)," *Journal of Applied Physics,* vol. 94, pp. 3536-3542, Sep 1 2003.

[111] K. C. Kwong, *et al.*, "Phase-Change Memory RESET Model Based on Detailed Cell Cooling Profile," *Ieee Transactions on Electron Devices,* vol. 58, pp. 3635-3638, Oct 2011.

[112] Y. H. Shih, *et al.*, "Understanding amorphous states of phase-change memory using Frenkel-Poole model," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, 2009, pp. 1-4.

[113] X. Q. Wei, *et al.*, "HSPICE macromodel of PCRAM for binary and multilevel storage," *Ieee Transactions on Electron Devices,* vol. 53, pp. 56-62, Jan 2006.

[114] D.-H. Kim, *et al.*, "Three-dimensional simulation model of switching dynamics in phase change random access memory cells," *Journal of Applied Physics,* vol. 101, p. 064512, 2007.

[115] D. Ielmini and Y. Zhang, "Analytical model for subthreshold conduction and threshold switching in chalcogenide-based memory devices," *Journal of Applied Physics,* vol. 102, p. 054517, 2007.

[116] I. Daniele, *et al.*, "Recovery and Drift Dynamics of Resistance and Threshold Voltages in Phase-Change Memories," *Electron Devices, IEEE Transactions on,* vol. 54, pp. 308-315, 2007.

[117] D. Fugazza, *et al.*, "Distributed-Poole-Frenkel modeling of anomalous resistance scaling and fluctuations in phase-change memory (PCM) devices," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, 2009, pp. 1-4.

[118] R. Ongaro and A. Pillonnet, "Synthetic theory of Poole and Poole-Frenkel (PF) effects," *Science, Measurement and Technology, IEE Proceedings A,* vol. 138, pp. 127-137, 1991.

[119] D. Ielmini*, et al.*, "Switching and programming dynamics in phase-change memory cells," *Solid-State Electronics,* vol. 49, pp. 1826-1832, 2005.

[120] U. Russo*, et al.*, "Modeling of programming and read performance in phase-change memories - Part I: Cell optimization and scaling," *Ieee Transactions on Electron Devices,* vol. 55, pp. 506-514, Feb 2008.

[121] J. W. Cahn, "Theory of Crystal Growth and Interface Motion in Crystalline Materials," *Acta Metallurgica,* vol. 8, pp. 554-562, 1960.

[122] D. Kuzum*, et al.*, "Nanoelectronic Programmable Synapses Based on Phase Change Materials for Brain-Inspired Computing," *Nano Letters,* 2011.

[123] J. B. Park*, et al.*, "Phase-change behavior of stoichiometric Ge2Sb2Te5 in phase-change random access memory," *Journal of the Electrochemical Society,* vol. 154, pp. H139-H141, 2007.

[124] D. Kuzum*, et al.*, "Energy efficient programming of nanoelectronic synaptic devices for large-scale implementation of associative and temporal sequence learning," in *Electron Devices Meeting (IEDM), 2011 IEEE International*, 2011, pp. 30.3.1-30.3.4.

[125] V. G. Karpov*, et al.*, "Nucleation switching in phase change memory," *Applied Physics Letters,* vol. 90, pp. 123504-3, 2007.

[126] A. L. Lacaita*, et al.*, "Electrothermal and phase-change dynamics in chalcogenide-based memories," in *Electron Devices Meeting, 2004. IEDM Technical Digest. IEEE International*, 2004, pp. 911-914.

[127] T. D. Happ*, et al.*, "Novel One-Mask Self-Heating Pillar Phase Change Memory," in *VLSI Technology, 2006. Digest of Technical Papers. 2006 Symposium on*, 2006, pp. 120-121.

[128] V. Giraud*, et al.*, "Thermal characterization and analysis of phase change random access memory," *Journal of Applied Physics,* vol. 98, pp. 013520-7, 2005.

[129] K. Bouziane, *et al.*, "DC magnetron sputtered tungsten: W film properties and electrical properties of W/Si Schottky diodes," *Applied Physics A: Materials Science & Processing,* vol. 81, pp. 209-215, 2005.

[130] P. Nath and K. L. Chopra, "Thermal conductivity of copper films," *Thin Solid Films,* vol. 20, pp. 53-62, 1974.

[131] D. W. Denlinger, *et al.*, "Thin-Film Microcalorimeter for Heat-Capacity Measurements from 1.5-K to 800-K," *Review of Scientific Instruments,* vol. 65, pp. 946-958, Apr 1994.

[132] F. Bedeschi, *et al.*, "A Bipolar-Selected Phase Change Memory Featuring Multi-Level Cell Storage," *Solid-State Circuits, IEEE Journal of,* vol. 44, pp. 217-227, 2009.

[133] I. S. Kim, *et al.*, "High performance PRAM cell scalable to sub-20nm technology with below 4F2 cell size, extendable to DRAM applications," in *VLSI Technology (VLSIT), 2010 Symposium on*, 2010, pp. 203-204.

[134] U. K. Mishra, *et al.*, "AlGaN/GaN HEMTs - An overview of device operation and applications," *Proceedings of the Ieee,* vol. 90, pp. 1022-1031, Jun 2002.

[135] Y. F. Wu, *et al.*, "30-W/mm GaNHEMTs by field plate optimization," *Ieee Electron Device Letters,* vol. 25, pp. 117-119, Mar 2004.

[136] S. Delage, "Wide band gap semiconductor reliability : Status and trends," *Microelectronics Reliability,* vol. 43, pp. 1705-1712, 2003.

[137] K. A. Filippov and A. A. Balandin, "Thermal Boundary Resistance and Heat Diffusion in AlGaN/GaN HEFTs," *Proceedings of the MRS Spring Meeting, San Francisco,* 2003.

[138] J. Das, *et al.*, "Improved Thermal Performance of AlGaN/GaN HEMTs by an Optimized Flip-Chip Design," *Electron Devices, IEEE Transactions on,* vol. 53, pp. 2696-2702, 2006.

[139] R. Gaska, *et al.*, "High-temperature performance of AlGaN/GaN HFETs on SiC substrates," *Electron Device Letters, IEEE,* vol. 18, pp. 492-494, 1997.

[140] P. Regoliosi, *et al.*, "Experimental validation of GaNHEMTs thermal management by using photocurrent measurements," *Ieee Transactions on Electron Devices,* vol. 53, pp. 182-188, Feb 2006.

[141] M. Kuball, *et al.*, "Measurement of temperature distribution in multifinger AlGaN/GaN heterostructure field-effect transistors using micro-Raman spectroscopy," *Applied Physics Letters,* vol. 82, p. 124, 2003.

[142] J. Cho, *et al.*, "Thermal Interface Resistance Measurements for AlGaN/GaN HEMT on SiC Substrate," *in preparation*.

[143] A. Sarua, *et al.*, "Thermal boundary resistance between GaN and substrate in AlGaN/GaN electronic devices," *Ieee Transactions on Electron Devices,* vol. 54, pp. 3152-3158, Dec 2007.

[144] W. Liu and A. A. Balandin, "Temperature dependence of thermal conductivity of $Al_xGa_{1-x}N$ thin films measured by the differential 3ω technique," *Applied Physics Letters,* vol. 85, p. 5230, 2004.

[145] A. Manoi, *et al.*, "Time-dependent thermal crosstalk in multifinger AlGaN/GaN HEMTs and implications on their electrical performance," *Solid-State Electronics,* vol. 57, pp. 14-18, 2011.

[146] S. T. Allen, *et al.*, "Progress in high power SiC microwave MESFETs," in *Microwave Sym. Digest, IEEE MTT-S Int'l*, 1999, pp. 321-324 vol.1.

[147] J. E. Graebner, *et al.*, "Large Anisotropic Thermal-Conductivity in Synthetic Diamond Films," *Nature,* vol. 359, pp. 401-403, Oct 1 1992.

[148] J. E. Graebner, *et al.*, "The Thermal-Conductivity of Chemical-Vapor-Deposited Diamond Films on Silicon," *Journal of Applied Physics,* vol. 71, pp. 3143-3146, Apr 1 1992.

[149] E. Worner, *et al.*, "Thermal conductivity of CVD diamond films: High-precision, temperature-resolved measurements," *Diamond and Related Materials,* vol. 5, pp. 688-692, May 1996.

[150] W. Liu and A. A. Balandin, "Thermal conduction in $Al_xGa_{1-x}N$ alloys and thin films," *Journal of Applied Physics,* vol. 97, p. 073710, 2005.

[151] C. Luo, *et al.*, "The temperature dependence of the thermal conductivity of single crystal GaN films," *Journal of Electronic Materials,* vol. 30, pp. 138 - 146, 2001.

[152] R. Kato, *et al.*, "Thermal conductivity measurement of submicron-thick films deposited on substrates by modified ac calorimetry," *International Journal of Thermophysics,* vol. 22, pp. 617-629, 2001.

[153] J. Zou, *et al.*, "Thermal conductivity of GaN films: Effects of impurities and dislocations," *Journal of Applied Physics,* vol. 92, p. 2534, 2002.

[154] A. Feldman, "Algorithm for solutions of the thermal diffusion equation in a stratified medium with a modulated heating source," *High Temperature - High Pressure,* vol. 33, pp. 293-298, 1999.

[155] H.-C. Chien, *et al.*, "Measurement and evaluation of the interfacial thermal resistance between a metal and a dielectric," *Applied Physics Letters,* vol. 93, p. 231910, 2008.

[156] X. G. Liang and B. Shi, "Two-dimensional molecular dynamics simulation of the thermal conductance of superlattices," *Materials Science and Engineering a-Structural Materials Properties Microstructure and Processing,* vol. 292, pp. 198-202, Nov 30 2000.

[157] D. G. Stearns, *et al.*, "Multilayer Mirror Technology for Soft-X-Ray Projection Lithography," *Applied Optics,* vol. 32, pp. 6952-6960, Dec 1 1993.

[158] I. Nedelcu, *et al.*, "Thermally enhanced interdiffusion in Mo/Si multilayers," *Journal of Applied Physics,* vol. 103, p. 083549, 2008.

[159] R. R. Kola, *et al.*, "Stress-Relaxation in Mo/Si Multilayer Structures," *Applied Physics Letters,* vol. 60, pp. 3120-3122, Jun 22 1992.

[160] M. I. Kaganov, *et al.*, "Relaxation between Electrons and the Crystalline Lattice," *Soviet Physics Jetp-Ussr,* vol. 4, pp. 173-178, 1957.

[161] T. Q. Qiu and C. L. Tien, "Femtosecond Laser-Heating of Multilayer Metals .1. Analysis," *International Journal of Heat and Mass Transfer,* vol. 37, pp. 2789-2797, Nov 1994.

[162] T. Q. Qiu, *et al.*, "Femtosecond Laser-Heating of Multilayer Metals .2. Experiments," *International Journal of Heat and Mass Transfer,* vol. 37, pp. 2799-2808, Nov 1994.

[163] J. M. Freitag and B. M. Clemens, "Stress evolution in Mo/Si multilayers for high-reflectivity extreme ultraviolet mirrors," *Applied Physics Letters,* vol. 73, pp. 43-45, Jul 6 1998.

[164] R. S. Rosen, *et al.*, "Silicide Layer Growth-Rates in Mo/Si Multilayers," *Applied Optics,* vol. 32, pp. 6975-6980, Dec 1 1993.

[165] J. H. Kim, *et al.*, "Application of the three omega thermal conductivity measurement method to a film on a substrate of finite thickness," *Journal of Applied Physics,* vol. 86, pp. 3959-3963, Oct 1 1999.

[166] D. G. Cahill, *et al.*, "Thermal conductivity of kappa-Al2O3 and alpha-Al2O3 wear-resistant coatings," *Journal of Applied Physics,* vol. 83, pp. 5783-5786, Jun 1 1998.

[167] B. Behkam, *et al.*, "Thermal property measurement of thin aluminum oxide layers for giant magnetoresistive (GMR) head applications," *International Journal of Heat and Mass Transfer,* vol. 48, pp. 2023-2031, 2005.

[168] P. B. Allen, "Theory of thermal relaxation of electrons in metals," *Physical Review Letters,* vol. 59, pp. 1460-1463, 1987.

[169] X. Y. Wang, *et al.*, "Time-Resolved Electron-Temperature Measurement in a Highly Excited Gold Target Using Femtosecond Thermionic Emission," *Physical Review B,* vol. 50, pp. 8016-8019, Sep 15 1994.

[170] G. Grimvall, *The electron-phonon interaction in metals*. Amsterdam ; New York: North-Holland Pub. Co. : sole distributors for the U.S.A. and Canada, Elsevier North-Holland, 1981.

[171] W. L. Mcmillan, "Transition Temperature of Strong-Coupled Superconductors," *Physical Review,* vol. 167, pp. 331-&, 1968.

[172] D. A. Papaconstantopoulos, *et al.*, "Calculations of Superconducting Properties of 32 Metals with Z Less-Than-or-Equal-to 49," *Physical Review B,* vol. 15, pp. 4221-4226, 1977.

[173] P. W. Mcmillan, "Advances in Ceramics, Vol 4, Nucleation and Crystallization in Glasses - Simmons,Jh, Uhlman,Dr, Beall,Gh," *Glass Technology,* vol. 24, pp. 207-207, 1983.

[174] S. Y. Savrasov and D. Y. Savrasov, "Electron-phonon interactions and related physical properties of metals from linear-response theory," *Physical Review B,* vol. 54, pp. 16487-16501, Dec 15 1996.

[175] E. Colavita*, et al.*, "Electronic-Structure of Nb-Mo Alloys," *Physical Review B,* vol. 20, pp. 4864-4871, 1979.

[176] J. D. Walker*, et al.*, "Electronic and structural properties of molybdenum thin films as determined by real-time spectroscopic ellipsometry," *Applied Physics Letters,* vol. 94, Apr 6 2009.

[177] D. H. Kang*, et al.*, "An experimental investigation on the switching reliability of a phase change memory device with an oxidized TiN electrode," *Journal of Applied Physics,* vol. 100, Sep 1 2006.

[178] S. M. Yoon*, et al.*, "Nanoscale observations of the operational failure for phase-change-type nonvolatile memory devices using Ge2Sb2Te5 chalcogenide thin films," *Applied Surface Science,* vol. 254, pp. 316-320, Oct 31 2007.

[179] C. Kim*, et al.*, "Direct evidence of phase separation in Ge2Sb2Te5 in phase change memory devices," *Applied Physics Letters,* vol. 94, May 11 2009.

[180] A. Pirovano*, et al.*, "Reliability study of phase-change nonvolatile memories," *Ieee Transactions on Device and Materials Reliability,* vol. 4, pp. 422-427, Sep 2004.

[181] L. Krusin-Elbaum*, et al.*, "Evidence for segregation of Te in Ge2Sb2Te5 films: Effect on the "phase-change" stress," *Applied Physics Letters,* vol. 90, Apr 2 2007.

[182] S. W. Nam*, et al.*, "Phase separation behavior of Ge(2)Sb(2)Te(5) line structure during electrical stress biasing," *Applied Physics Letters,* vol. 92, Mar 17 2008.

[183] S. W. Nam, *et al.*, "Electric-Field-Induced Mass Movement of Ge2Sb2Te5 in Bottleneck Geometry Line Structures," *Electrochemical and Solid State Letters,* vol. 12, pp. H155-H159, 2009.

[184] D. Kang, *et al.*, "Analysis of the electric field induced elemental separation of Ge2Sb2Te5 by transmission electron microscopy," *Applied Physics Letters,* vol. 95, Jul 6 2009.

[185] D. Wamwangi, *et al.*, "Crystallization kinetics of Ge4Sb1Te5 films," *Thin Solid Films,* vol. 408, pp. 310-315, Apr 3 2002.

[186] W. K. Njoroge and M. Wuttig, "Crystallization kinetics of sputter-deposited amorphous AgInSbTe films," *Journal of Applied Physics,* vol. 90, pp. 3816-3821, Oct 15 2001.

[187] W. K. Njoroge, *et al.*, "Density changes upon crystallization of Ge2Sb2.04Te4.74 films," *Journal of Vacuum Science & Technology a-Vacuum Surfaces and Films,* vol. 20, pp. 230-233, Jan-Feb 2002.

[188] Q. Guo, *et al.*, "Crystallization-induced stress in thin phase change films of different thicknesses," *Applied Physics Letters,* vol. 93, Dec 1 2008.

[189] C. Chieh-Fang, *et al.*, "Endurance Improvement of Ge2Sb2Te5-Based Phase Change Memory," in *Memory Workshop, 2009. IMW '09. IEEE International*, 2009, pp. 1-2.

[190] S. H. Hong and H. Lee, "Failure Analysis of Ge2Sb2Te5 Based Phase Change Memory," *Japanese Journal of Applied Physics,* vol. 47, pp. 3372-3375, May 2008.

[191] J. Im, *et al.*, "A microscopic model for resistance drift in amorphous Ge2Sb2Te5," *Current Applied Physics,* vol. 11, pp. E82-E84, Mar 2011.

[192] J. Im, *et al.*, "Effects of pressure on atomic and electronic structure and crystallization dynamics of amorphous Ge2Sb2Te5," *Physical Review B,* vol. 81, Jun 18 2010.

[193] M. Mitra, *et al.*, "Extremely low drift of resistance and threshold voltage in amorphous phase change nanowire devices," *Applied Physics Letters,* vol. 96, May 31 2010.